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# Current Leakage Evolution in Partially Gate Ruptured Power MOSFETs

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**Abstract**—It has been observed that power MOSFETs can experience an SEGR and continue to function with altered parameters. We propose that there are three different types of SEGR modes; the micro-break, the thermal runaway, and the avalanche breakdown. Data that demonstrates these stages of device failure are presented as well as a proposed model for the micro-break. Brief discussions of the other modes, based on analysis combined with our interpretations of the older literature, are also given.

**Index Terms**—Avalanche breakdown, power MOSFET, SEGR, thermal runaway.

## I. INTRODUCTION

**P**OWER metal oxide semiconductor field-effect transistors (MOSFETs), typically employing the double diffused metal oxide semiconductor (DMOS) architecture, have become an integral part of many spacecraft designs. Fig. 1 illustrates the common DMOS structure. Unfortunately, these devices can, under certain biasing conditions, be susceptible to a single-event burnout (SEB) and/or a single-event gate rupture (SEGR). The subject considered here is a SEGR wherein an ion hit produces a leakage current path through the gate oxide. The resulting gate-to-drain leakage from an SEGR varies over several orders of magnitude. Typical leakage in a virgin device is a few nanoamperes, while the leakage from an SEGR ranges from hundreds of nanoamperes to amps.

Tutorials on SEGR are given in three review papers [1]–[3]; however, the main focus of our experimental work is on a less familiar manifestation of SEGR that we will call the “micro-break”. This is an event wherein the gate leakage current ranges from hundreds of nanoamperes to tens of microamperes, as opposed to the much larger currents associated with a catastrophic SEGR.

Micro-breaks are obtained by operating the device at a voltage that is not large enough to produce a catastrophic SEGR, but still large enough to produce a detectable event. Micro-breaks have been seen in previous investigations (e.g., in [4], where they were called partial gate ruptures) and are the main focus in the current work. From an experimental point of view, these events have an advantage in that they are not immediately catastrophic (although a sufficient accumulation can degrade device functionality), so they can be accumulated to obtain good statistics. Statistically meaningful data sets can

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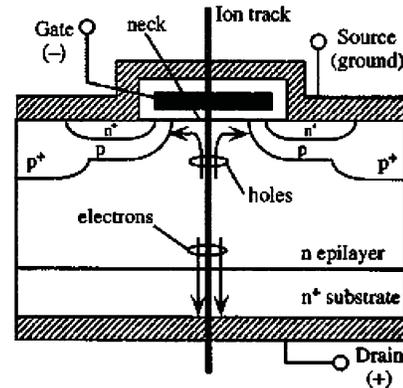


Fig. 1. Typical DMOS architecture with an ion event that triggers SEGR.

be compared to postulated physical mechanisms to test the credibility of the postulate; this is one of the objectives of the current work.

Although most of the experimental work focused on micro-breaks, we also provide a theoretical prediction of the time scale needed for a thermal runaway. This result, combined with our interpretation of the older literature, leads to the suggestion that there might be three different SEGR modes. These modes are proposed and compared in Section VI.

## II. EXPERIMENTAL PROCEDURE AND SETUP

The tested devices were a 100-V MOSFETs (IRHMS58160 and IRF1310), a 200-V MOSFET (IRHM3250), and a 500-V (IRHM8450 and IRF840) rated N-channel power MOSFET manufactured by International Rectifier. All devices were irradiated at the Texas A&M Cyclotron (TAMU) Facility. The ions selected for the experiment had a range that exceeded the length of the body region ( $> 200 \mu\text{m}$  in silicon). Two types of ions were used: xenon ( $^{129}\text{Xe}$ ) and krypton ( $^{84}\text{Kr}$  @ 25 MeV/n). All devices were biased and measured with a high-voltage source measurement unit (SMU) connected to a personal computer (PC) via a general-purpose instrument bus (GPIB). The current and voltage changes were measured in 100-ms steps and the maximum current resolution of the SMU was 1 nA. Non-destructive electrical-characterization measurements were conducted on all test devices using a curve tracer. The devices were de-encapsulated using either an acid etching machine or a micro-milling machine. Parts that did not have identical parametrics (as measured by a curve tracer) were rejected from the test lot.

During irradiations, test devices were continuously monitored for leakage currents through the gate, source, and drain terminals at a constant gate to source voltage ( $V_{GS}$ ) and a

constant drain-to-source voltage ( $V_{DS}$ ). Between irradiations, the device was tested for catastrophic SEGR by measuring the current with  $V_{GS} =$  specification maximum ( $-20$  V) and  $V_{DS} = 0$  volts, followed by  $V_{DS} =$  specification and  $V_{GS} = 0$  volts. If the DUT was still operational, the voltage was stepped up and the device was irradiated once again. Bias conditions during irradiation consisted of  $V_{GS}$  having one a value of 0,  $-10$ ,  $-15$ , or  $-20$  volts, and with  $V_{DS}$  incremented until catastrophic failure. Starting values for  $V_{DS}$  were under the SEE critical voltage.

The definition of an SEGR is the exclusive rise in gate-to-drain current. That is, the rise in gate-to-drain current is the metric by which SEGR is determined. If the rise in drain current correlates solely with a rise in source current, then SEB might have occurred and the data point will be rejected. Furthermore, any Single Event Transient (SET) wherein the source current spikes then relaxes and, therefore, might stress the device, will be rejected. In this vein, a permanent increase in drain current is a suitable metric by which to describe SEGR characteristics.

The magnitude of an SEGR can range from a 10-nA increase to a 1-A increase in gate leakage when the device is maximally biased in the off mode; as such, we define a 10-nA increase as nearly immeasurable and a 1-A increase as catastrophic device damage and failure. A natural delineation in the spectrum of SEGR damage is the post-event behavior of the event. We define a macro-break, which will be identified herein as an SEGR, as an event that immediately causes device failure through heating and oxide breakdown. That is, the SEGR site induces increasing damage until the device is no longer able to function as a transistor. Likewise, the working experimental definition of a “micro-break” includes two characteristics: 1) is a discontinuous rise in gate leakage current not greater than 10-mA while 2) the device can still hold off the applied voltage. As such, the gate impedance—not an imposed limit from the biasing source—limits the current in the device.

### III. EXPERIMENTAL DATA

It was experimentally found that the source current did not change appreciably during breakdown events, and remained orders of magnitude smaller than the gate current following a micro-break (or larger SEGR). Therefore, the gate current following a micro-break (or larger SEGR) can be measured either at the gate or at the drain. It should be noted that exceptions have been found in previous work. For example, Selva *et al.* [4] tested a variety of devices and found that most catastrophic SEGR currents were from gate to drain; however, Selva also noted that the SEGR currents were occasionally from gate to source. The absence of anomalous source currents in our experiments is interpreted to be an indication that the SEGRs are occurring in the neck region shown in Fig. 1 and in the thin oxide below the gate contact, as opposed to the thicker oxide that insulates the gate contact from the source contact.

Fig. 2 shows a typical strip chart for a heavy-ion SEGR. This 500-V-rated part experiences a microampere-order SEGR (a micro-break) at a  $V_{DS}$  of 150 V and then experiences a “full” SEGR at a  $V_{DS}$  of 200 V. Although the device might be viable for operation after the microampere event, it is unusable after the

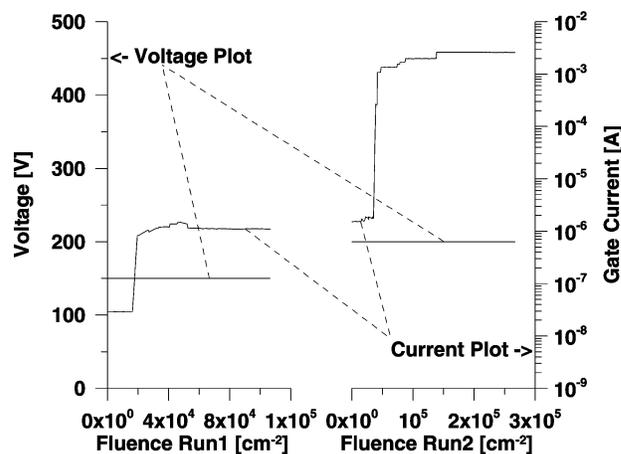


Fig. 2. Strip chart of a device that exhibited a small magnitude event when biased at 150 V (Run 1) but experienced a larger SEGR when exposed to ions at a higher voltage (Run 2). Device is a IRHM8450 (k0357) under Xe@39.8 MeV.  $\text{cm}^2/\text{mg}$  and flux of  $6500 \text{ cm}^{-2}\text{s}^{-1}$ . Both of these events are micro-breaks by the working definition. The plot epitomizes the fundamental problem upon which this study is focused.

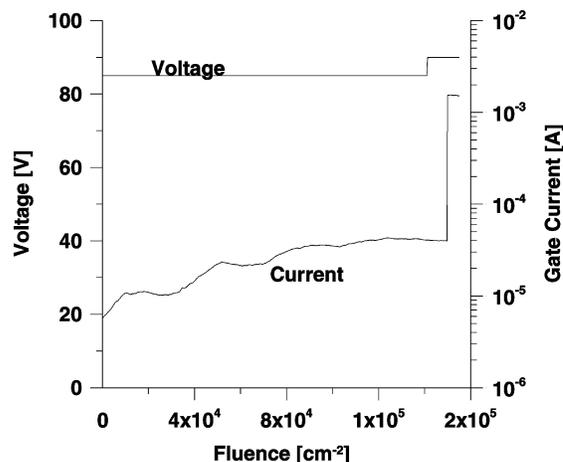


Fig. 3. A large micro-break SEGR in an IRF1310. The device can still hold off 90 V with  $\sim 2$  mA leakage. It still functions as a MOSFET while sinking almost 0.2 W. The micro-break was from Kr@19 MeV.  $\text{cm}^2/\text{mg}$  at a flux of  $1\text{e}3 \text{ cm}^{-2}\text{s}^{-1}$ .

gate leakage jumps to more than one hundred milliamps. Fig. 3 shows an SEGR that is larger than most micro-breaks, but still classified as a micro-break because the device remained functional when operating at 90 V. Prior to the break, the leakage current was barely above the charge collection noise from the beam, which is approximately 100  $\mu\text{A}$ . After the break, the current increased to approximately 2 mA. This rupture is expected to reduce lifetime and promote degradation in the gate oxide and substrate. The change in functionality before and after the SEGR is depicted in Figs. 4 and 5, which shows that a micro-break alters overall function very little, while presenting a significant risk to part reliability. The device represented by the curves is an IRF1310 irradiated with Krypton with  $V_{DS} = 90$  V and  $V_{GS} = -20$  V. The leakage from the gate to source is 1 mA when the gate is biased to 20 V. As can be seen in Fig. 5, while not ideal, the transfer curve still represents a functioning transistor. The lack of clearly defined saturation, linear, and triode

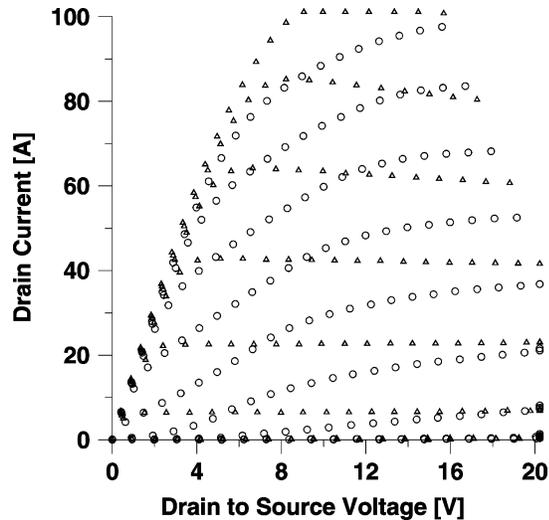


Fig. 4. Curve trace for the device in Fig. 3. The curve tracer (a 371b) saturated its readings at 100 A. The gate voltage step between curves is 1 V. The triangle symbols ( $\Delta$ ) are pre SEGR and the circles ( $\circ$ ) are post SEGR. The device still functions in principal as a MOSFET after SEGR, but the performance and reliability are affected.

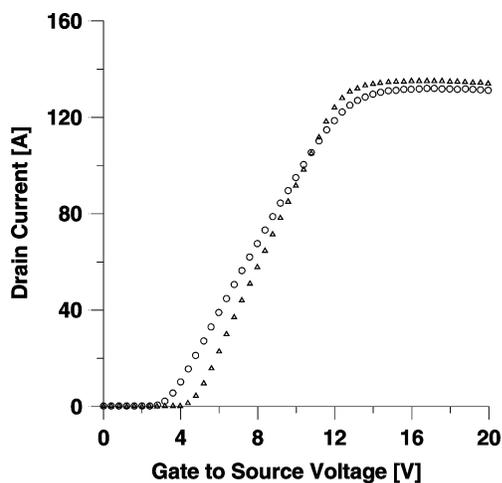


Fig. 5. Transconductance curve for the device in Fig. 3. The drain to source voltage is 30 V. The triangle symbols ( $\Delta$ ) are pre SEGR and the circles ( $\circ$ ) are post SEGR. Both transconductance and threshold voltage are reduced, which correlated with leakage through a gate damaged by radiation.

regions in Fig. 4 indicates that the leakage of the gate reduces the effectiveness of the inversion layer. Note that current in an irradiated device is lower per unit  $V_{DS}$ ; one can infer that this effect is due to the leakage from the gate damage reducing the effect  $V_{GS}$  voltage.

Devices with increased leakage will experience accelerated damage and increases in temperature. The result of this is a much earlier device failure. Fig. 6 demonstrates this. A part that experienced a micro-break is characterized on a standard 371b curve tracer. The pre-irradiation and post-irradiation curves are almost identical for  $V_{GS}$  up to 14 V; however, the post-irradiation run shows the device shorted at 14 V during the first pass on the curve tracer. The part is completely broken as of this point.

Fig. 7 shows a device biased below its "macro-SEGR" voltage (identified as 120 V in previous testing) so that micro-breaks accumulate during a single biasing condition

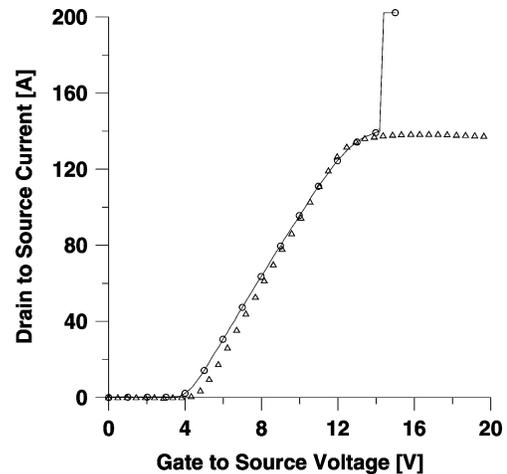


Fig. 6. Field demonstration of susceptibility of post-irradiation breakdown due to a micro-break in a device. Neither this device nor any IRF1310 prepared for testing exhibited a pre-irradiation breakdown after repackaging. The pulse width on the curve tracer was 20  $\mu$ s. This device's parameters were barely affected by the initial micro-break, which implies that even a small break can result in large failure when operation stresses are applied.

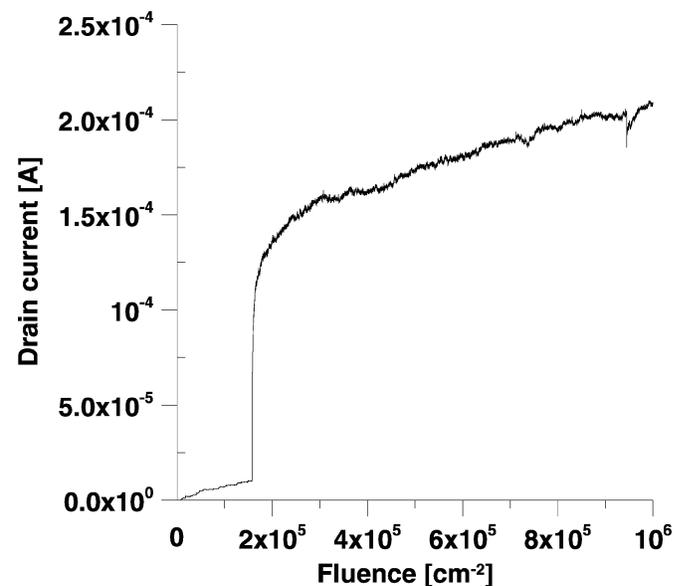


Fig. 7. The device exhibited a multitude of very-small-magnitude SEGR events accumulated during a single biasing condition. The drain-to-source voltage during irradiation was 105 V. The part is IRHM3250 tested with Xe@39.8 MeV.cm<sup>2</sup>/mg and flux was 362 ions/cm<sup>2</sup>.s. The increase in current is basically linear and distinct current jumps are discernable for low flux. The larger event at  $1.75 \times 10^5 \text{ cm}^{-2}$  demonstrates that the initial damage is not dependent on history.

using a Xe beam. The strip chart shows the increase in total gate leakage as ion irradiation occurs. This response is linear if the micro breaks are small. Note that, despite the large event at  $1.75 \times 10^5 \text{ cm}^{-2}$ , the increase is linear after this event. The total leakage increases in increments as new micro-breaks occur; these increments can be read from the recorded current measurements. Fig. 8 shows the distribution of these increments for the device shown in Fig. 7. A vast majority of the breaks occur with a mean of 2 nA. Approximately 0.01% of the breaks occur with a larger magnitude, the largest of which is 40  $\mu$ A. All of these events are quantified as microbreaks. The

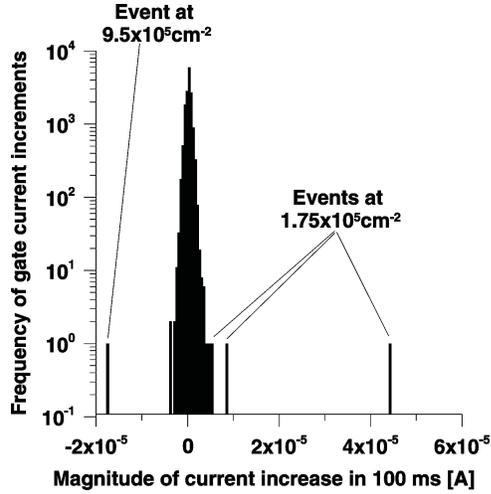


Fig. 8. A histogram of the magnitude of breaks in the device shown in Fig. 7. The difference in current after each time step of 100 ms exhibits a population of microbreaks averaging 200 nA juxtaposed to several larger events.

distribution of events in Fig. 8 shows that there are negative increases in the current. This phenomenon occurs because the definition of a change in current is the difference in 100 ms of irradiation, which results, due to thermal noise, in necessarily negative current increases. When the voltage and/or ion flux is increased, the current increases are large and the thermal noise does not result in a net negative current step. The data in Figs. 7 and 8 represent a low flux to isolate current steps; therefore, the noise is an inescapable factor.

Data such as shown in Fig. 7, but obtained from a set of devices instead of a single device, can be further analyzed by recording the increase in gate current produced by an increment of irradiation fluence as a function of applied bias. To do this, a set of IRF1310 MOSFETs was identically prepared. That is, the devices were selected from the same lot and de-packaged to expose the die using identical protocols, and then screened to have nearly identical electrical parameters. The yield of parts that have nearly identical pre-depackaging and post-depackaging parameters is about 40%. The devices were then exposed to Xenon ions for various gate-to-drain voltages while holding the gate-to-source at 0 V. It was experimentally found that, at a fixed biasing condition, the increase in gate current produced by a fluence increment was proportional to the fluence increment. Therefore, the ratio of current increase to fluence increment is an experimentally well-defined quantity at each biasing condition, but the ratio depends on the biasing. This dependence is shown in Fig. 9 to be a function of  $V_{GD}$ , when  $V_{GS}$  is zero. Each point in the figure was obtained from a different sample of the 100 V devices (note that two points at  $V_{GD} = 50$  V appear as one because they are almost on top of each other). The IRF1310 experienced no increase in current for  $V_{GD} = 40$  V. The device promptly exhibits SEGR at  $V_{GD} = 70$  V; consequently, the data point at this bias was very hard to obtain. Only one device did not immediately suffer a massive rupture. As a result, the slope of the current increase with fluence was very steep, which results in a larger error bar at this abscissa value.

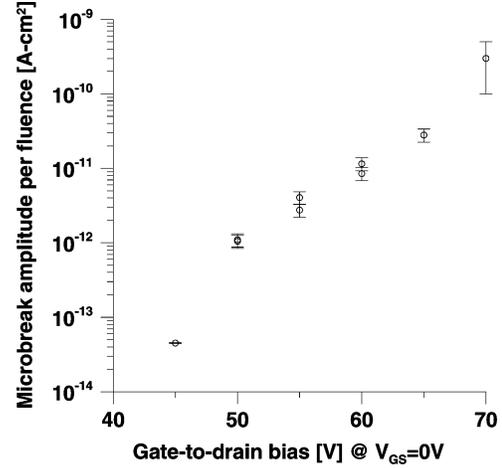


Fig. 9. Ratio of gate leakage increment to fluence increment increases with gate to drain bias. Identically prepared 100 V IRF1310s each produced one of the above points.

#### IV. DATA ANALYSIS

The plot in Fig. 9 can be compared to proposed leakage current models if the plot can be converted into a plot of leakage current versus oxide electric field strength. This conversion follows. The first step expresses the vertical axis in Fig. 9 as a measure of the oxide leakage current associated with a single but typical micro-break. The total gate current, denoted  $I_{gate}$ , is the sum of gate leakage currents summed over all micro-breaks that were created up to the time of measurement. Our analysis hypothesized that the device, which might have already been exposed to some irradiation fluence, is exposed to an additional increment of fluence  $\Delta F$ , producing an increase  $\Delta I_{gate}$  of gate current (a sum of the newly created leakage currents). The vertical scale in Fig. 9 shows the resulting ratio  $\Delta I_{gate}/\Delta F$ . Note that the fluence increment  $\Delta F$  created some number,  $N$ , of new SEGRs. The increase in device current is the sum of these new SEGR currents. Specifically,

$$\frac{\Delta I_{gate}}{\Delta F} = \frac{1}{\Delta F} \sum_{n=1}^N I_n = \left( \frac{N}{\Delta F} \right) \left( \frac{1}{N} \sum_{n=1}^N I_n \right)$$

where  $I_n$  is the gate leakage current at the  $n$ th SEGR site. The parenthesis containing the number of new events divided by the fluence increment is the cross section for producing an SEGR. The other parenthesis is the average per-SEGR current for the biasing conditions considered. Using  $X$  to denote the cross section and  $I_{avg}$  to denote the average micro-break current, the equation becomes

$$\frac{\Delta I_{gate}}{\Delta F} = X I_{avg}. \quad (1)$$

The next step converts the horizontal axis in Fig. 9 into a measure of the oxide electric field strength. The region of interest here is the neck region in Fig. 1 (which is the assumed location of an SEGR), where the oxide is above n-type silicon. Applying a negative gate bias will ordinarily produce two types of charge layers in the n-type silicon below the oxide. The upper layer is an inversion layer consisting of a narrow and dense layer of free holes (minority carriers) adjacent to the oxide. Below this is a

depletion layer consisting of uncompensated, immobile, positive-impurity (doping) ions. The voltage across the combined set of structures (oxide and silicon charge layers) is  $V_{GD}$ ; however, the way in which this voltage is divided between the oxide and the silicon charge layers depends on other factors. Ordinarily, even small reverse-bias leakage currents are enough for nearby p-n junctions to influence the inversion layer in such a way that the voltage across the oxide is controlled by  $V_{GS}$ . However, Fig. 9 shows that the situation considered here is not ordinary because the leakage current increment per fluence increment increases exponentially with  $V_{GD}$  while  $V_{GS}$  is held fixed at zero, indicating that, for this device under the tested conditions, it is  $V_{GD}$  rather than  $V_{GS}$  that controls the oxide electric field strength. An explanation is suggested by the experimental observation that the leakage current through the oxide is several orders of magnitude larger than the source current, with the latter current being the source of holes to the inversion layer. Although it is not clear how efficiently the gate leakage current removes holes from below the oxide, it will still be postulated that a gate leakage current ranging from micro-amperes to milliamperes (when summed over SEGRs) can remove holes as fast as a nano-amp source current can supply them; that is the gate leakage current prevents an inversion layer from forming. The division of voltage between the oxide layer and the silicon charge layer is then the same as it is for a MOS capacitor operating in the depletion mode with a negligible inversion layer; thus, the voltage across the oxide is controlled by  $V_{GD}$ , not by  $V_{GS}$ . This assertion is the postulated explanation for the experimental data in Fig. 9, showing that the gate leakage current has a strong dependence on  $V_{GD}$ , even though  $V_{GS}$  is held fixed at zero volts.

Although analysis of MOS capacitors is not new, because the analysis needed here consists of only a few simple steps, a review is given. Note that an ion hit creates ionization in the depletion region, which disturbs this region. However, the duration of this disturbance is measured in nanoseconds, while the current measurements in Fig. 9 are static measurements. Therefore, for the purpose of interpreting Fig. 9, these disturbances are irrelevant and a static analysis can be used. Also, in view of the large biasing voltages applied during the experiments (compared to the smaller perturbations associated with oxide surface charges [interface states] and work function differences), the analysis below will neglect surface charges and equilibrium contact potentials between different materials. An ion hit will have produced some charging in the oxide interior [5]; it is postulated here, however, that a persistent leakage current will eventually neutralize this charge. Therefore, oxide charging is also ignored in this analysis.

Let  $\Delta V_{SC}$  denote the absolute value of the voltage across the space-charge region in the silicon and let  $E_S$  denote the magnitude of the electric field in the silicon adjacent to the oxide boundary. The depletion approximation assumes that the silicon space-charge region has a sharp boundary, with negligible net charge outside this region and with a charge density inside this region equal to  $qN_D$ , where  $q$  is the elementary charge and  $N_D$  is the doping density in the n-type silicon. Using the depletion approximation,  $\Delta V_{SC}$  and  $E_S$  are related by

$$\Delta V_{SC} = \frac{\epsilon_{si}}{2qN_D} E_S^2$$

where  $\epsilon_{si}$  is the permittivity constant of silicon. Ignoring interface charges at the oxide boundary, the electric field in the oxide, denoted  $E_{oxide}$ , is related to  $E_S$  by the ratio of permittivity constants. The above equation can, therefore, be written as

$$\Delta V_{SC} = \frac{\epsilon_{ox}^2}{2qN_D\epsilon_{si}} E_{oxide}^2 \quad (2)$$

where  $\epsilon_{ox}$  is the permittivity constant of the oxide. Ignoring space charges in the oxide interior, the absolute value of the voltage across the oxide is  $E_{oxide}T$ , where  $T$  is the oxide thickness. The voltage polarities are such that the absolute value of the voltage across the oxide is added to the absolute value of the voltage across the silicon space charge region to obtain the absolute value of the voltage across the combined structure. Ignoring equilibrium contact potentials between dissimilar materials, this becomes

$$|V_{GD}| = E_{oxide}T + \Delta V_{SC}. \quad (3)$$

Combining (2) and (3) produces a quadratic equation for  $E_{oxide}$ . The solution is

$$E_{oxide} = \frac{\sqrt{T^2 + 4a|V_{GD}|} - T}{2a} \quad (4a)$$

where

$$a \equiv \frac{\epsilon_{ox}^2}{2qN_D\epsilon_{si}}. \quad (4b)$$

Although precise values for  $N_D$  and  $T$  were not measured, values that are typical for a 100-volt device (which are  $N_D = 10^{16}/\text{cm}^3$ , and  $T = 50$  nm) will be assumed for calculations. This gives

$$E_{ox}\# = \sqrt{(7.01 \times 10^4)^2 + (1.68 \times 10^5)^2 |V_{GD}\#|} - 7.01 \times 10^4 \quad (5)$$

where the dimensionless number  $E_{ox}\#$  is the numerical part of  $E_{oxide}$  when the units are volts/cm and the dimensionless number  $V_{GD}\#$  is the numerical part of  $V_{GD}$  when the units are volts.

Using the conversions given by (1) and (5), the points in Fig. 9 are re-plotted and shown as the points in Fig. 10. The curve in Fig. 10 is discussed in the next section.

## V. SUGGESTED PHYSICAL MODEL FOR THE MICRO-BREAK

The cross section in the vertical scale of Fig. 10 is assumed to be roughly equal to the geometric area of the neck region, so it is expected to be roughly constant. The vertical axis is then interpreted as being proportional to the current. To test the validity of the proposed model, the data points can be compared to a proposed physical model for leakage current. The proposed model is the tunneling of electrons from trapping sites in the oxide into the conduction band (which is a process that can be repeated to produce a steady-state current), from the metalization into the oxide conduction band (Fowler-Nordheim tunneling), or from both. The proposed explanation for an enhanced current associated with a micro-break is displacement damage caused by the ion hit in the oxide, creating a significant number of damage sites at which there is a reduced potential barrier through which the tunneling must travel. For either tunneling

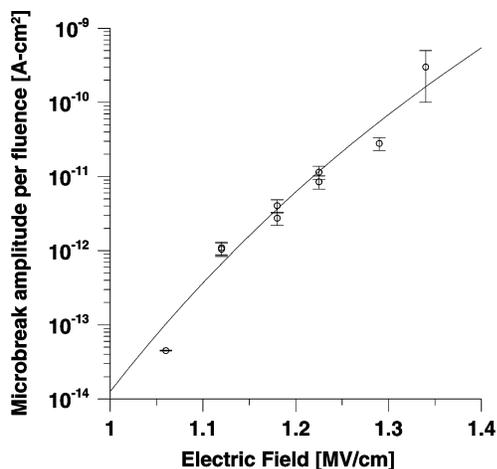


Fig. 10. The same points in Fig. 9 are plotted with a change in axis labels. The curve is a fit to (6).

mechanism (oxide trapped to oxide conduction or surrounding material to oxide conduction), the current should be given by [6]

$$I = AE_{\text{oxide}}^2 \exp\left(-\frac{B}{E_{\text{oxide}}}\right) \quad (\text{model}) \quad (6)$$

where  $A$  and  $B$  are fitting parameters. Selecting parameters to fit the points in Fig. 10 produces the curve in the figure with  $B = 35$  MV/cm. Note that if the tunneling was from either surrounding material (metallization or silicon) into the conduction band of a high-quality (undamaged) oxide, we should have  $B \approx 190$  MV/cm [7]. Also, the  $B$  parameter is proportional to the three halves power of the potential barrier through which the tunneling must travel [6], indicating that the potential barrier associated with oxide damage sites is about one-third of the potential barrier between surrounding material and the conduction band in undamaged oxide. This damage-induced potential barrier reduction seems credible, particularly if the tunneling is from oxide traps to oxide conduction (so the ion-induced defects are trapping sites). The proposed model, therefore, appears to be credible.

## VI. PROPOSED SEGR MODES

We have experimentally observed two types of SEGR:

- i) The micro-break (a steady leakage current; not a runaway).
- ii) The evolution of a micro-break into a massive breakdown, induced by electrical stress when outside of the ion beam. Although not the focus of our experimental work, there is another type of event:
- iii) The more common massive breakdowns that occur while the device is exposed to the ion beam.

Based partly on the work done here and partly on our interpretations of the older literature, we propose that the three types of events are each caused by different physical mechanisms. The physical mechanisms themselves are neither conjecture nor are they new, but the assertion that each SEGR mode is associated with a different mechanism is an unproven theory. The discussions below are intended to add some credibility to this theory.

### A. Micro-Break

As stated before, the proposed model for the micro-break is the tunneling of electrons from trapping sites in the oxide into the conduction band, from surrounding materials into the oxide conduction band, or from both. The proposed explanation for an enhanced current associated with a micro-break is that oxide defects from displacement damage caused by the ion hit create a significant number of damage sites at which there is a reduced potential barrier that the tunneling must penetrate. Note that oxide defects play a role that is qualitatively similar to the role of impurities in doped semiconductors in the sense that a finite number of defects can produce a current having unlimited time duration (i.e., a steady-state current). The underlying physics for the micro-break are probably very similar to the physics investigated in oxide reliability studies [8], with the important distinction being in the source of oxide defects (an ion hit for one case versus device currents during normal operation for the other). Enhanced leakage currents following irradiation have also been reported by other investigators (e.g., Anderson *et al.* [9]).

### B. Thermal Runaway

It has been known for quite some time that a thermal instability condition can occur in dielectrics and that the change in resistance in semiconductors at high temperatures leads to reliability effects. While tunneling is the dominant conduction mechanism at low temperatures, thermally induced mechanisms (e.g., a Frenkel-Poole emission wherein field-enhanced thermal excitation moves trapped electrons into the conduction band, with the process repeated to produce a steady-state current) become dominant at higher temperatures. Joule heating from currents flowing through the oxide increase the electrical conductivity of the oxide (via thermal generation of carriers), which, in turn, increases the current through the oxide. This regenerative process can, under certain conditions, produce an unstable condition (i.e., a thermal runaway). During the 1960s, Klein and Gafni [10] found that the thermal stability theory agrees with measured breakdown-field strengths for silicon oxides. To obtain experimental data, the authors used a self-healing property to remove oxide defects and, thereby, obtain a homogeneous oxide having macroscopic lateral dimensions (areas ranging from 0.2 to 0.02 cm<sup>2</sup>) in thin film capacitors. The temporal scale associated with these large areas results in heat conduction being quasi-static in the sense that the entire thin-film capacitor was at a nearly uniform temperature. Heat removal from the capacitor was through the ambient atmosphere. A similar study by Sze [11] found that the thermal stability theory agrees with data for silicon nitride films.

The connection between SEGR and thermal stability is that the same defects (created by an ion hit) that contribute to enhanced tunneling currents can also contribute to an enhancement of thermally induced currents. By producing defects (or weak spots) in the oxide, an ion hit can reduce the electric field strength needed for a thermal runaway. Such an event is indicated in Fig. 6, suggesting that a micro-break had evolved into a thermal meltdown while the device was operating outside of the ion beam.

### C. Avalanche Breakdown

Avalanche breakdown is the self multiplication of liberated charge due to impact ionization from a current. It will be argued below that avalanche breakdown might be the mechanism relevant to the massive breakdowns that are most frequently observed while the device is exposed to the ion beam. The argument is based on two well-known experimental observations.

The first well-known experimental observation is that device susceptibility to a catastrophic SEGR under reverse biasing conditions is strongly dependent on whether the test ions have adequate range to penetrate deep into the device. This indicates that a rearrangement of charge, liberated by the ion in the depletion region below the gate oxide, is an important factor for the type of SEGR mode seen in these experiments. This charge rearrangement reduces the portion of the device voltage that is across the depletion region and increases the portion of the device voltage that is across the gate oxide (i.e., the oxide electric field is enhanced). However, the time duration of this electric-field enhancement is measured in nanoseconds because the depletion region recovers from the ion hit, indicating that the SEGR event is a fast process.

The second well-known experimental observation is that external current limits will not prevent this SEGR because it can be driven by electrical energy stored in the parasitic capacitance of device structures.

It was noted above that the type of SEGR mode considered here is a fast process that is driven by stored electrical energy. However, an analysis in the Appendix indicates that a thermal runaway is a slow process that requires a continuous supply of electrical energy, even if the electrical energy stored in a parasitic capacitance exceeds the thermal energy needed to melt portions of the device. The reason is that the silicon below the oxide and metallization above are initially cold and remove heat from the oxide too fast for a thermal instability to occur. A thermal instability requires that the material surrounding the oxide also be hot, thereby slowing the rate of heat removal from the oxide. However, this "entire-device heating" is a slow process and requires a continuous supply of electrical energy from an external power supply (i.e., energy stored in the device capacitance is not enough). The conclusion is that the type of SEGR mode considered here is not a thermal runaway. Note that this conclusion is contrary to a suggestion by Wrobel [12] that the breakdown is a thermal runaway. Wrobel noted that the thermal energy needed to melt a localized volume (the damaged region) is available in the form of stored electrical energy, but did not include a transient thermal analysis to determine if this is sufficient for a thermal runaway. Our analysis concludes that this is not sufficient because heat is removed too fast from the volume via thermal conduction to the surrounding cooler portions of the device.

It is generally accepted that dielectric breakdown is either thermal or electric, whichever occurs first [6]. Excluding thermal leaves electric as the only possibility. Note that the maximum field strength of the Si-O bond is roughly 30 MV/cm [6]. When the electric field comes sufficiently close to this value (how close is "close enough" depends on the oxide thickness, with thinner oxides able to support stronger fields; i.e., fields that are closer to this limiting value [6]), avalanche breakdown

becomes possible. This is the suggested breakdown mechanism for this SEGR mode.

There still remains the question of what causes the electric field to approach breakdown strength. One well-known contribution is the electric field enhancement, discussed earlier, due to the depletion-region disturbance that is produced by a long-range ion track. A possible second contribution is the oxide charging discussed by Boruta *et al.* [5]. An ion hit through the oxide liberates free charge carriers in the oxide. Although most of the electrons liberated in the oxide recombine with holes, the remaining electrons are swept out by the electric field, leaving some uncompensated holes behind. This leaves a net oxide charge that, in turn, results in a non-uniform electric field in the oxide. A non-uniform field has a larger maximum (maximized in the spatial coordinates) than a uniform field governed by the same oxide voltage; this could lead to a breakdown at a voltage that is lower than what would be needed if the electric field were uniform. A possible third contribution is the silicon bump discussed by Carlotti *et al.* [13]. An ion strike through an oxide produces structural modifications at the oxide/silicon interface due to a complex set of interactions; the end result is a small silicon bump extending into the oxide. This effectively thins the oxide and creates a high-curvature region in the conducting silicon. Both effects contribute to an intense local electric field near the bump.

## VII. CONCLUSION

SEGR in power MOSFETs that do not result in an immediate massive failure of the part (that is, a SEGR where the device still works but exhibits large gate leakage) can result in a later massive failure when enough operational stress is applied to the device. This study demonstrates that the destruction of a device that has endured a micro-break is observed and expected due to device physics. Three SEGR modes are proposed: the micro-break, the thermal runaway, and the avalanche breakdown. For each mode, it is possible to define a threshold value for the oxide electric field strength to be the value that must be exceeded for the event to occur (note that the threshold might depend on the type of radiation environment). When comparing the three modes in the same environment, the micro-break has the smallest threshold electric field strength; these events, therefore, can occur at a biasing voltage below the value needed for a massive SEGR. The underlying physics of the micro-break is presumed to be similar to the physics relevant to oxide reliability, except that the damage is caused by an ion hit for the former case instead of a current-induced wear-out. If the electric field is increased above the micro-break threshold, it can reach the threshold needed for a micro-break to evolve into a massive thermal runaway. This can occur while the device is operating outside of the beam if a micro-break is already present. However, this event requires the electric field to have a long time duration, so an increase in bias voltage is needed to convert a micro-break into a thermal runaway. In contrast, the avalanche breakdown, which also requires an intense electric field, is a fast process that does not require that the electric field have a long duration. Intense but transient field enhancements, due to rearrangements of charge liberated by the ionizing particle

(with long-range particles able to produce stronger enhancements than short-range particles having the same incident LET, can trigger this event. The threshold electric field can be reached by a combination of bias voltage and transient field enhancement. Therefore, this is typically a spontaneous (i.e., immediately after the ion hit) event, and device susceptibility is greater for long-range ions than for short-range ions having the same incident LET.

These effects have the immediate implication of changing the acceptance parameters of testing devices for SEE. Referring to Fig. 2, if the definition of an SEGR is gate current leakage over 1 mA, the device fails at 200 V. This level is 50 V higher than the bias at which a smaller 1  $\mu$ A break was seen. Considering that the device would function as a MOSFET for both the 1- $\mu$ A and 1-mA leakage level, the definition of a failed part is resultantly arbitrary. That is, since an application can sustain a certain amount of leakage and the MOSFET that resides in the application can survive said leakage, the level of acceptable risk is what will determine the feasibility of the device. This results in the predictable maxim of a short mission being able to be more aggressive with high-risk parts since the shortened lifetime and increased failure probably will not be expressed over short time frames. This study does not specifically address any correlation between ion effect type or magnitude and amount of decrease in device lifetime. This study addressed the question of whether a power MOSFET that has experienced a small but significant SEGR should expect to fail in a normal operating environment. The data and calculation of this study indicated that the device will indeed fail. Later studies would obviously correlate the degree of damage of an ion, which would be measured with metrics yet to be determined, to the average and variance of the decrease in device lifetime. This correlation would allow for an estimate of failure probability for an application.

#### APPENDIX

##### TIME SCALE OF A THERMAL RUNAWAY

Two extreme time scales are considered. A thermal process will be called “slow” if it is sufficiently quasi-static to allow the spatial distribution of temperature within the device to be approximately uniform; that is, the oxide temperature is controlled by the rate of heat removal from the entire device through the ambient atmosphere (or by radiation if the device is in a vacuum). A thermal process in an oxide will be called “fast” if the temperature distribution is localized thereby enabling the metallization above the oxide and silicon below the oxide to remain much cooler than the local “hot spot” in the oxide; that is, the oxide temperature is controlled by the rate of heat removal from the oxide by thermal conduction into the surrounding cooler portions of the device. (An “intermediate” process is not considered here.) Note that a fast process can be driven by the electrical energy stored in the gate capacitance, while a slow process requires a continuous supply of energy from an external source. The objective is to compare the electric field strength required for a fast-process thermal runaway to the electric field strength required for a slow-process thermal runaway. The theory applicable to a slow process has already been developed; it is therefore, only necessary to derive the theory for a fast process.

Because a fast process is highly transient, a time-dependent heat equation is needed. The heat equation is driven by Joule heating, so the leakage electric current density must be included. Tunneling currents depend only on the electric field, while thermally induced currents depend on both temperature and electric field; therefore, when all currents are summed, the result will be a function of both temperature and electric field. The electrical current density is denoted  $J(E, T)$ , where  $E$  is the electric field in the oxide and  $T$  is the oxide temperature. Note that  $J$  increases if either  $E$  or  $T$  increases. The driven time-dependent heat equation, applied to the oxide interior, is

$$\vec{\nabla} \circ [K(T)\vec{\nabla}T(\vec{x}, t)] + J(E, T)E = \rho \frac{\partial [c(T)T(\vec{x}, t)]}{\partial t} \quad (7)$$

where  $\rho$  is the mass density of the oxide,  $c$  is the specific heat of the oxide, and  $K$  is the thermal conductivity of the oxide. While the thermal conductivity and specific heat in (7) have some temperature dependence, this dependence is much milder than the strong dependence that  $J(E, T)$  has on temperature. We must, therefore, use the approximation of treating  $K(T)$  and  $c(T)$  as constants, and attribute all of the temperature dependence to  $J(E, T)$ . Using this approximation, (7) becomes

$$K\nabla^2T(\vec{x}, t) + J(E, T)E = \rho c \frac{\partial T(\vec{x}, t)}{\partial t} \text{ in oxide interior.} \quad (8)$$

Boundary conditions and initial conditions are also needed. Before the initiation of an SEGR, the device is assumed to be at an ambient temperature denoted  $T_a$ . Also, note that the silicon below the oxide and the metallization above the oxide each have thermal conductivities that are two orders of magnitude larger than the thermal conductivity of the oxide; therefore, the silicon and metallization are approximated as ideal heat sinks at a temperature  $T_a$ . Because the oxide is regarded as a thin slab, heat conduction through the edges is not important. Boundary conditions at the edges can be selected on the basis of analytical convenience. It is convenient to use reflective boundary conditions. The initial condition and boundary conditions become

$$T(\vec{x}, t) = T_a \text{ at } t = 0 \quad (9)$$

$$T(\vec{x}, t) = T_a \text{ on upper and lower oxide boundary} \quad (10a)$$

$$T(\vec{x}, t) \text{ satisfies reflective conditions at edges.} \quad (10b)$$

The governing equations for  $T$  are (8), (9), and (10). Some properties implied by these equations can be deduced by first defining a function  $\psi$  by

$$\psi(\vec{x}) = \sin\left(\frac{\pi z}{h}\right)$$

where  $h$  is the oxide thickness and  $z$  is the vertical coordinate and is positioned so that the upper oxide boundary is at  $z = h$  and the lower boundary is at  $z = 0$ . The explicit expression

for  $\psi$  is actually less important than properties implied by this expression, which are

$$\nabla^2 \psi(\vec{x}) = -\frac{\pi^2}{h^2} \psi(\vec{x}) \text{ in oxide interior} \quad (11)$$

$$\psi(\vec{x}) = 0 \text{ on upper and lower oxide boundary.} \quad (12a)$$

$$\psi(\vec{x}) \text{ satisfies reflective conditions at edges.} \quad (12b)$$

$$\psi(\vec{x}) > 0 \text{ in oxide interior.} \quad (13)$$

Note that Green's theorem gives

$$\begin{aligned} \oint \psi \vec{\nabla} T \circ d\vec{S} - \oint (T - T_a) \vec{\nabla} \psi \circ d\vec{S} \\ = \int \psi \nabla^2 T d^3x - \int (T - T_a) \nabla^2 \psi d^3x \end{aligned}$$

where the surface integrals are over the closed oxide boundary and the volume integrals are over the oxide interior. The boundary conditions (10) and (12) imply that the surface integrals are zero; therefore, substituting (11) into the second volume integral gives

$$\int \psi \nabla^2 T d^3x = -\frac{\pi^2}{h^2} \int (T - T_a) \psi d^3x. \quad (14)$$

Now multiply (8) by  $\psi$  and integrate over the oxide, and then use (14) to substitute for one of the integrals to get

$$\begin{aligned} \rho c \frac{\partial}{\partial t} \int T \psi d^3x \\ = \int \left\{ J(E, T) E - \frac{\pi^2}{h^2} K (T - T_a) \right\} \psi d^3x. \quad (15) \end{aligned}$$

Suppose  $E$  is selected to be large enough so that the curly bracket in (15) is positive for all finite  $T$ , including values of  $T$  that might not be consistent with the heat equation. Because  $\psi$  is positive throughout the oxide interior, the assumed condition implies that the time derivative on the left is positive; therefore, the integral on the left is increasing in  $t$ . Furthermore, this increasing integral does not asymptotically approach a finite value because evaluating (15) at any finite  $T$ , including a value that exceeds any assumed asymptotic limit, still leads to the conclusion that the integral on the left is increasing. Therefore, the integral on the left side of (15) increases without bound as  $t \rightarrow \infty$ , implying that  $T$  increases without bound. Therefore, a thermal runaway will occur if  $E$  is large enough so that the curly bracket in (15) is positive for all  $T$ . This condition is satisfied by any  $E$  that exceeds  $E^*$ , where  $E^*$  is selected so that the minimum, in  $T$ , of the curly bracket is zero; that is,  $E^*$  satisfies

$$\min_{\xi} \left\{ J(E^*, \xi) E^* - \frac{\pi^2}{h^2} K (\xi - T_a) \right\} = 0.$$

This equation can also be written as

$$J(E^*, T^*) E^* - \frac{\pi^2}{h^2} K (T^* - T_a) = 0 \quad (16a)$$

where  $T^*$  is the minimizing argument and is, therefore, calculated from the equation

$$E^* \left. \frac{\partial J(E^*, \xi)}{\partial \xi} \right|_{\xi=T^*} - \frac{\pi^2}{h^2} K = 0. \quad (16b)$$

The simultaneous equations in (16) will solve for  $T^*$  and  $E^*$  each as a function of  $T_a$ . The solution for  $E^*$ , which will be denoted  $E^*(T_a)$  to display the  $T_a$  dependence, has the property that a thermal runaway will occur if  $E > E^*(T_a)$ .

The equations in (16) have the same structure as those presented by Klein and Gafni [10] for the maximum breakdown field strength in a quasi-static capacitor that dissipates heat to the ambient atmosphere. Their equations can be written as

$$J(E^*, T^*) E^* - \frac{\Gamma_a}{Ah} (T^* - T_a) = 0$$

$$E^* \left. \frac{\partial J(E^*, \xi)}{\partial \xi} \right|_{\xi=T^*} - \frac{\Gamma_a}{Ah} = 0$$

where  $A$  is the oxide area,  $T_a$  is the ambient temperature, and  $\Gamma_a$  is the thermal conductance between the capacitor and the ambient environment. The oxide area (rather than the device area that controls  $\Gamma_a$ ) appears in the above equations because this is the area that the current density is multiplied by to obtain the terminal current, which in turn controls the electrical power dissipated in the device. Note that the equations for the slow process and the equations for the fast process can be written in the same form as

$$J(E^*, T^*) E^* - \frac{\gamma}{h} (T^* - T_a) = 0 \quad (17a)$$

$$E^* \left. \frac{\partial J(E^*, \xi)}{\partial \xi} \right|_{\xi=T^*} - \frac{\gamma}{h} = 0 \quad (17b)$$

where

$$\gamma = \begin{cases} \frac{\pi^2 K}{h} & \text{for fast process} \\ \frac{\Gamma_a}{A} & \text{for slow process.} \end{cases} \quad (18)$$

For either case, we interpret  $\gamma$  as an effective conductance per unit area. The term "effective" is used for the fast process because  $\gamma$  was obtained from the time-dependent heat equation, wherein the temperature varies with both location and time, instead of a static analysis of heat transport between isothermal surfaces. The term "effective" is used for the slow process because the area divided into the conductance is the oxide area, which could be less than the device surface area that controls the thermal conductance.

The fast and slow processes are governed by the same (17) and are distinguished only by the numerical value assigned to the effective conductance per unit area,  $\gamma$ , which is given by (18). Klein and Gafni [10] solved (17) for the slow breakdown field and obtained good agreement with experimental data over a wide range of conditions. A breakdown field of several (roughly 5) MV/cm was found for  $\text{SiO}_2$  when  $\gamma \sim 0.3 \text{ W/cm}^2\text{-}^\circ\text{C}$ . The same equations will predict a breakdown field of several MV/cm for the fast process if  $\gamma$  for the fast process is roughly the same as for the slow process (with the latter being roughly  $0.3 \text{ W/cm}^2\text{-}^\circ\text{C}$ ). However, using (18) to evaluate  $\gamma$  for the fast process,

we find that the effective conductance per unit area is about five orders of magnitude larger for the fast process than for the slow process. It is clear that the electric field needed for a fast thermal instability, when heat is rapidly being removed from the oxide, is much larger than the electric field needed for a slow thermal instability when heat is slowly removed from the oxide.

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