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## **Reliability of PWB microvias for high density package assembly**

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**Abstract:** High density PWB (printed wiring board) with microvia technology is required for implementation of high density and high I/O area array packages (AAP). COTS (commercial off-the-shelf) AAP packaging technologies in high reliability versions with 1.27 mm pitch are now being considered for use in a number of NASA systems including Space Shuttle and Mars Rovers. NASA functional system designs are requiring more and more dense AAP packages and board space, which makes board microvia technology very attractive for effectively routing a large number of package inputs/outputs. However, the reliability of the fine feature microvias including via in pads is unknown for space applications.

Understanding process and QA (quality assurance) indicators for reliability are important for low risk insertion of these newly available packages and PWBs. This paper presents literature search as well as test results for a high density board subjected to various thermal cycle and reflow profiles representative of tin-lead and lead-free solder reflow. Microvias sizes ranged from two to six mil with and without filling. Daisy chain microvias monitored during the test and PWBs were cross-sectioned to determine failure and locations. Optical and SEM photographs as well as resistance changes during cycling and T<sub>g</sub>/T<sub>d</sub> (glass transition/decomposition temperature) characterisations are presented.

**Keywords:** Printed Wiring Board (PWB); microvia; lead-free; fill via; thermal cycle; Plated Through Hole (PTH); glass transition temperature (T<sub>g</sub>); delamination; thermal damage; Coefficient of Thermal Expansion (CTE).

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**Biographical notes:** Dr. Reza Ghaffarian has nearly 30 years of industrial and academic experience. For the last 15 years, he led R&D activities in BGA/CSP/CGA/SiP/MEM packaging/reliability and has been a consultant resource for all JPL/NASA's projects. He received many award including the NASA Exception Service Medal for outstanding leadership and industrial partnership. He has authored more than 150 technical papers, co-editor of a CSP book, four book chapters and two guidelines. He serves as technical Advisor/Committee to *Microelectronics Journal*, SMTA, IMAPS, IEEE IEMT/CPMT, and IPC. He received his PhD in 1982 from University of California at Los Angeles (UCLA).

## 1 Introduction

High density PWB (printed wiring board) with microvia technology is required for implementation of high density and high I/O area array packages (AAP). COTS (commercial off-the-shelf) AAP packaging technologies in high reliability versions with 1.27 mm pitch are now being considered for use in a number of NASA systems including Space Shuttle and Mars Rovers. NASA functional system designs are requiring more and more dense AAP packages and board space, which makes board microvia technology very attractive for effectively routing a large number of package inputs/outputs. However, the reliability of the fine feature microvias including via in pads is unknown for space applications.

Understanding process and QA (quality assurance) indicators for reliability are important for low risk insertion of these newly available packages and PWBs. This paper presents literature search as well as test results for a high density board subjected to various thermal cycle and reflow profiles representative of tin-lead and lead-free solder reflow. Microvias sizes ranged from two to six mil with and without filling. Daisy chain microvias monitored during the test and PWBs were cross-sectioned to determine failure and locations. Optical and SEM photographs as well as resistance changes during cycling and Tg/Td (glass transition/decomposition temperature) characterisations are presented.

## 2 Microvia technology trend

Figure 1 compares plated-through-hole (PTH), via, and microvia technologies used for conventional and fine pitch BGA (ball grid array) and CSP (chip scale package) board assemblies. The vias can be buried (providing interconnection between inner layers), semiburied (providing interconnection from one of the two outer layers to one of the internal layers), or through vias or PTHs that provide interconnection between the outer two layers. Microvias are fine feature vias that generally are blind surface vias with sizes of six mil (150  $\mu\text{m}$ ) or lower.

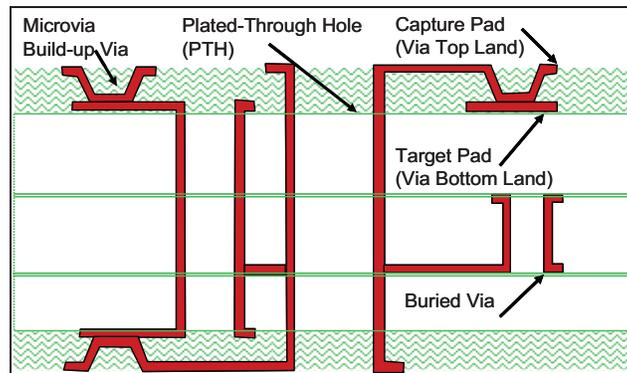
Microvia technology is now well established for use in commercial applications by means of published books, book chapters, industry guidelines, and specifications on this subject (Coombs, 2001; Lau and Ricky Lee, 2000; IPC/JPCA-2315, 2000). This technology is required when high I/O area array packages (AAP) with lower than 0.8 mm pitches (distance between adjacent ball centers) are designed for area and weight efficiency (Fjelstad et al., 2002; Ghaffarian, 2006).

Conventional PWBs with PTH vias with six mil (150  $\mu\text{m}$ ) or larger diameters are still the vias of choice used for AAP with larger pitches. PTHs serve to electrically connect different conductor layers in multilayer PWBs. For NASA space applications, this board via technology is the norm for conventional packages and AAP packages with 1.27 mm pitch.

The denser packages with tighter pitches or higher I/O with fully populated arrays of balls/columns require use of high density interconnect (HDI) technology with microvias to meet miniaturisation and performance requirements (Ghaffarian, 2002; 2006). AAP with pitches less than 0.8 mm generally require PWB boards with microvia in pad in order to accommodate electrical signal routing. The fine pitch area array packages (FPAAPs), a.k.a. CSPs, are miniaturised versions of BGAs. These are also smaller

configurations of leaded and leadless packages. Package level microvia technology and other approaches to achieve higher density interconnects (Fillion et al., 1992; Boettcher et al., 2005) are of interest, but not discussed here.

**Figure 1** Comparison of plated-through hole via and microvia technologies (see online version for colours)



### 3 Microvia reliability

Microvia reliability covers two key areas:

- 1 Reliability of PWB with microvias as formed and its resistance to normal assembly processes.
- 2 After assembly, the effects of via-in-pad (ViP) microvias on solder voids and sensitivity of the via structure to use conditions, including exposure to thermal and mechanical stresses.

In late 1990, ITRI (the former R&D division of the IPC) established limitations in size fabrication and relative reliability of various microvias. Two recent papers covered reliability of PWBs under high thermal excursion (Sauter, 2006; Freda and Barker, 2006). The development of more effective board design and appropriate standards for detecting defects under thermal exposure are other critical aspects of this technology ([www.polarinstruments.com](http://www.polarinstruments.com); [www.Hats-Tester.com](http://www.Hats-Tester.com); [www.pcbquality.com](http://www.pcbquality.com); Venkat and Hanon, 2000; Liu et al., 2002).

The effects of PWB microvia on assembly reliability also need to be considered as compared to conventional PTH technology. One of the main assembly issues for the ViP microvias is the formation of voids in solder joints. Blind ViP is the most efficient routing to accommodate high density interconnects especially for AAP with pitches lower than 0.8 mm. Voids result when gases trapped in microvias do not escape during reflow. Hajinder and Sethuraman (2004) and Grano et al. (2003) investigated the effect of package pitch size, board design including microvia sizes, surface finish, and assembly process parameters on the formation of voids. Their findings for tin-lead solder are the following:

- With the exception of 1.27 mm BGAs, as the pitch decreased, so did the occurrence of voids.
- The smaller the microvia size, the smaller the void size. The centered and off-center design microvias had the most voids. Whereas the copper-filled and inverted microvias showed virtually no voids.
- ENIG surface finish PWBs tend to generate more voids compared to IAg (immersion silver) and OSP finish; ENIG with 25% higher voids than IAg. In addition, with ENIG, voids were present at the component site after first reflow and moved to the PWB site after second reflow.

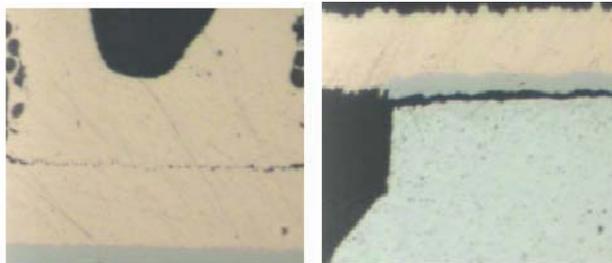
A reflow profile with extended soak above 150°C and a lower peak reflow temperature and a shorter reflow time were all effective to some extent in reducing voids. On the other hand, solder paste type, solder particle size, and double-pass paste printing had a minimum effect on voiding. The addition of silver to tin-lead eutectic solder paste decreased void size.

The four mil ViP accounted for only 6% of the total voids whereas the six and eight mil ViPs had equally high void percentages with 40% and 46%, respectively. Microvias with one layer of depth accounted for only 12% of the total voids, whereas those with three layers of depth (layer 1 to layer 3) accounted for 56% of the total voids. The thinner the PWB, the more voids produced.

Scanlan et al. (2005) investigated manufacturing issues and board level reliability for a 0.4 mm pitch FPBGA where microvias exist both in the package substrate and the PWB. Results were compared after thermal cycling, drop testing, and mechanical bending. ViP package substrates showed better resistance to thermal cycling by 20% relative to NViP package substrates. Failures were both microvia and solder joint cracking (see Figure 2). ViP/NViP combination showed excellent drop performance with the first failure after 148 drops whereas ViP-ViP combination showed poor performance with failure after seven drops. In contrast, the best bend cycling results were for the ViP-ViP followed by the NViP-ViP combinations.

Jonnaalagadda (2002) investigated the effect of ViP on the mechanical cycle bending behaviour for 196 I/O Globtop PBGA packages with one mm pitch that were assembled on PWBs with ViP structure. Test results in conjunction with finite element analysis indicated that the ViP structure by itself does not pose a reliability risk. However, increase in applied loads could induce dielectric cracking that in turn can lead to trace and via failures.

**Figure 2** Package via crack and solder joint crack during drop test (see online version for colours)



Source: Scanlan et al. (2005)

The proximity of microvias to PTHs and its effect on the reliability of microvias was evaluated by Primavera and Joshi (2001) using different vendors and exposure to liquid-liquid thermal shock (LLTS) in the range of  $-55^{\circ}/125^{\circ}\text{C}$  with ten seconds in transition. Results indicate that the maximum failures were for the vias at a distance of 40 mils from the PTHs (60 mils center to center distance from 20 mil PTH). In addition, few failures were found in the vias at the distance of five mils from the PTH. The first failure was after 1100 LLTS cycles.

Andrews et al. (2005) had experienced intermittent opens during electrical testing for a specific lot of high-end PWB assemblies having double-sided SMT. Using an IR technique, they were able to narrow failures to microvias. Cross-sectioning revealed a target pad to copper plating separation at the bottom of microvia. Further investigation showed that a small percentage of microvias exhibited barrel cracks, and sometimes, knee corner cracks.

Bora (2005) evaluated ALIVH-G (any layer interstitial via hole) board technology used for cell phones having a double stack of microvias on the outer layers. The microvias were laser drilled; the interconnections were conductive copper paste, lines and spaces were 100 and 100 microns, and vial/land of 200/400. Reliability of double-sided surface mount assemblies on an eight-layer thin board (0.8 mm thick) epoxy-glass with low moisture were evaluated after two reflow operations, one rework, and environmental exposures. Assemblies with BGA passed 500 thermal shocks in the range of  $-25^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and a 1000 hour humidity test at  $85^{\circ}\text{C}/85\%$ . Cross-sectioning revealed graininess of solder after thermal shock with no separation of the microvia connection to the capture pad. In addition, no layer-to-layer separation was observed when the phone level drop test was performed at 1.5 meters on a hard vinyl surface.

## **4 Experimental procedures**

A large number of PWBs with various sizes of microvias as well as conventional PTHs were subjected to inspection, reflow cycles, and extreme thermal cycling to determine their integrity and reliability using both nondestructive method by continuity of daisy chains and by destructive method using cross-sectional examination. Only the following aspects of evaluation are presented here.

- features of the PWB test vehicle (TV) that include microvias from two to four mils both filled and non-filled as well as eight mil through-hole vias
- visual and X-ray information on this TV
- thermal reliability results of a set of PWBs
- optical and scanning electron microscopy (SEM) of microvias revealing failures after thermal cycle exposure.

### *4.1 PWB TV features*

A test vehicle was designed and built covering both PTHs and microvias with and without filling materials. The board included BGA and FPBGA packages from 0.4 to 1.27 mm pitches with I/Os varying from 48 to 784. A TSOP package with 54 I/Os was used as control.

Table 1 lists a summary of packages and the types of microvias designed for the test vehicle. Plated-through hole via-in-pads eight mil in diameter were used only on 784 I/O BGA pads. Except for the three mil microvia diameter for one design of a 192 I/O FPBGA with 0.4 mm pitch, the rest had four mil microvias. Daisy chain microvias, however, had sizes as low as two mil and also included three and four mil microvias either filled or nonfilled as well as eight mil ViPs. The daisy chain microvias and ViPs were monitored during thermal cycling.

**Table 1** List of packages, PTHs, PTHViPs, and microvias for the test vehicle

<i>Ref Des</i>	<i>Nomenclature</i>	<i>Pitch</i>	<i>Definition</i>	<i>Via dia. &amp; definition</i>
U1	FPBGA_280_CNF	0.8mm	CNF=control non filled	4-mil (100- $\mu$ m)- $\mu$ via
U2	FPBGA_280_CNF		ONF=offset non filled	4-mil (100- $\mu$ m)- $\mu$ via
U3	FPBGA_280_RNF		RNF=runout non filled	4-mil (100- $\mu$ m)- $\mu$ via
U4	FP_CSP_48_CSP	0.8mm	CNF=control non filled	4-mil (100- $\mu$ m)- $\mu$ via
U5	FP_CSP_48_ONF		ONF=offset non filled	4-mil (100- $\mu$ m)- $\mu$ via
U6	FP_CSP_48_RNF		RNF=runout non filled	4-mil (100- $\mu$ m)- $\mu$ via
U7	784_FC_BGA	1.27mm	C8F=control – 8mil – filled	8-mil (200- $\mu$ m) – THVIP*
U8	784_FC_BGA_ONF		ONF=offset non filled	4-mil (100- $\mu$ m)- $\mu$ via
U9	KY_144_.8	0.8mm	CNF=control non filled	4-mil (100- $\mu$ m)- $\mu$ via
U10	KY_144_.8_RNF		RNF=runout non filled	4-mil (100- $\mu$ m)- $\mu$ via
U11	FPBGA_192_C4NF	0.4mm	C=control – 4mil via non filled	4-mil (100- $\mu$ m)- $\mu$ via
U12	FPBGA_192_O4NF		O=offset – 4mil via non filled	4-mil (100- $\mu$ m)- $\mu$ via
U13	FPBGA_192_R4NF		R=Runout – 4mil via non filled	4-mil (100- $\mu$ m)- $\mu$ via
U14	FPBGA_192_C3NF		C3NF=control – 3mil via non filled	4-mil (100- $\mu$ m)- $\mu$ via
U15	FPBGA_192_C3F		C3F=control – 3mil via filled	4-mil (100- $\mu$ m)- $\mu$ via
U16	FPBGA_192_C4F		C4F=control – 4mil via filled	4-mil (100- $\mu$ m)- $\mu$ via
U17	TSOP_54	0.8mm	CNF=control non filled	4-mil (100- $\mu$ m)- $\mu$ via

Note: \*THVIP = thru hole via in pad

#### 4.2 PWB TV inspection before environmental test

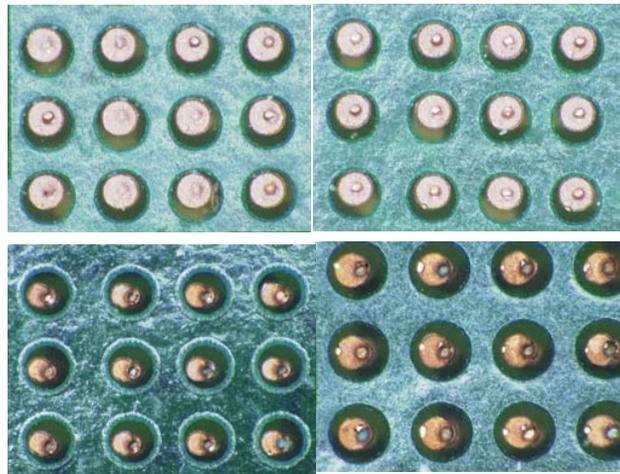
PWBs from two lots were chosen for inspection and subsequent environmental tests. Because of the cutting edge microvia technology built into the design, the first batch was considered unacceptable due to two-mil and three-mil microvia inconsistency even though the quality of most other microvias and vias was acceptable. Only a limited number of ViPs for finer pitch CSPs exhibited unacceptable microvias build due to the pad breakages. The second batch was of higher quality and considered to be acceptable

for use in assembly. Both types of PWBs were inspected by optical microscopy and X-ray to document their quality and defect types.

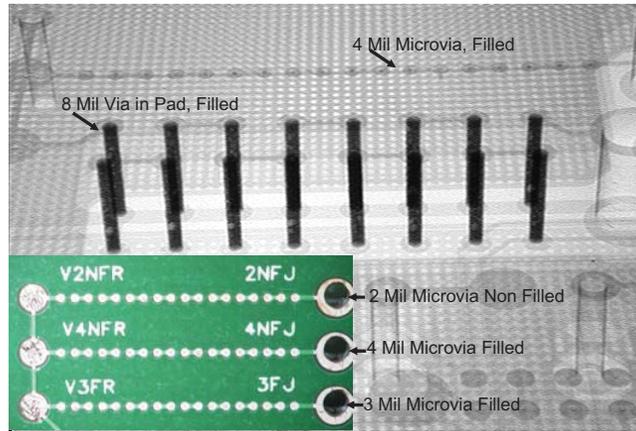
Figure 3 shows optical photomicrographs of acceptable and ‘unacceptable’ (bottom) microvias chosen from the two PWB lots. Note that visually acceptable microvias are generally located at the center of pads whereas unacceptable microvias in this case cut the pad’s edge at various distances. This condition was observed more often for finer pitch/pads array configuration than for conventional package. Even though such a condition is considered to be unacceptable from an assembly perspective, the microvia itself might be good and acceptable. Inspection by microsectioning is the only assured method of determining if the vias are acceptable.

A number of microvias were designed with a daisy-chain configuration to monitor their integrity during environmental testing. Figure 4 shows representative daisy-chaining in three photomicrographs taken by optical microscopy and X-ray. Apparent in the figure are two of the daisy-chain microvias (filled) with three and four mil diameters showing darker images by X-ray, whereas the two mil microvias are unfilled (top row daisy chain). Resistance changes of these and other daisy chains were monitored during environmental tests to determine cycles to failures.

**Figure 3** Optical photomicrographs of acceptable (top) and unacceptable microvias (see online version for colours)



**Figure 4** X-ray and optical photographs of daisy-chain microvias, filled (dark) and unfilled vias (see online version for colours)



### 4.3 Environmental test-thermal cycle profiles

Industry has proposed several specific test coupons and thermal cycling test methods with various temperature ranges and rates in order to standardise testing conditions for PWBs with PTHs and more recently for microvia characterisation and qualification. However, there are no proposed approaches for effective screening testing similar to those performed for high performance hybrid packages that cover both extreme hot and cold conditions. Such screening tests should be able to effectively discriminate behaviour between an acceptable and unacceptable PWB with microvias. Most qualification tests for commercial applications consider cost effectiveness and engineering efficiency and attempt to provide a test with the shortest possible test period.

For solder joints under thermal cycling, the dominant failure mechanisms are creep and relaxation. Adequate high temperature dwells as specified by IPC-9701A (2006) are necessary for temperature stabilisation, but dwell is of less importance for PWB evaluation where the PWB is made of polymeric materials with less dependency on creep. For PWBs, however, excessive dwell at high temperatures may cause excessive resin polymerisation, consequently rendering the board more susceptible to brittle fracture. The ramping rates of heating and cooling are usually limited by the capacity of the environmental test chamber.

The PWB TV with added daisy-chain PTHs and microvias enables monitoring of daisy chains during cycling without destruction for their integrity. Microsectioning after completion of environmental tests allows for the further comparison of the daisy chain configuration with a more realistic ViP configuration.

## 5 Test results

### 5.1 Extreme thermal cycle ( $-65^{\circ}/150^{\circ}\text{C}$ ) test results

The test thermal cycle condition ranged from  $-65^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , with a maximum rate specified in IPC-9701A (2006) (for solder joints at  $10^{\circ}\text{C}/\text{min}$ ), acceptable high heating and cooling rates, and a dwell of ten minutes at the extreme temperatures. The restriction of heating/cooling rate to condition that is well established to be acceptable for solder joint failure characterisation eliminates any concern on unwanted failures due to rapid thermal changes. In addition, this thermal cycle profile was also used to determine solder joint reliability under this condition relative to other cycle profiles (Ghaffarian, 2006).

Three PWBs were subjected to this thermal cycle range, one from the acceptable batch (SN01) and two from unacceptable batches (SN101 and SN102). Six daisy chains were monitored. These were:

- Daisy chain #1 eight mil THViP (plated-through-hole-via-in-pad)
- Daisy chain #2 four mil microvia, nonfilled
- Daisy chain #3 four mil microvia, filled
- Daisy chain #4 three mil microvia, filled
- Daisy chain #5 three mil microvia, nonfilled
- Daisy chain #6 three mil, nonfilled

Daisy chain resistances were measured prior to and during thermal cycling exposure to document cycles to failures based on changes in resistance. The PWBs were subjected to a total of 100 thermal cycles ( $-65^{\circ}/150^{\circ}\text{C}$ ); the daisy chain resistances were checked at 44 and 100 cycles. Ideally, continuous monitoring is preferred. Table 2 lists daisy chain resistances before and at 44 and 100 thermal cycles.

**Table 2** Microvia/THViP daisy chain resistance after 0, 44, and 100 thermal cycles ( $-65^{\circ}/150^{\circ}\text{C}$ ) (see online version for colours)

Daisy Chain #	SN01 – Acceptable quality resistance			SN101 – Unacceptable quality resistance			SN102 – Unacceptable quality resistance		
	RT	44~	100~	RT	44~	100~	RT	44~	100~
#1, 8mil THViP	0.4	0.4	0.4	0.3	0.3	0.3	1.1	1.1	0.5
#3, 3mil No Fill	15.6	15.6	11.1	open	open	open	open	open	open
#4, 3mil Fill	3.7	3.7	135	0.4	0.4	0.4	9.9	9.9	open
#5, 4mil No Fill	3.7	3.7	11.5	0.3	0.3	0.3	0.4	0.4	0.7
#2, 4mil Fill	1	1	1	0.3	0.3	0.3	0.4	0.4	0.4
#6, 2mil No Fill	3.6K	3.6K	163 – fluc	open	open	open	open	open	open

Note: \*RT = Pre-test/no cycle measurement done at room temperature.

Several observations can be deduced from the table:

- Via and microvia quality depends on many variables including size and whether the microvia was filled or nonfilled. For array patterns, location of the microvia relative

to the pad is also critical and becomes unacceptable if pad breakage occurs. This criterion is not apparent when daisy chain resistance is measured.

- Poor quality microvias existed for daisy chain microvias irrespective of whether the original lot was acceptable or unacceptable (ViP breakage). An initial resistance of greater than one ohm was considered to be poor quality, e.g., SN01, 3F.
- Good quality microvias existed for daisy chain microvias irrespective of whether the original lot was acceptable or unacceptable (ViP breakage). Those with low initial resistance that came from the acceptable lot always showed no resistance change to 100 thermal cycles. This is not always true for those came from an unacceptable lot, e.g., SN101, 3F.
- Large size THViP vias, e.g., case #1, passed the 100 cycles with no failures. The cutting edge two mil microvia exhibited poor quality and failed by 100 thermal cycles.
- All poor quality microvias with high initial resistance showed consistently high resistance or they became opens after 100 thermal cycles.
- Based on these limited test results, the 100 extreme thermal cycles ( $-65^{\circ}/150^{\circ}\text{C}$ ) appear to be a good screening test method even though more comprehensive tests are required to verify these test results.

## 5.2 *Tin-lead thermal reflow test results*

Three additional PWBs were subjected to a reflow cycle, one from the acceptable batch (SN02) and two from unacceptable batches (SN103 and SN104). Again, six daisy chains were monitored. These PWB TVs were subjected to 50 reflow cycles representative of the tin-lead solder paste reflow profile using a vapor phase reflow machine. Results of daisy-chain resistances before exposure (zero cycle) and after each reflow cycles are listed in Table 3. Measurement was done at RT using an ohmmeter after the completion of each reflow cycle of the 50 reflows. Only selective measurements after ten reflows, every five measurement, are shown in the table.

It is interesting to note that initially before environmental testing, only one microvia daisy chain from the unacceptable lot (SN104, three mil nonfilled) showed an open out of a total of 18 chains. These vias had apparently better quality than the previous ones used for the  $-65^{\circ}$  to  $150^{\circ}\text{C}$  thermal cycling. The rest had chain resistances generally less than 0.5 ohm including probe wires. Therefore, they are assumed to have acceptable quality. Verification by microsectioning is a must to determine microvia quality acceptance.

After reflow exposure, microvia failures occurred at different cycles depending on via size and type of PWB with no obvious trend. The only trend that appears to be consistent to reflow cycle is the failures at the two extreme via sizes. The largest size, eight mil THViP, showed no failure to 50 cycles whereas the smallest size, two mil microvia, failed early, between two and three reflow cycles. During cycling, however, the two mil via from the acceptable lot showed high resistance after three reflow cycles, but resistance is reduced in higher cycles, and near 50 reflow cycles it became open. Failures for other microvias for both acceptable and unacceptable lots were between three and nine reflow cycles.



At the start of the test, it was thought that reflow cycling could be used as a screening test method since it is fast and easy to implement. However, these test data indicate that the reflow thermal cycle test method, even though it provides some insight into microvia workmanship, is not a clear discriminator test for determining the quality of microvia daisy chains. Further work is required to substantiate these test results.

5.3 SEM and optical characterisation after cycling

Cross-sectioning with subsequent optical and SEM characterisation was carried out to determine microvia quality and to compare these techniques to the daisy-chain resistance monitored during thermal cycling. Figure 5 shows a representative of optical photomicrographs of microvias and THViPs. Optical inspection and photomicrographs can provide some insight as to the quality of microvias, but because of their fine sizes, other more power techniques such as SEM are required to better characterise failures. A representative of SEM photomicrography showing a failure is included in Figure 6.

Figure 5 Optical photomicrographs of cross sectioned microvias and THViPs after 100 thermal cycles (-65°/150°C) (see online version for colours)

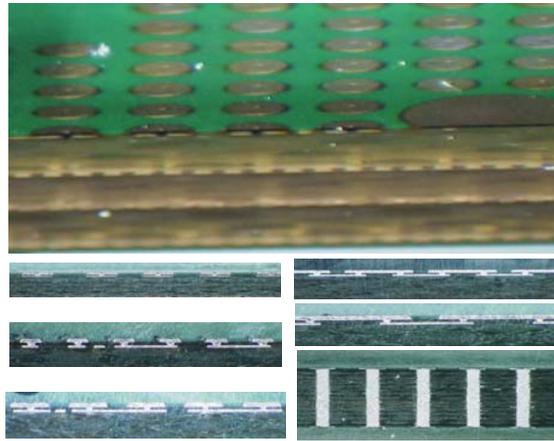


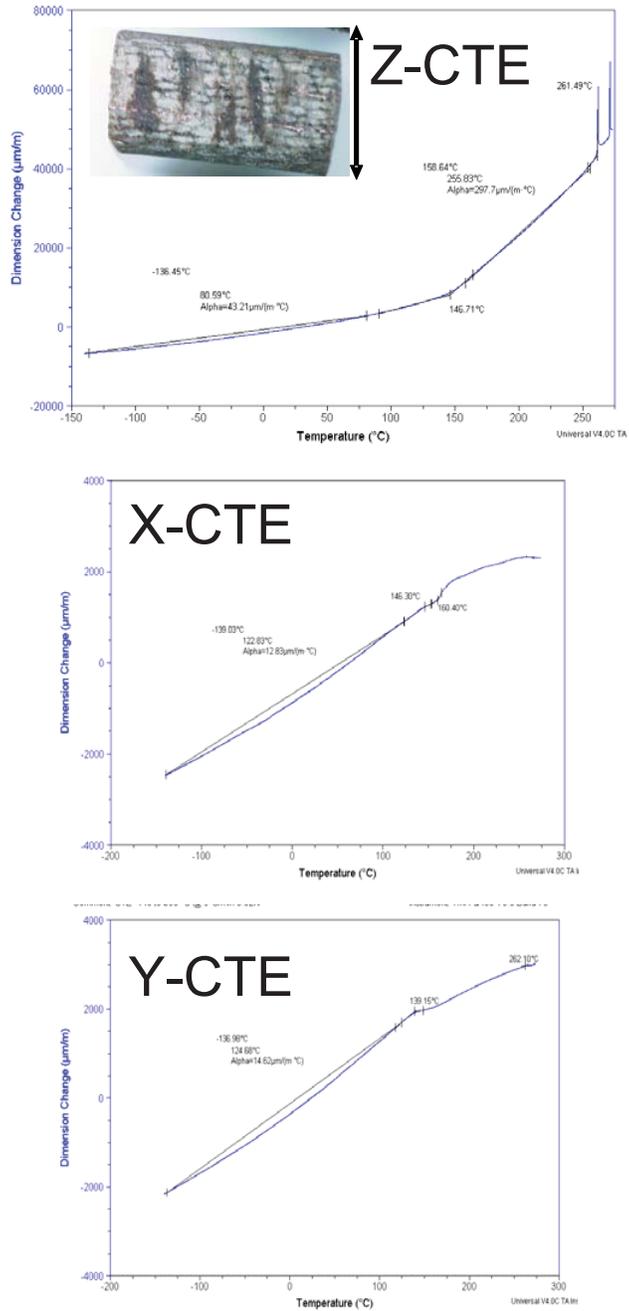
Figure 6 SEM photomicrographs cross-sectioned from a three mil nonfilled microvia after 100 thermal cycles (-65°/150°C)



Note: The microvias are filled even though a nonfilled condition set at design.

5.4 Tg and capability for lead-free reflow temperature

Figure 7 The x, y, z CTEs by TMA for a thermal-cycled PWB (see online version for colours)



Since there was minor PWB damage due to 100 thermal cycles, representative samples from a cycled PWB, SN01, were characterised for Tg, CTE, and extreme thermal cycles. The expansion variation and therefore Tg, CTEs in x/y/z, and exposure to thermal cycling in the range of  $-150^{\circ}\text{C}$  to  $+275^{\circ}\text{C}$  were all carried out using suitable thermal mechanical analysis (TMA) equipment. Generally high stress in a PWB via or microvia occurs due to through-thickness (z direction) thermal expansion during a thermal excursion.

Figure 7 shows thermal expansion and CTEs for the z, x, and y directions, respectively. The CTE for the z direction is 43.21 ppm, which is about three times that of the y and x directions having values of 14.62 and 12.83 ppm, respectively. Above the Tg, the CTE in the z direction significantly increases and become 297.7 ppm. The Tg of the PWB is about  $145^{\circ}\text{C}$  ( $146.71^{\circ}\text{C}$ ). The Tg experiences significant changes detected at about  $260^{\circ}\text{C}$ . After exposure to this temperature, the sample was cooled to RT, and it was noticed that the PWB had delaminated. It was presumed that at lower temperatures, even with repetitive exposure, delamination would not occur.

The peak reflow temperature was reduced to  $245^{\circ}\text{C}$ , representing a lead-free solder joint assembly process. Again, the TMA technique was used to determine microvia behaviour under this and a lower extreme temperature using a thermal cycle in the range of  $-100^{\circ}\text{C}$  to  $245^{\circ}\text{C}$ . Three thermal cycles were executed, while at the same time dimensional changes due to thermal cycling were continuously monitored by TMA. There was a small deviation in CTEs during the second cycle, but the deviation disappeared during the third cycle. Visual inspection after one, two, and three cycles revealed no delamination. Figure 8 compares samples from this (bottom photo) and the previous one with thermal excursion to  $260^{\circ}\text{C}$ . No delamination was noted for the  $245^{\circ}\text{C}$  maximum reflow temperature.

**Figure 8** Condition of TMA samples: the top one exposed to one cycle ( $-100^{\circ}$  to  $+275^{\circ}\text{C}$ ) and the bottom one exposed to three thermal cycles ( $-100^{\circ}$  to  $+245^{\circ}\text{C}$ ) (see online version for colours)



## 6 Summary and findings

HDI technology with six mil or smaller size microvias is required to implement the finer pitch area array packages. Key issues and findings from the literature survey and test results are summarised in the following:

- For conventional multilayer PWB and array packages with 1–1.27 mm pitch, PTHs could be used. However, it should be born in mind that the most common thermally induced board failures are due to PTHs.
- Microvia reliability involves two aspects: failures due to PWB microvia build and subsequent assembly processes and failures due to void formation in the solder with subsequent potential failure during field thermal and mechanical exposures.
- Regarding microvia reliability, only limited work has been performed by others. The effects of various board and manufacturing parameters on ViP void formation at board sites, the combination of ViP/NViP in package substrates and ViP/NViP on PWBs, and the effect of distance of microvias to PTHs are among the various issues of microvia reliability that have been investigated.
- Visual inspection using optical microscopy was more effective in determining the condition of the microvias than X-rays. X-ray radiography clearly identified filled vias but was of limited value for detecting other conditions. Added daisy chain pattern representative of microvia type/size/fill for evaluation was found to be valuable. Verification by microsectioning is a must similar to PTH requirement for high reliability application.
- Results after 100 thermal cycles ( $-65^{\circ}/150^{\circ}\text{C}$ ) revealed that microvia reliability depends heavily on size and whether they were filled or nonfilled. The eight mil THViPs passed the 100 thermal cycles with no failures, whereas the state-of-the-art two mil microvias showed poor quality and failed due to 100 thermal cycles.
- Cross-sectional examination after 100 thermal cycles revealed cracks at via/layer interface for the two mil microvias, but no appreciable cracks for any other vias.
- After 50 reflow cycles (tin-lead, RT to  $217^{\circ}\text{C}$ ), the largest eight mil vias showed no failures, whereas the two mil microvias all failed after only a few reflow cycles based on daisy-chain resistance measurements.
- TMA characterisation of cycled PWBs revealed that the Tg of the test board was about  $150^{\circ}\text{C}$  with delamination starting at  $260^{\circ}\text{C}$ .
- TMA was also used to thermal cycle specimens between  $-100^{\circ}\text{C}$  and  $245^{\circ}\text{C}$ . The latter temperature is representative of the maximum temperature for a lead-free assembly. After three cycles, no delamination was observed. The samples exposed to  $260^{\circ}\text{C}$ , however, did exhibit delamination.
- Based on the overall test results and failures, it appears that the 100 extreme thermal cycles ( $-65^{\circ}/150^{\circ}\text{C}$ ) is a good screening test method even though more comprehensive tests are required to verify these test results. A good thermal profile should cover both cold and hot temperatures in order to induce severe stresses due to

cold exposure by being far from the T<sub>g</sub> of PWB and at hot temperature by just being close to the T<sub>g</sub>, but not higher to avoid unacceptable failures.

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