

Advanced Embedded Active Assemblies for Extreme Space Applications

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Abstract—This work describes the development and evaluation of advanced technologies for the integration of electronic die within membrane polymers.¹² Specifically, investigators thinned silicon die, electrically connecting them with circuits on flexible liquid crystal polymer (LCP), using gold thermo-compression flip chip bonding, and embedding them within the material. Daisy chain LCP assemblies were thermal cycled from -135 to +85°C (Mars surface conditions for motor control electronics). The LCP assembly method was further utilized to embed an operational amplifier designed for operation within the Mars surface ambient. The embedded op-amp assembly was evaluated with respect to the influence of temperature on the operational characteristics of the device. Applications for this technology range from multifunctional, large area, flexible membrane structures to small-scale, flexible circuits that can be fit into tight spaces for flex to fit applications.

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1. INTRODUCTION

Integrating microelectronics into membrane materials to provide multifunctional and adaptive capabilities will enable new mission concepts for NASA and DoD. Such highly integrated, multifunctional, large area, flexible membrane structures would allow low cost, low launch volume and high performance future missions. Some specific applications are membrane antennas for space-

based radar, membrane solar arrays for space power systems, integral health monitoring sensors for membrane radar and solar sails. One example of a NASA application that would benefit greatly from the technology being evaluated in this proposal is Synthetic Aperture Radar (SAR) for surface deformation, topography, soil moisture and land cover change. In order to maximize Earth coverage and minimize revisit times, such SAR systems would need to be placed in Medium or Geosynchronous Earth Orbit (MEO or GEO), requiring respective antenna sizes of 400m² and 700m². The large mass and stow volume of a phased array antenna of this size that is built using conventional technologies would greatly exceed the maximum capacity of all available launch vehicles. However, a membrane antenna with embedded electronics would make this mission possible.

In addition, systems requiring electronics to fit into small or irregularly shaped cavities will greatly benefit from this technology. This work provides a whole new realm of possible configurations for electronic systems in environments such as the Mars ambient which require wide, low temperature cycle reliability.

2. MATERIALS SELECTION AND EVALUATION

Multifunctional materials for membrane antennas will be required to perform widely contrasting roles. In the case of space-based phased arrays, the membrane is used for RF interconnect, antenna RF aperture, mechanical structure and substrate for electronics. Therefore material properties such as dielectric constant and loss tangent, strength and dynamic modulus, coefficient of thermal expansion, and dimensional stability are important. These materials need to function over a wide range of temperatures, in varying radiation environments, and for a large number of cycles depending on the specific orbit and application. Some membrane materials are excellent with respect to one or more of these functions but unusable with respect to another. Table 1 shows several material properties important in the selection of materials for membrane antennas.

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Table 1. Summary of requirements for large area, multifunctional membrane antenna materials.

Property	Requirements
Dielectric Constant (ϵ_r)	Low
Dissipation Factor/Loss Tangent ($\tan \delta$)	Low
Min. Strength to maintain flatness	50 psi
Tensile Modulus	Min. 100 ksi (prefer 300 ksi)
Coefficient of Thermal Expansion (CTE) – Room Temperature	As close to Si (8 ppm/°C) as possible w/o delaminating from Cu (16.5 ppm/°C).
Glass Transition Temperature (T_g)	Outside of operating range -100 to 120°C (application dependent)
Melt/Decomposition Temperature	> Processing temperatures 210-215°C for 63Sn37Pb
Flex Behavior	Dynamic flex (> 1000 cycles)
Solderability	pass

Based on a theoretical evaluation of available flexible printed circuit board and structural membrane polymers, two materials were selected for this evaluation: a low CTE Liquid Crystal Polymer (LCP) and a commercially available Polyimide (PI) used in printed circuit board applications. LCP was selected due to its excellent combination of mechanical and electrical properties, and especially the capability of laminating thinned Si die onto flexible circuits. PI was selected as a baseline because of its proven space reliability, along with its mature circuit fabrication technology and its superior mechanical properties.

Influence of Temperature on Mechanical Behavior

The influence of temperature on the tensile behavior of these materials is presented in Figure 1. As seen in this figure, strength decreases with increasing temperature for both polymers, with this reduction being more significant for the thermoplastic LCP. It should be noted that the stresses applied to these materials to keep the membrane flat is limited to about 50 psi, which is significantly lower than the yield strength of both materials. Nevertheless, the use of LCP should be limited to below 150°C.

Membrane Radar Specific Behavior

As well as the environmental testing described above, LCP and PI were compared with respect to their membrane radar specific behavior. The traditional method of joining separate membranes together to form large membrane apertures was employed to prepare the test samples shown in Figure 2a. Each of the samples was tested in tension, and the results of such tests revealed that there were no parent film failures, indicating that the tensile strength of LCP is more than adequate for the proposed application. As shown in Figures 2b-2d, structure wrinkling, folding crease, and random handling testing were also conducted on the .002 inch thick LCP and PI sheets, to determine their comparable capability to withstand deformation and wrinkling. When held in the

configuration shown in Figure 2b, LCP exhibited a low-level wavelike deformation at low loads and some rippling at the attachment points at higher loads. During the crease and random handling tests shown in Figures 2c and 2d, LCP was observed to retain deformation for a slightly longer time than PI. In summary, the PI exhibited superior mechanical behavior to that of LCP, but the LCP sample is more than adequate for the requirements of the present application, given that the temperature does not rise above 150°C.

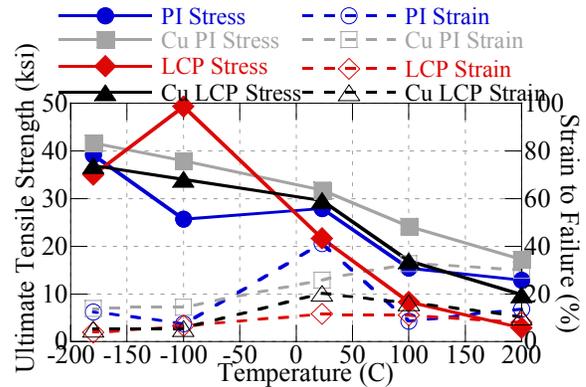


Figure 1. Influence of temperature on mechanical behavior.

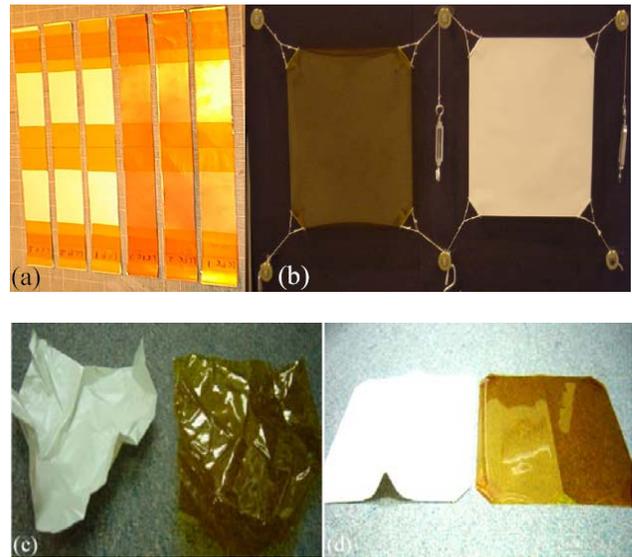


Figure 2. Photographs of PI and LCP following joining (a) and wrinkling (b-d) tests to determine the comparable membrane radar specific behavior of the two materials.

Influence of Radiation Exposure on Mechanical Behavior

PI and LCP samples were exposed to 1MeV electron radiation at dose levels of 1, 10, and 100 MRAD. The influence of this exposure on the mechanical behavior of these samples is presented in Figures 3 and 4.

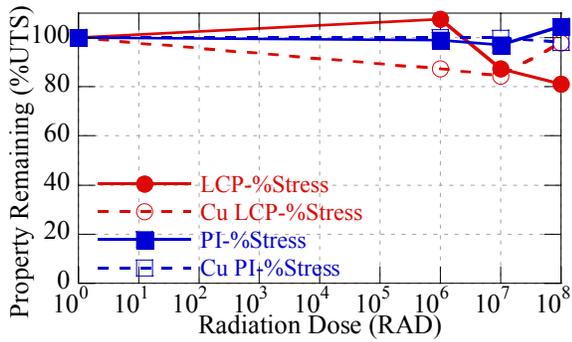


Figure 3. Influence of radiation dose on strength.

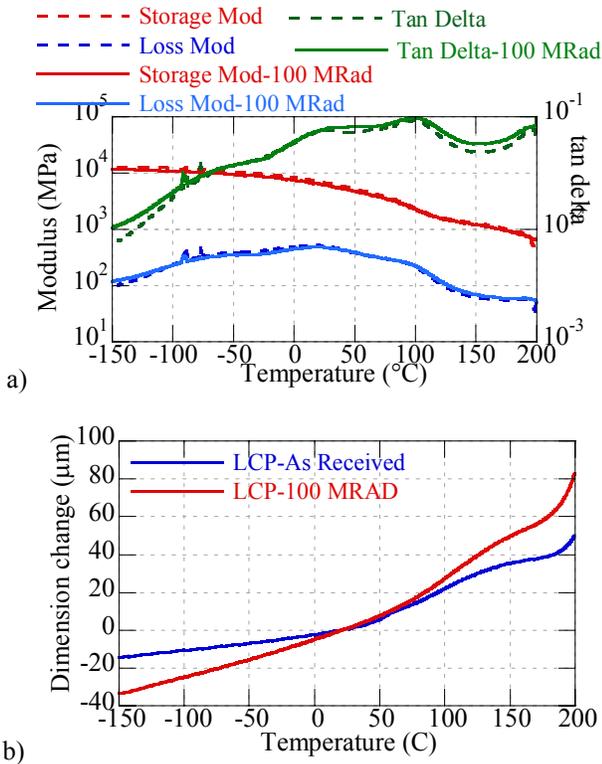


Figure 4. Influence of radiation on (a) Dynamic Mechanical and (b) Thermomechanical behavior of LCP.

As seen in Figure 3, all of the materials maintained at least 80% of their room temperature strength following up to 100 MRAD radiation. Results of Dynamic Mechanical Analyzer (DMA) and Thermal Mechanical Analyzer (TMA) testing (-150 to +200°C) of LCP films in the as-received and irradiated (100 MRAD) conditions are shown in Figure 4. The viscoelastic behavior of the film remains relatively consistent before and after radiation exposure. The difference in deflection as a function of temperature between the as-received and post-irradiation TMA curves (Figure 4b) is attributable more to a relaxation of the post-processing stresses due to sample heating during irradiation than to irradiation damage itself. As shown in Figure 5, the post-irradiated (100 MRAD) LCP sample exhibited discoloration immediately following irradiation, which annealed away with time.

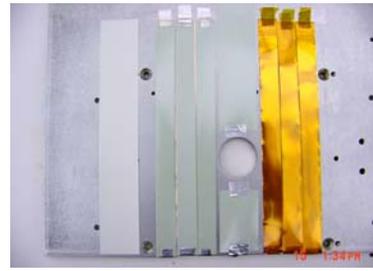


Figure 5. Photograph of 100 MRAD irradiated samples.

Influence of Radiation Exposure on Electrical Behavior

A test was performed to determine the effects of radiation on the effective dielectric and attenuation constants of LCP and PI over a range of frequencies from about 2.5 to 18GHz. The results are summarized in Figure 6.

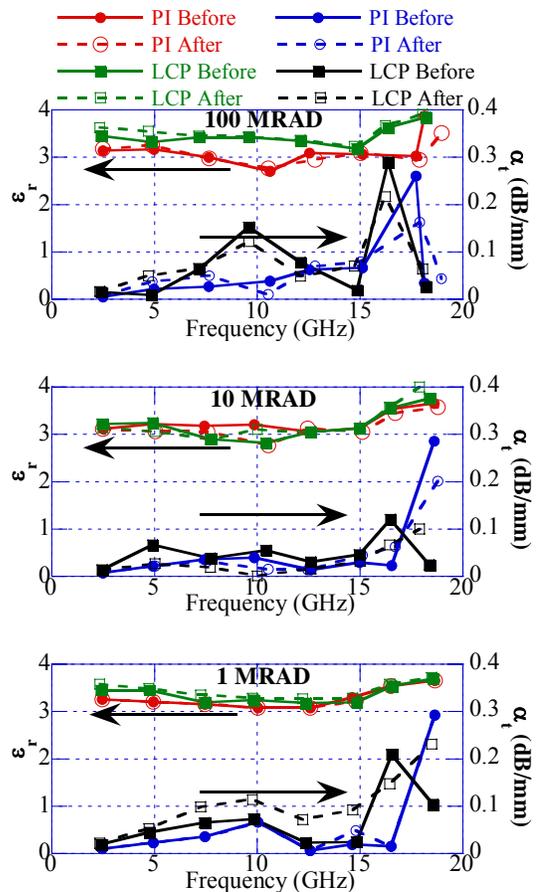


Figure 6. Plots indicating the influence of radiation on dielectric constant and attenuation.

Microstrip lines of lengths 1.5 and 3 inches were fabricated. The propagation coefficient γ of each of the lines was extracted from S-parameter measurements of the lines using the method of Gronau.[1] The complex permittivity ϵ was then found from γ , which provides the dielectric and attenuation constants. The lines were then irradiated with 1, 10, and 100 MRAD and S-parameter measurements were

made once again to find the dielectric and attenuation constants post radiation. Irradiation had minimal influence on dielectric behavior.

3. EMBEDDED DAISY-CHAIN ASSEMBLY

A technique has been developed (Figure 7) to laminate die onto LCP films.[2-4] As will be discussed, the die are thinned to $50\mu\text{m}$, integrated with the circuit on the bottom layer of LCP, and embedded within the circuit using a second layer of LCP bonded onto the backside of the circuit.

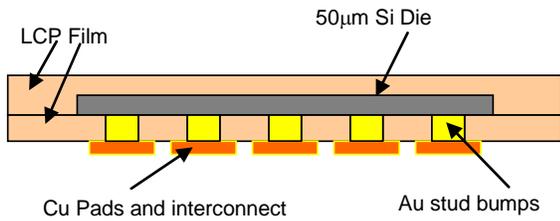


Figure 7. Illustration of LCP Substrate and Thermo-compression Bond Au Stud Bump Assembly Approach.

A key to achieving this techniques is the thinning of die to a thickness of $50\mu\text{m}$ or thinner. For the development of this process, daisy chain test die were purchased in wafer form with electroless Ni/immersion Au under bump metallurgy. These wafers were thinned as shown in Figure 8.

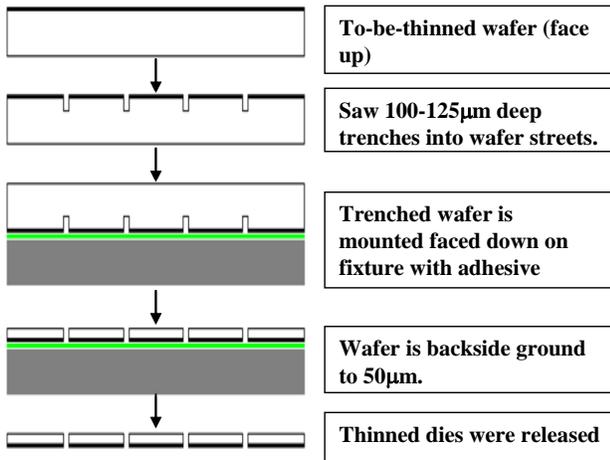


Figure 8. Flowchart of Thinning Process

A $100\text{-}125\mu\text{m}$ deep trench was sawn into dicing streets on the front side of the to-be-thinned wafer. The trenched wafer was mounted on a grinding fixture with a temporary adhesive. Sequential grinding was used to remove the bulk silicon and polish the backside of the die. When the thickness of the thinned die was less than the depth of the trenches, the trench grids were exposed and the thinned wafer was automatically turned into an array of thinned die.

The thinning process continued until the thickness reached the target value of $50\mu\text{m}$. After completion of the thinning, the thinned die are released from the grinding fixture by dissolving the adhesive. The process had high yield and there was no damage to the die edges.

As shown in Figure 9, thin die tended to curl. The radius of curvature ranged from 130 to $150\mu\text{m}$, in both the x and y directions. For ease of handling through the assembly process and to reduce the degree of die warpage, thinned die were transferred onto thick flat handle die with a temporary adhesive. The thinned die can then be packaged in or on the flexible substrate.

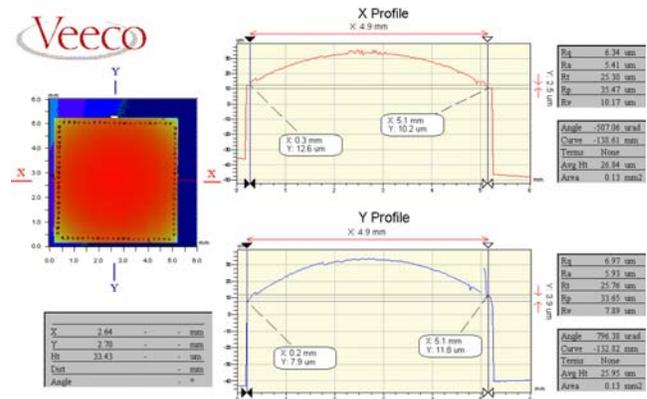


Figure 9. Surface Profile and Curvature for the $50\mu\text{m}$ die.

Double copper clad films were used to fabricate the substrates. Cu circuitry was first patterned onto the topside of the substrate. Vias were then etched into the substrate using reactive ion etching. Alternately, laser etching could be used for via formation in high volume production. Ni and Au were electroplated onto the Cu traces and the Cu exposed at the bottom of the etched vias. Figure 10 shows photographs of an LCP substrate after Ni/Au plating.

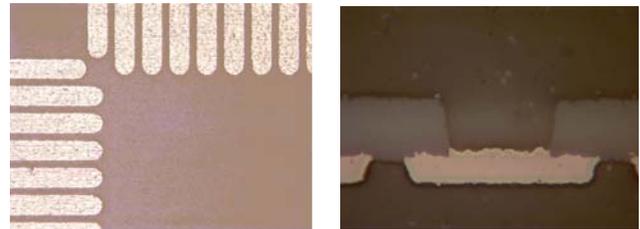


Figure 10. Photographs of (a) the circuitry side and (b) via cross-section for an LCP substrate after Ni/Au plating.

The wafers were then electroless Au plated to a thickness of $2\text{-}3\mu\text{m}$. After the thinned die were mounted on the handle die as previously described, the die were Au stud bumped. While stud bumping prior to wafer thinning would be preferred, there was concern about mounting the bumped wafer for thinning. A uniform, void free adhesive layer between the die and the handle was required to avoid

fracture of the die during thermosonic wire bonding. Scanning acoustic microscopy was used to inspect the die-to-handle attachment during the process development. The assembly process is illustrated in Figure 11. The Au stud bumped die was bonded onto the LCP substrate by thermocompression bonding. This formed the electrical connections and laminated the LCP to the active face of the die in one step, eliminating the need for underfill. A cross section of a stud bump connection is shown in Figure 12.

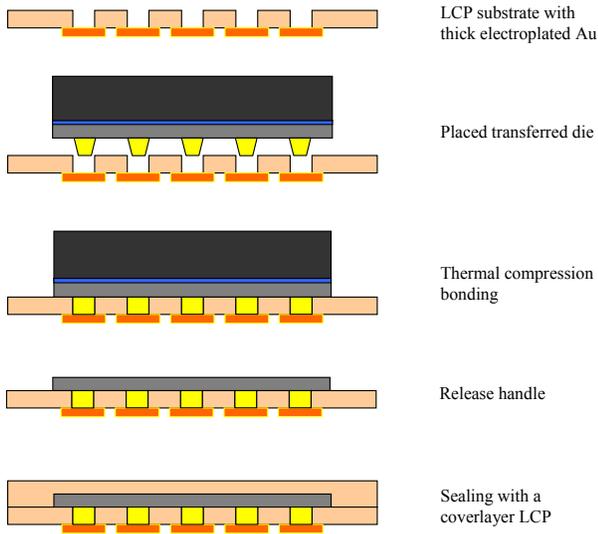


Figure 11. Illustration of the embedded assembly process with gold stud bump connections.

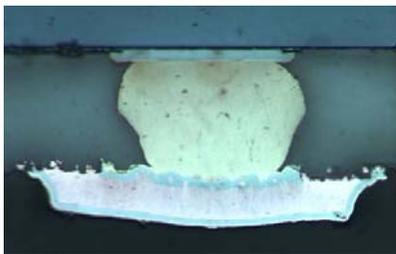


Figure 12. Photograph of gold stud bump interconnect.

4. RELIABILITY OF EMBEDDED ASSEMBLIES

Daisy chain assemblies have been cycled according to an Extreme Low temperature range (-135 to +85°C). The plot in Figure 13 shows the temperatures, ramp rates, and dwell times used for the thermal cycling experiments. It should be noted that a problem with the liquid nitrogen valve resulted in two exposures to -196°C, without failure. At this time, a single failure for the extreme temperature cycles occurred following 348 cycles; however, the remaining samples have survived 618 cycles without failure. As shown in Figure 14, the single failure occurred due to a crack in the Si die at the corner of the device.

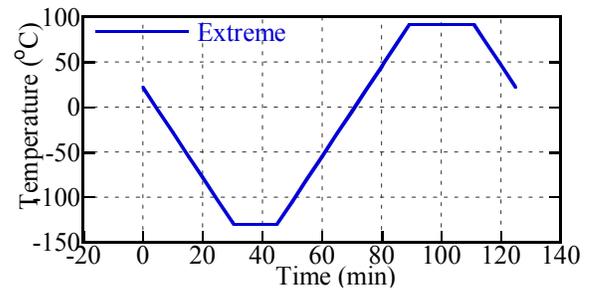


Figure 13. Plot of Extreme and Mil Standard thermal cycles, including ramp and dwell times.

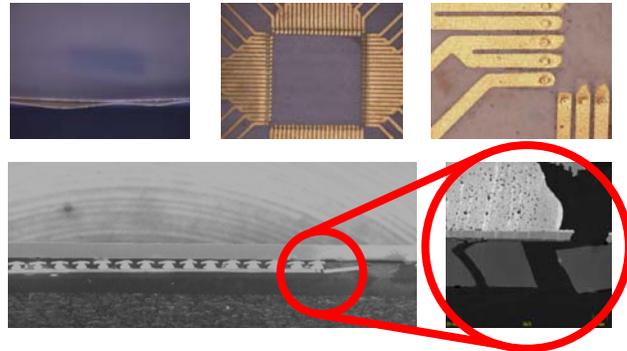


Figure 14. Photographs of the failed assembly and SEM SE images of the corresponding cross-sections.

5. EMBEDDED ACTIVE ASSEMBLY

To evaluate the influence of the previously described assembly procedure on the electrical behavior of active devices, a Honeywell MOI5, custom-designed quad op-amp chip (Figure 15) targeted for low-temperature and wide-temperature range applications was used for this task. Just as with the previously described daisy chain die, the quad op-amp was thinned to 50 μ m, and embedded between two layers of LCP.

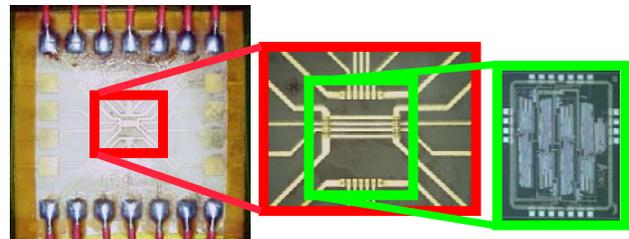


Figure 15. Low and high magnification photographs of an embedded op-amp assembly and an as-received device.

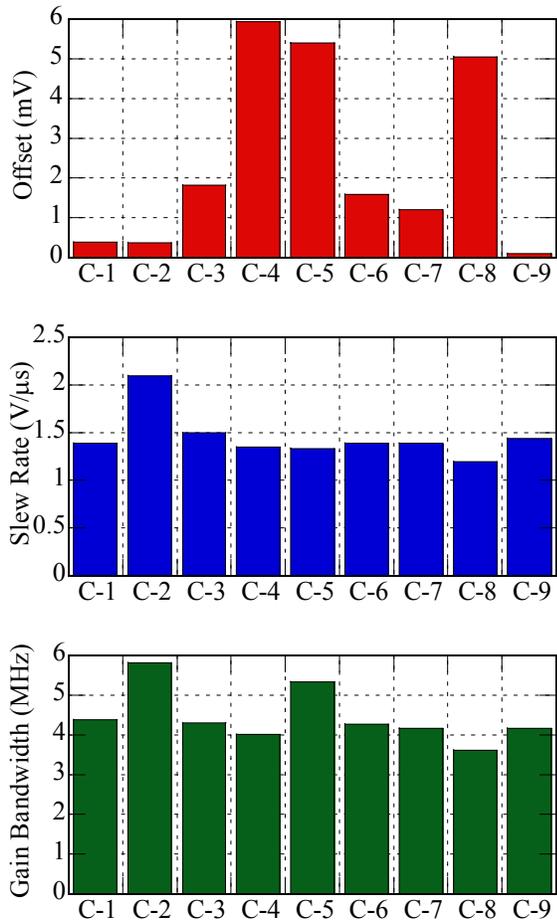


Figure 16. Measured (a) Offset, (b) Slew Rate, (c) Gain Bandwidth for nine embedded opamp assemblies.

Electrical Evaluation as a Function of Temperature

With the operational amplifier (powered between complementary supply voltages) in an closed-loop negative feedback configuration with 0-V input common-mode level, the opamp’s offset was calculated by tying the input to analog ground, measuring the output voltage, and dividing by the gain factor. The slew-rate was measured by calculating the dV/dt of the opamp’s output signal with a square wave input. Finally, the gain-bandwidth was estimated by measuring the amplifiers’ small-signal risetime and calculating [5]

$$GBW = \frac{f_n \tau_r}{\text{small-signal risetime}}$$

As summarized in Figure 16, voltage offset, slew rate, and gain bandwidth were measured at room temperature for nine samples. In addition, the same parameters were measured as a function of temperature for two select embedded op-amp assemblies. The results are shown in Figure 17.

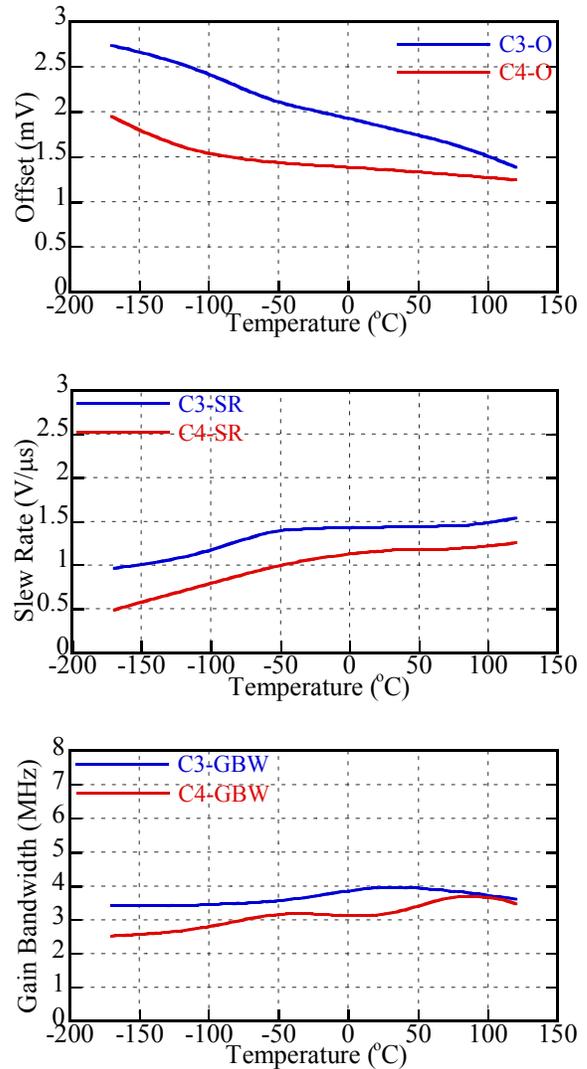


Figure 17. Measured (a) Offset, (b) Slew Rate, (c) Gain Bandwidth for two representative embedded opamp assemblies (C3 and C4) as a function of temperature.

Since the measured offset sample to sample exhibited consistent polarity, it is apparent that opamp offset was systematic in nature, dominated by asymmetry within the opamp’s internal circuit topology. Amplitude variability observed for the voltage offset in both figures can be explained by random mismatch chip-to-chip, and is well within the anticipated offset of conventional CMOS opamps. Slew rate and gain bandwidth are relatively consistent among the nine samples, with the differences attributed to statistical chip-to-chip variation in the opamp’s internal bias current generator. The consistent behavior trends among these samples suggest that the assembly method is consistent.

6. CONCLUSION

A reliable method of producing embedded active assemblies has been developed. Thermal cycling tests indicate that this assembly method is capable of long term operation within extreme temperature environments.

REFERENCES

- [1] G.Gronau, "Scattering-parameter measurement of microstrip devices," *Microwave Journal*, 1992: p. 82-92.
- [2] Tan Zhang, Zhenwei Hou, R. Wayne Johnson, Alina Moussessian, Linda Del Castillo and Charles Banda, "Flip Chip Assembly of Thinned Silicon Die on Flex Substrates," *Proceedings of the 2005 APEX Conference*, Anaheim, CA, February 21-24, 2005.
- [3] Brian Holland, Ryan McPherson, Tan Zhang, Zhenwei Hou, Robert Dean, R. Wayne Johnson, Linda Del Castillo and Alina Moussessian, "Ultra-Thin, Flexible Electronics," *Proceedings of the 58th Electronic Components and Technology Conference 2008*, Lake Buena Vista, FL, May 27-30, 2008.
- [4] Tan Zhang, Zhenwei Hou, R. Wayne Johnson, Alina Moussessian, and Linda Del Castillo, "Assembly of Thin, Flexible Electronics," to be submitted to *IEEE Transactions on Advanced Packaging*.
- [5] J.F. Pierce and T.J. Paulus, *Applied Electronics*, Fourth Edition, Bell and Howell Company, 1972.

BIOGRAPHY



Linda Del Castillo is a Senior Materials Scientist/Engineer in the Advanced Electronic Packaging Group at the Jet Propulsion Laboratory (JPL). She received her B.S. in Mechanical Engineering from California State Polytechnic University, Pomona, followed by M.S. and Ph.D. degrees in Materials Science and Engineering from the University of California, Irvine. Since beginning her work at JPL in 2000, she has been involved with electronic packaging for active membrane radar applications, flexible embedded active devices, heterogeneous integration of a MEMS neuro-prosthetic system, investigations of embedded passives and lead free solders, as well as MEMS fabrication, and high temperature survivable electronic systems for the Venus environment.



Alina Moussessian received her Ph.D. in Electrical Engineering from Caltech in 1997. At Caltech she worked on microwave and millimeter-wave power combining, beam-steering, computer-aided design and microwave circuits. After graduation she joined the Radar Science and Engineering Section at JPL where she worked on Shuttle Radar Topography Mission (SRTM) radar testing and the development of a testbed airborne radar sounder for the Europa Orbiter Radar Sounder. She worked in industry from 2000 to 2001, developing optical telecommunication components. Since returning to JPL in 2002 she has been involved in technology development projects for very large aperture phased arrays. She is currently working on membrane radar systems for future NASA missions and advanced components technology for membrane-based phased arrays. She is currently the supervisor of the RF Radar Electronics Group.



Mohammad Mojarradi received his Ph.D. degree in Electrical Engineering from the University of California, Los Angeles (UCLA) in 1986. Prior to joining Jet Propulsion Laboratory, Pasadena, CA, he was an Associate Professor at Washington State University and the Manager of the mixed-voltage/specialty integrated circuit group at the Xerox Microelectronics Center, El Segundo, CA. He is a Specialist in integrated mixed-signal/mixed-voltage electronic sensors, micromachined interface circuits, and mixed-mode integrated circuit design. He has more than 20 years of combined industrial and academic experience in his field. His current work focuses on developing highly efficient integrated mixed-signal electronics for sensors, actuators, and power management and distribution systems (PMAD) for avionics system on a chip for deep space using the SOI CMOS process.



Elizabeth Kolawa has been with the Jet Propulsion Laboratory, Pasadena, CA, since 1993. Presently, she is responsible for developing thermal cycle resistant electronics for the Mars focused technology program and managing the advanced measurement and detection technology program for JPL. Her research interest includes electrical contacts to semiconductors, diffusion barriers, and integration of microsystems, electronics packaging and technologies for extreme environments.



R. Wayne Johnson is a Professor of Electrical Engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP).

Current research projects include lead free electronics assembly, mixed lead free and Sn/Pb electronics assembly, wafer level packaging, flip chip assembly, assembly of ultra thin Si die, and electronics packaging for extreme environments (-230°C to +485°C). He is Vice President of Publications for the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society Board of Governors and Editor-in-Chief of the IEEE Transactions on Electronics Packaging Manufacturing. Wayne received B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and a Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in Electrical Engineering.



Benjamin J. Blalock is an Associate Professor in the Min H. Kao Department of Electrical Engineering and Computer Science at the University of Tennessee where he directs the Integrated Circuits and Systems Laboratory (ICASL). He received his B.S. degree in Electrical Engineering from the University of Tennessee,

Knoxville, in 1991 and his M.S. and Ph.D. degrees, also in Electrical Engineering, from the Georgia Institute of Technology, Atlanta, in 1993 and 1996 respectively. His research focus at UT includes analog integrated circuit design for extreme environments (both wide temperature and radiation) on CMOS and SiGe BiCMOS, multi-gate transistors and circuits on SOI, analog circuit techniques for sub 100-nm CMOS, mixed-signal/mixed-voltage circuit design for systems-on-a-chip, and biomicroelectronics. Dr. Blalock has co-authored 100 refereed papers. He has also worked as an analog IC design consultant for Cypress Semiconductor, Concorde Microsystems, and Global Power Electronics. Dr. Blalock is a senior member of the IEEE.

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