Smart Payload Development for High Data Rate Instrument Systems

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# Definition of Terms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>SoC</td>
<td>System On a Chip</td>
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<tr>
<td>MARVEL</td>
<td>Mars Volcanic Emission and Life</td>
</tr>
<tr>
<td>MATMOS</td>
<td>Mars Atmospheric Trace Molecule Spectroscopy</td>
</tr>
<tr>
<td>FTIR</td>
<td>Fourier Transform Infrared (Spectrometer)</td>
</tr>
<tr>
<td>FTS</td>
<td>Fourier Transform Spectrometer</td>
</tr>
<tr>
<td>APU</td>
<td>Auxiliary Processing Unit</td>
</tr>
<tr>
<td>FPU</td>
<td>Floating Point Unit</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>SVM</td>
<td>Support Vector Machine</td>
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</table>
Smart Payload Motivation

Assertion: On-board computation has become a bottleneck for advanced science instrument and engineering capabilities.

Smart Payload Definition:

1) Localized instrument “smarts” that offload the flight processor of extensive computing cycles, simplify the interfaces, and minimize the dependency of the instrument on the flight system

2) Smart development processes that emphasize design flexibility, scalability, and robustness, and significantly increase instrument performance while reducing cost, risk, and preserving schedule

Target Platform:

- Xilinx Virtex-4 FPGA with embedded PowerPC405 processor

Benefits include: better performance, lower cost, reconfigurability
MARVEL/MATMOS Overview

- Proposed 2011 Mars Scout Mission - *not selected*

- MATMOS - Solar occultation FTIR Spectrometer
  - for detection of trace gases: CH$_4$, N$_2$O produced by life or volcanism
  - volumes of raw infra-red spectrum data in 3 minute bursts during Martian sunrise & sunset
  - remaining 112 minutes of orbit for science data processing and compression for downlink
On-Board Science Data Processing

• Two 3-minute occultations produce **691 Mbytes** of data
  – 2 Gbytes on-board storage meet mission requirements
  – Only enough memory for 2 orbits of raw interferogram data

• MATMOS On-Board Data Processing:
  – An observation every 2.5 sec. --> $192 \text{ kHz} \times 2.5 \text{ s} = 480,000$ raw samples/channel
  – After re-sampling, $2^{18} = 262,144$ HgCdTe points and $2^{19} = 524,288$ InSb points

  – Time-domain data stream re-sampling to path difference domain reduces data volume by a factor of 1.5

  \[
  \frac{(2 \times 480000)}{(262144 + 524288)} \times 1.5 = 1.83, \text{ combined re-sampling data reduction}
  \]

  – FFT phase correction by convolution reduces data volume by a factor of 2
  – FFT spectrum computation reduces data volume by a factor of 6.1
  – Further processing of the spectra (includes averaging scans taken above atmosphere) reduces data volume by a factor of 2
  – Standard image compression techniques applied before transmission to S/C computer reduces data volume by a factor of 1.8
MATMOS Baseline Design Trade

- Simulated raw FTS interferogram data on both Rad750 and Virtex-II Pro platforms

- Virtex-II Pro lagged Rad750 primarily due to smaller cache size and lack of hardware FPU

- A soft-core FPU implemented on the Virtex-II Pro still exhibited high latency associated with floating-point instruction execution

<table>
<thead>
<tr>
<th>Software Component</th>
<th>Processor: RAD750</th>
<th>Xilinx</th>
<th>Xilinx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>VxWorks</td>
<td>Linux</td>
<td>Linux</td>
</tr>
<tr>
<td>Clock Speed:</td>
<td>133 MHz</td>
<td>300 MHz</td>
<td>300 MHz</td>
</tr>
<tr>
<td>Memory:</td>
<td>128 MB</td>
<td>128 MB</td>
<td>128 MB</td>
</tr>
<tr>
<td>w/Perflib</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Execution Time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reject Dark Interferograms</td>
</tr>
<tr>
<td>Interferogram Re-sampling</td>
</tr>
<tr>
<td>Non-Linearity Correction</td>
</tr>
<tr>
<td>Phase Correction</td>
</tr>
<tr>
<td>Fast Fourier Transformation</td>
</tr>
<tr>
<td>Spectra Averaging</td>
</tr>
<tr>
<td>Lossless Compression</td>
</tr>
<tr>
<td>Total (112 min available)</td>
</tr>
</tbody>
</table>

MARVEL baselined 2 Rad750s in their 2011 Mars Scout Proposal
Features of the Virtex-4

- Three families: 1. LX (logic), 2. SX (DSP apps), 3. FX (embedded processing)
- Single or dual embedded PowerPC405 cores, clocked up to 450 MHz
- Auxiliary Processor Unit (APU)
  - integrates directly into the processor pipeline
  - decodes soft co-processor supported instructions
  - ex. APU I/F to soft-core FPU eliminates need for software floating point

Xilinx’s APU Floating Point Unit v2.1

<table>
<thead>
<tr>
<th>Supported Device Family</th>
<th>Core Specifics</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Virtex-4 FX</td>
</tr>
<tr>
<td>Resources Used</td>
<td>Slices</td>
</tr>
<tr>
<td>Lite (no div/sqrt)</td>
<td>1100</td>
</tr>
<tr>
<td>Full (with div/sqrt)</td>
<td>1250</td>
</tr>
<tr>
<td>Clock Speeds</td>
<td></td>
</tr>
<tr>
<td>-10 part</td>
<td>137.5 MHz</td>
</tr>
<tr>
<td>-11 part</td>
<td>150 MHz</td>
</tr>
<tr>
<td>-12 part</td>
<td>170 MHz</td>
</tr>
</tbody>
</table>

Graphics Credit to Xilinx
The APU-FPU System

- APU-FPU (single precision)
- RS232 UART (terminal I/O)
- 64 MB DDR RAM (for heap + stack space)
- 64 KB BRAM (for all other linker sections, i.e. text)
- L1 cache support for all memories
  - 16 KB data
  - 16 KB instruction
- Compact Flash Interface (for reading large data files)

RESOURCE UTILIZATION OF THE APU-FPU SYSTEM

<table>
<thead>
<tr>
<th>Resource</th>
<th>Usage</th>
<th>ML403 (V4FX12)</th>
<th>ML410 (V4FX60)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slices</td>
<td>3,455</td>
<td>63%</td>
<td>14%</td>
</tr>
<tr>
<td>BRAM</td>
<td>34</td>
<td>94%</td>
<td>15%</td>
</tr>
<tr>
<td>XtremeDSP</td>
<td>4</td>
<td>12%</td>
<td>3%</td>
</tr>
</tbody>
</table>
Results of Virtex-4FX12 with APU FFT

FPGA embedded processing system evaluated in 3 configurations
1. No FPU, software FP emulation through GCC
2. No FPU, software FP emulation through IBM Perflib
3. Hardware acceleration via APU-FPU

Virtex-4FX12 RESULTS

<table>
<thead>
<tr>
<th>Setup</th>
<th>FFT Time / Iteration (SEC)</th>
<th>Speedup (vs. base case)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx Virtex-4FX12 PowerPC405 No OS (GCC 3.4.1, patched) CPU Freq: 200 MHz FPU Freq: 100 MHz</td>
<td>40</td>
<td>base case</td>
</tr>
<tr>
<td>No FPU</td>
<td>40</td>
<td>base case</td>
</tr>
<tr>
<td>No FPU, Perflib</td>
<td>16</td>
<td>2.5</td>
</tr>
<tr>
<td>APU-FPU</td>
<td>3.56</td>
<td>11.24</td>
</tr>
</tbody>
</table>

MCP750 RESULTS

<table>
<thead>
<tr>
<th>Setup</th>
<th>FFT Time / Iteration (SEC)</th>
<th>Speedup (vs. base case)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motorola MCP750 PowerPC750 VxWorks OS / Compiler Freq: 233 MHz</td>
<td>0.637</td>
<td>62.79</td>
</tr>
<tr>
<td>Hardware FPU</td>
<td>0.637</td>
<td>62.79</td>
</tr>
</tbody>
</table>

Other optimizations to be evaluated include:
- Support for vector math operations with hardware acceleration
- OS (Linux, VxWorks, XMK) with access to APU co-processors
- Additional co-processors targeted at specific algorithms (example: 5.25 ms 1,000,000 point FFT core, on the market today)
- Optimize APU-FPU utilization
  - Parallelize code to take advantage of pipelined multiply and addition/subtraction
  - Remove data dependencies
  - Evaluate the use of optimized fused multiply-addition/subtraction operation
- Further optimizations in memory
  - Different memory configurations
  - Different cache options
A MATMOS Computer Concept

- MATMOS needs **1.2 \times \text{RAD750}, 133 MHz**
  - 112 minutes available for science data processing
  - RAD750 needs 130 minutes = 1.16\times112 \text{ min}
- Scaled down MCP750 is **3.2x faster than V4FX12**
  - MCP750 (233 MHz) is 5.59x faster than V4FX12 (200 MHz)
  - MCP750 is 233 MHz, scale down to 133 MHz to compare (0.57x)
  - Real speed factor: 3.19 = 5.59\times0.57
- Use dual core FPGA: MCP750 = **1.6 \times \text{ dual core V4FX12}** (3.2 / 2)
- For flight: 1.2\times1.6 = **1.9 \times \text{ dual core V4FX12}**

Xilinx ML410 Board -- a good candidate
Task Summary - SVM Application

Objectives:

• Demonstrate new/smart on-board data processing capabilities, driven by data actively collected by instrument sensors and enabled by Field Programmable Gate Array (FPGA) co-processor implementations, which reduce the most significant bottlenecks limiting new measurement concepts including: 1. Decision-making 2. Event detection 3. Reconfiguration

• Prototype how advanced data fusion algorithms, such as support vector machines (SVM) and others, in signal and image processing can be realized within this architecture to demonstrate improved data processing capabilities and performance

Approach:

• Target Xilinx ML403/410 Development Platforms including Virtex-4FX FPGA with Auxiliary Processing Unit (APU)

• Use CoDeveloper™ C-to-HDL tool set by ImpulseC

• Implement SVM algorithm (legacy C-code) in FPGA and demonstrate performance improvement

Support Vector Machine (SVM) Algorithms

Co-designed in an FPGA with PowerPC405 processor and auxiliary controller
Technical Approach

- **SVM Application**
  - Producer in sw.c
    - Reads input image file
    - Streams data to SVM
    - To run in embedded PowerPC405 processor
  - Consumer in sw.c
    - Streams data from SVM
    - Writes pixel classifications to output file
    - To run in embedded PowerPC405 processor
  - SVM in hw.c
    - Original algorithm + added I/O
    - C-to-HDL auto-translation and optimization via CoDeveloper™
    - Synthesized in Xilinx ISE for execution in FPGA fabric

```
/* If all reflectances are reasonable, apply the SVM. */
for(class_index=0; class_index<NUM_CLASSES; class_index++) {
    PIXEL output =
        (-svm_biases[class_index]) +
        refl8  * svm_coefs[class_index][0] +
        refl21 * svm_coefs[class_index][1] +
        refl31 * svm_coefs[class_index][2] +
        refl34 * svm_coefs[class_index][3] +
        refl41 * svm_coefs[class_index][4] +
        refl51 * svm_coefs[class_index][5] +
        refl65 * svm_coefs[class_index][6] +
        refl110  * svm_coefs[class_index][7] +
        refl150 * svm_coefs[class_index][8] +
        refl210 * svm_coefs[class_index][9] +
        refl213 * svm_coefs[class_index][10];
    if (class_index==0 || output > best_value) {
        best_class = class_index;
        best_value = output;
    }
}
```
Synthesis Results

- Simulated in CoDeveloper™
  - I/O read/write
  - Producer, SVM, and Consumer execution

- Pixel classification results:
  - Total pixels = 857,856
  - Snow = 146,138
  - Water = 356,773
  - Ice = 99,119
  - Land = 197,374
  - Cloud = 40,971
  - Unclassified = 17,481

- ImpulseC resource output:
  - 10 Adders/Subtractors (6 bit)
  - 1 Adder/Subtractor (32 bit)
  - 11 Multipliers (3 bit)
  - 1 Comparator (2 bit)
  - 2 Comparators (32 bit)
  - 12 Floating Point Adders/Subtractors (32 bit)
  - 11 Floating Point Multipliers (32 bit)

- HDL auto-generated
- Synthesized in Xilinx ISE for V4FX12 and V4FX60 FPGAs

- Design fits on V4FX60

<table>
<thead>
<tr>
<th>FPGA RESOURCES</th>
<th>V4FX60 (on ML410)</th>
</tr>
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<tbody>
<tr>
<td>Number of Slices:</td>
<td>8495 out of 25280 (33%)</td>
</tr>
<tr>
<td>Number of Slice Flip Flops:</td>
<td>9640 out of 50,560 (19%)</td>
</tr>
<tr>
<td>Number of 4 input LUTs:</td>
<td>10495 out of 50560 (20%)</td>
</tr>
<tr>
<td>Number of DSP48s:</td>
<td>44 out of 128 (34%)</td>
</tr>
<tr>
<td>Maximum frequency:</td>
<td>129.95 MHz</td>
</tr>
</tbody>
</table>
Summary

- Hybrid FPGA technology can deliver breakthrough performance by tightly coupling hardware and software.

- Interest in the Xilinx Virtex-4FX FPGA for space flight & instrument applications is growing.

- Smart Payload designs for instruments such as MATMOS can meet science data return requirements with more competitive use of available on-board resources.

- Smart Payload designs can provide algorithm acceleration in hardware leading to implementation of better (more advanced) algorithms in on-board systems for improved science data return.
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