Ultra-Thin, Flexible Electronics

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Abstract

Thinned die can be used to realize ultra-thin flexible electronics for applications such as conformal and wearable electronics. Three techniques have been developed to achieve this goal using thinned die: die flip chip bonded onto flexible substrates, die laminated onto LCP films, and die embedded in polyimide. A key to achieving each of these techniques is the thinning of die to a thickness of 50µm or thinner. Conventional CMP processing can be used to thin to 50µm. At 50µm, the active die become flexible and must be handled by temporarily bonding them to a holder die, for further processing. Once bonded face down to the holder die, the active die can be further thinned by DRIE etching the exposed backside. The thinned die can then been packaged in or on the flexible substrate.

Introduction

Thinning of silicon wafers has become common practice in the packaging industry for use in stacked die packages [1-3]. Wafer thinning is also being used in the development of 3-D wafer stacking [4, 5]. This technology can be leveraged to build very thin, flexible electronics. Applications include electronics appliqués that can be bonded to non-flat surfaces to produce conformal electronics or to fabrics to create wearable electronics. Layers of flexible electronics can be stacked and interconnected to produce very thin, 3-D electronics assemblies with embedded active devices.

Three techniques have been developed to fabricate ultra-thin, flexible electronics: 1) thinned die flip chip bonded on polyimide or liquid crystal polymer (LCP) flex (Figure 1), 2) thinned die laminated into LCP films (Figure 2), and 3) thinned silicon die embedded in polyimide (Figure 3). The manufacturing methods and materials for each of these approaches is described in the following sections.

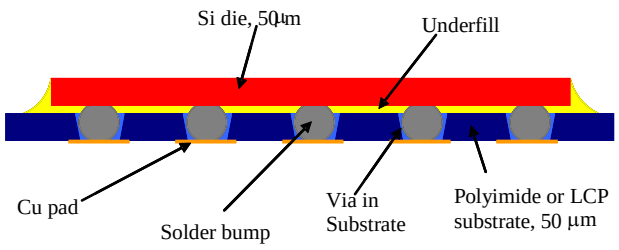


Figure 1. Illustration of Polyimide or LCP Substrate and Solder Assembly Approach.

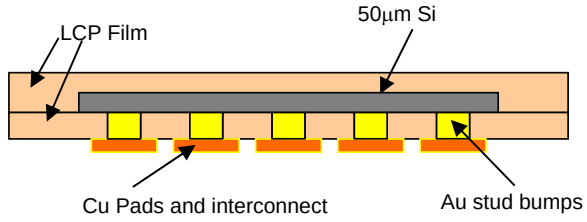


Figure 2. Illustration of Liquid Crystal Polymer (LCP) Substrate and Thermocompression Bond Au Stud Bump Assembly Approach.

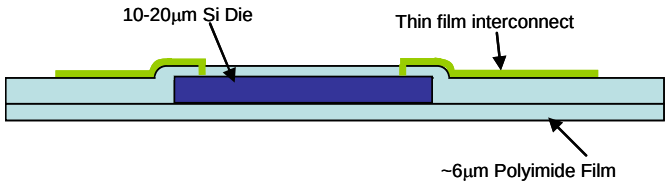
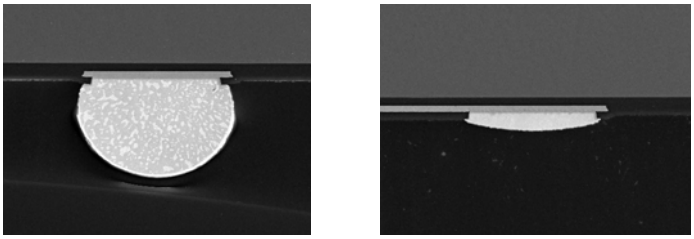


Figure 3. Illustration of Thinned Si Die Embedded in Polyimide with Thin Film Interconnect.

Thinned Flip Chip Bonded to Polyimide or LCP Flex

Die Thinning and Handling: PB8 (5mm x 5mm) perimeter I/O, daisy chain test die purchased from Delphi Electronics. The PB8 wafers were purchased with electroless Ni/immersion Au under bump metallurgy (UBM), but no solder bumps.

Conventional solder bumps are 75-125µm in height (Figure 4a). As will be discussed later, this height would cause problems in wafer mounting for the thinning operation. For the assembly process developed in this work, immersion bumps were used. The wafer was first cleaned with 5:1:1 (DI Water: Sulfuric Acid: Hydrogen Peroxide). Water soluble flux (Alpha Metal WS 619) was then brushed onto the wafer. Next, the wafer was dipped into molten eutectic SnPb solder at 220ºC. After immersion solder bumping, the wafers were cleaned with 10% DI water diluted Hydrex™ AC solution at a temperature of 43 to 49ºC for 10 minutes, followed by a DI water rinse and nitrogen blow dry to clean the flux residue. Low profile solder bumps (Figure 4b) were formed with a bump height of 13 – 15µm. Immersion bumping is a low cost bumping operation.



(a) Standard PB Solder Bump (b) Immersion Bumped PB8

Figure 4. Comparison of Standard PB8 Solder Bump and an Immersion Solder Bump.

Wafers were sent to APTEK Industries for thinning. Rather than attempting to saw 50µm thick silicon wafers, a process was used that singulated the die during the thinning process. The process is illustrated in Figure 5.

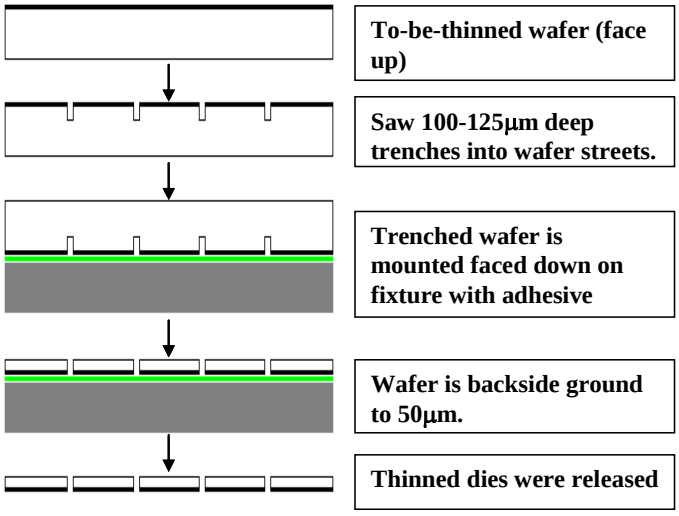


Figure 5. Flowchart of the Thinning Process.

A 100-125µm deep trench was sawn into dicing streets on the front side of the to-be-thinned wafer. At APTEK, the trenched wafer was mounted on a grinding fixture with a temporary adhesive. Conventional tall solder bumps would create a problem in the wafer mounting process. The immersion solder bumps were thinner than the adhesive layer and did not require any process modifications at APTEK. Sequential grinding was used to remove the bulk silicon and polish the backside of the die. When the thickness of the thinned die was less than the depth of the trenches, the trench grids were exposed and the thinned wafer was automatically turned into an array of thinned die. The thinning process continued until the thickness reached the target value of 50µm. After completion of the thinning, the thinned dies were released from the grinding fixture by dissolving the adhesive. The process had high yield and there was no damage to the die edges. The thinned die were returned in waffle packs.

Thin die tended to curl, as shown in Figure 6. In both the x and y directions, the curve radius ranged from 130 to 150mm. This curvature would result in uneven gaps between the solder bumps and pads on the flexible substrates during assembly, which would cause non-uniform solder joint connections or possibly opens. For ease of handling through the assembly process and to reduce the degree of die warpage, thinned die were transferred onto thick flat handle die with a temporary adhesive. In this process (Figure 7), an adhesive was employed to temporarily bond thinned die on the handle die. The adhesive was a mixture of acrylic based polymer with the solvents of 50%wt toluene and 15%wt methyl ethyl ketone (MEK). The adhesive was spin-coated on a handle silicon wafer at a spin rate of 1000 rpm for 30 seconds. The as-coated wafer was heated at 90°C for 2 hours. After drying, the adhesive was solidified, forming a coating on the handle wafer. The coated wafer was diced into pieces matching the size of the thinned die. The coated handle die were singularized from the diced wafer, and then dehydrated in a vacuum oven at 150ºC for 2 hours.

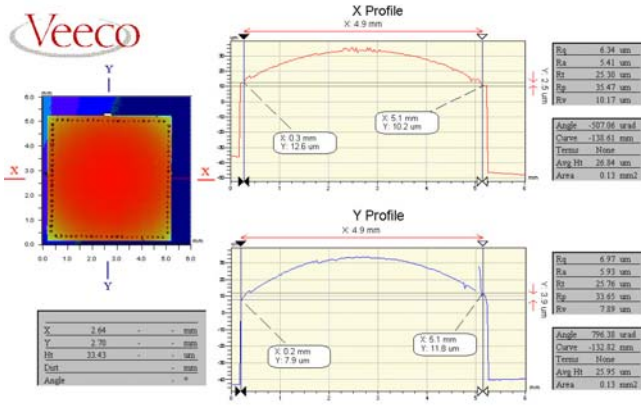


Figure 6. Surface Profile and Curvature for the 50 µm PB8 Die.

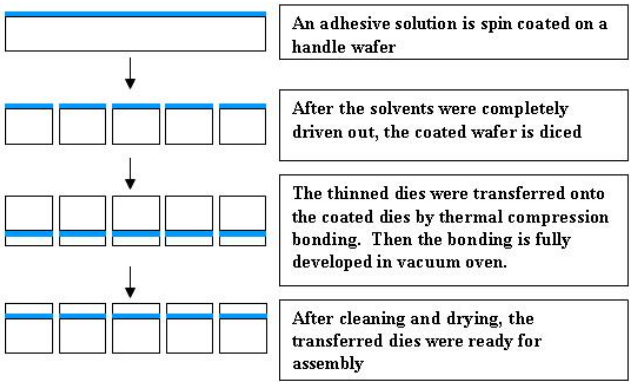


Figure 7. Flowchart of Thinned Die Transfer Process.

Bonding of thinned die to the coated die (handle) was carried out on a Karl Suss HP thermocompression flip chip bonder, one at a time. The coated handle die was accurately aligned and placed on a thinned die. The handle die was

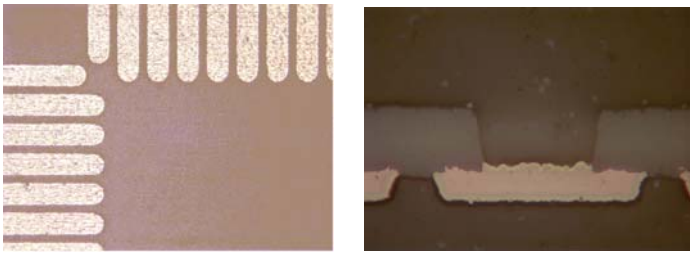
heated to 150°C (read from the machine) for 1.5 minutes with a pressure of 0.5 kg(f). To complete the bonding, the handle die/thinned die were placed in a vacuum oven and heated to 160°C for 2 hours. A weight of 400g was applied to enhance bonding.

With the handle die attached, the curve radius was increased to approximate 750mm. Therefore, the thin die mounted on a carrier could be treated as a normal thickness die as it goes through the placement and reflow stages of the flip chip assembly process.

Substrate Fabrication; Double copper clad polyimide and LCP [6] film were used to fabricate the substrates. The substrate fabrication sequence was: 1) pattern Cu circuitry, 2) pattern Cu on backside (via etch mask), 3) etch vias, 4) strip Cu etch mask, and 5) surface finish. Photolithographly and wet chemical etching were used to pattern the copper circuitry. Masking was used to protect the back side Cu during this step. This process was then reversed to pattern the backside Cu to serve as an etch mask for the via etching. On a laboratory scale, the patterning and etching of the two copper layers was done sequentially due to the different etch rates observed because of the difference in exposed Cu on the two sides. In a production environment, both copper patterns could potentially be etched simultaneously.

An STS AOE deep reactive ion etcher (inductively coupled plasma) was used to etch the vias in the polyimide and LCP films. Photoresist was applied and patterned in the etched vias to protect the exposed Cu at the bottom of the vias during wet chemical removal of the backside Cu etch mask. Alternately, laser etching could be used for via formation in high volume production.

Ni and Au were electroplated onto the Cu traces and the Cu exposed at the bottom of the etched vias. The Ni plating was 3-4μm thick. The Au plating thickness was 0.5μm. Figure 8 shows photographs of an LCP substrate after Ni/Au plating.



(a) Circuitry Side (b) Cross Section of Via

Figure 8. Photographs of an LCP Substrate after Ni/Au Plating.

Since the immersion solder bumps were only 13-15μm tall, they would not contact the pads at the bottom of the via (50μm deep). Eutectic SnPb solder paste, Aqualine 6023, was squeegeed into the polyimide substrate vias followed by a 220ºC peak temperature reflow. The paste was squeegeed directly into the vias – no stencil was used. Three passes of solder paste squeegeeing and reflow were required to deposit sufficient solder to reach the top of the via. The substrates were cleaned in a 10% HydrexTM AC solution at 43 – 49ºC, and then DI water rinsed after each reflow step. A finished substrate is shown in Figure 9. The Cu pattern is visible through the polyimide film.

Solder Assembly: A vacuum fixture method was developed to hold the flexible polyimide or LCP substrate flat during the assembly process. A porous metal plate was used to apply a diffuse vacuum under the substrate as illustrated in Figure 10. Vacuum was supplied using a high temperature silicone rubber hose. Kapton® tape was used to mask off the vacuum not covered by the flex substrate.

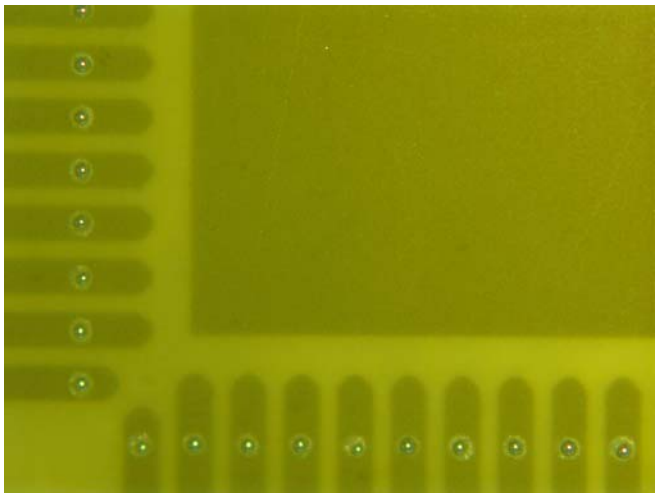
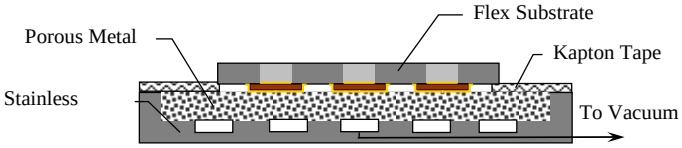
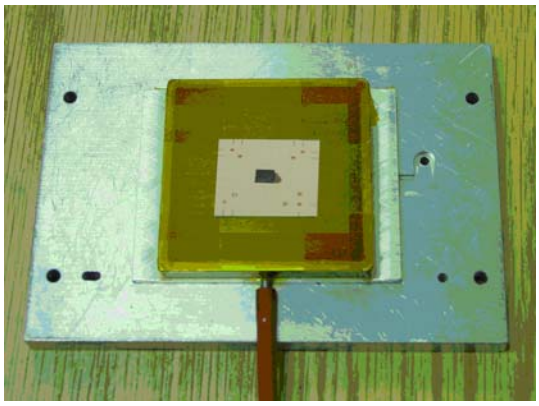


Figure 9. Photograph of a Solder Via Filled Polyimide Substrate. The Cu pads/traces can be seen through the polyimide on the opposite side.



(a) Illustration of the Fixture



(b) Photograph of the Actual Fixture

Figure 10. Vacuum Fixture for Solder Assembly of Die to Polyimide Substrate.

For assembly, Kester flux TSF 6522 was brushed on the substrate. The thinned, immersion bumped flip chip die with backside handle was aligned and placed on the substrate with a Karl Suss HP 4000 Flip Chip Bonder. The placement force was 5N. The assembly was then reflowed in a Heller 1800 reflow furnace with a peak temperature of 220ºC. The vacuum was on during the entire placement and reflow process. After reflow, the assembly was removed from the vacuum fixture and soaked in acetone to release the backside handle from the thinned flip chip. The underfill process must be carried out after releasing the backside handle since the underfill would form a fillet above the interface of the thin die and its handle and make the subsequent release impossible.

Lord Corp. underfill MTM 9086-71 was selected for use in this assembly. Before underfilling, the assembly was baked overnight at 125ºC to drive out any solvent remaining from the handle release process. An argon plasma treatment was used to enhance the underfill wetting to the substrate. Reducing the underfill-to-substrate wetting angle increased the underfill flow rate, which decreased the tendency for the underfill to 'pile up' at the dispense point. The substrate was then held on the vacuum fixture with the vacuum applied. The stage on the Cam/alot dispense system was heated to 100ºC to decrease underfill viscosity during capillary flow under the die. An alternating, multiple pass underfill dispensing pattern, with the starting and end points leading away from the die, was developed for this study, as illustrated in Figure 11. This dispensing approach provided a small amount of material at a time, thus allowing time for the underfill to flow beneath the thinned die instead of the underfill simply building up, which would cause the underfill to encroach onto the top of the die. After dispensing, the assembly was cured at 165ºC for 30 minutes on the vacuum fixture. Figure 12 shows a cross section of an assembly on LCP.

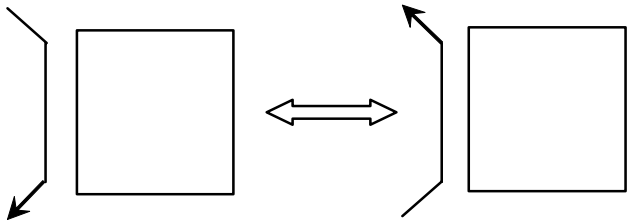


Figure 11. Multi-pass Underfill Dispensing Pattern.

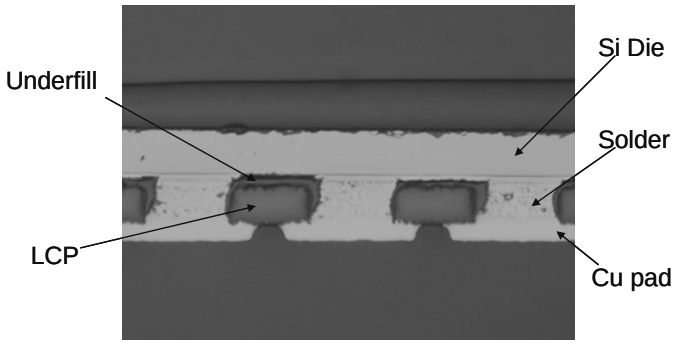


Figure 12. Cross-section of Thinned Low Profile Flip Chip Assembly.

Thinned Die Laminated into LCP Films

Die Thinning and Handling: PB8 die were also used for this construction. The die were thinned and handled as described in the previous section with few modifications. Rather than immersion solder coating the electroless Ni/immersion Au pads, the wafers were sent to an outside vendor for electroless Au plating to increase the Au thickness to 1-2µm. After the thinned die were mounted on the handle die as previously described, the die were Au stud bumped. While stud bumping prior to wafer thinning would be preferred, there was concern about mounting the bumped wafer for thinning. A custom fixture was developed to hold individual die on the Palomar 2640 thermosonic wire bonder for stud bumping. A uniform, void free adhesive layer between the die and the handle was required to avoid fracture of the die during thermosonic wire bonding. Scanning acoustic microscopy was used to inspect the die-to-handle attachment during the process development.

Substrate Fabrication: The LCP substrate followed the same procedure previously described. The only change was to electroplate thicker Au (2-3µm) into the vias to facilitate Au-to-Au thermocompression bonding of the stud bumps to the substrate metallization.

Stud Bump Assembly: The assembly process is illustrated in Figure 13. The Au stud bumped die was bonded onto the LCP substrate by thermocompression bonding. This formed the electrical connections and laminated the LCP to the active face of the die in one step, eliminating the need for underfill.

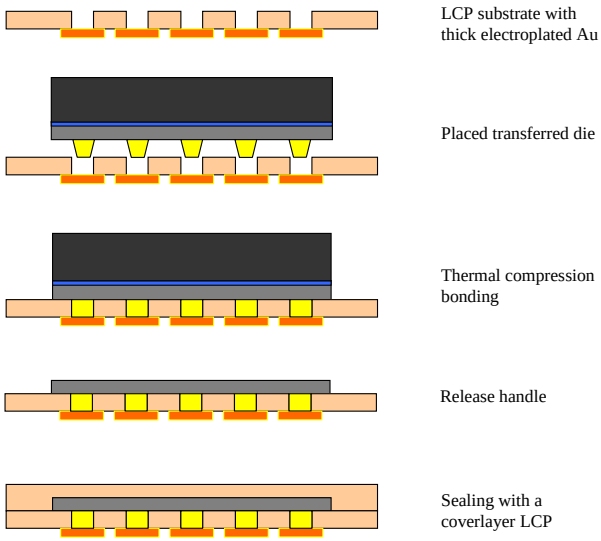


Figure 13. Illustration of Assembly Process with Gold Stud Bump Connections.

A design of experiments (DOE) was used to optimize the bonding parameters for die-to-LCP adhesion. Four primary parameters were adjustable for controlling assembly quality, namely the arm (nozzle) temperature, chuck temperature, bonding time and bonding force. Normal thickness PB8 dies

with gold stud bumps and LCP coupons were used for these tests. The die shear strength was used to evaluate the bonding quality. The DOE was used to identify the influential parameter effects based on the data from the die shear test. Eight runs are sufficient using the Taguchi design of L8 orthogonal arrays with two levels (Table 1). Each run was repeated five times. The parameter levels are listed in Table 2.

Table 1. L_8 (2^7) Orthogonal Arrays

Run #	Chuck Temp	Arm Temp	Time	Force	Ave Shear Force (kg-f)
1	0	0	0	0	7.432
2	0	0	1	1	8.257
3	0	1	0	1	10.766
4	0	1	1	0	8.096
5	1	0	0	1	16.283
6	1	0	1	0	12.343
7	1	1	0	0	15.970
8	1	1	1	1	16.823

Table 2. The Two Levels of Thermal Compression Bonding Parameters

	Level 0	Level 1
Chuck Temperature (°C)	150	300
Arm Temperature (°C)	370	410
Bonding Time (sec)	60	300
Bonding Force (gf)	1000	5000

The one-factor effect plots in Figure 14 demonstrate the chuck temperature to be the most influential parameter for the process under these experimental conditions. A high chuck temperature improves the bonding quality. Arm temperature and bonding force also positively affected the bonding quality. Compared to these three parameters, bonding time at the peak temperature exhibited a negative effect for die bonding. According to this result, high chuck temperature (300°C), a high arm temperature (410°C), large bonding force (5000gf) and short bonding time (60sec) were set for the die bonding. A cross section of a stud bump connection is shown in Figure 15.

The handle die was released by soaking the as-bonded part in acetone to remove the adhesive between the die and the handle. A second sheet of LCP was laminated over the back of the substrate and die to embed the die in LCP. The lamination was done with the thermocompression bonder and the parameters were: Nozzle Temperature: 380°C; Chuck Temperature: 150°C; Time at Peak Temperature: 60 seconds; and Bonding Force: 1000g-f. PB8 die have been assembled with 100% daisy chain continuity and an operational amplifier die has been thinned and assembled successfully.

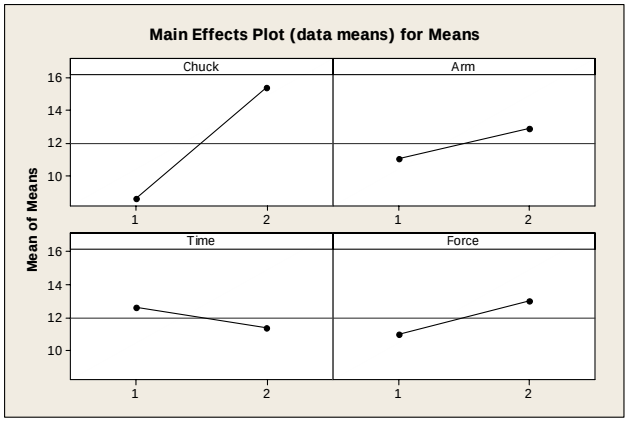


Figure 14. One–Factor Effects for Four Thermal Compression Parameters.

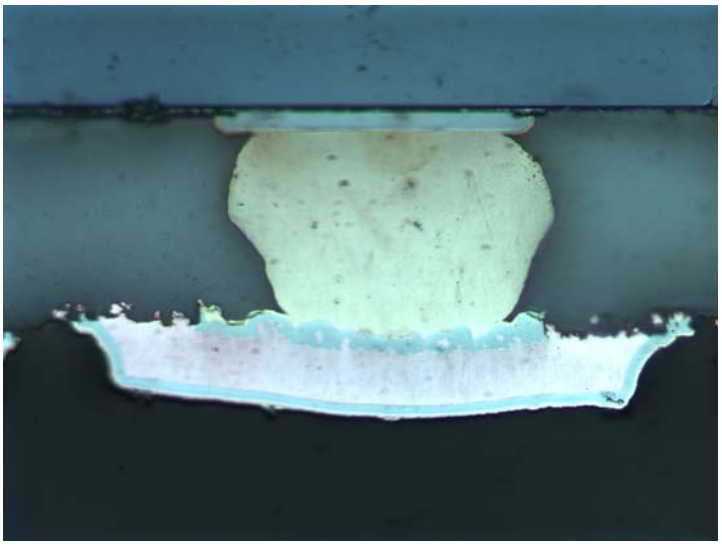


Figure 15. Photograph of Thermocompression Bonded Stud Bump.

Thinned Silicon Die Embedded in Polyimide

The overall concept of this process is to further thin the die to the 10-15μm range and embed them into polyimide. However, once thinned it became clear that die this thin were incredibly hard to manipulate and protect, and so it was

decided that the die should be individually bonded to a handle die as in previous sections. This bonding process was instrumental in the success of the project.

Die Thinning and Handling: This project made use of PB6 die, 5x5mm, thinned in a similar process to the previous PB8. The thickness of these die as received from APTEK varied from 45-50µm and were handled with a vacuum tool to minimize chipping. The handle die were produced using a standard 100mm silicon wafer polished on one side. A fast air drying, acrylic coating, was chosen as the adhesive. This was spun onto the unpolished side of the silicon wafer, dried, and diced into die approximately 0.05mm smaller than their PB6 counterparts. This size reduction was done to mitigate an issue in the thinning process where excess adhesive was coating the sides of the PB6 and causing an un-etched "ridgeline" to form on the thinned die. Reducing the size of the handle die helped to keep the adhesive on the front side of the die, thus alleviating this issue.

The two die were then bonded front to front using an HP4000 Flip-Chip bonder. A suitable process involved heating both die to 160°C while squeezing with 1000g of force. This was done for 3 minutes and the die was allowed to cool under pressure for 10 additional minutes. While this process does a fairly good job of bonding the die, it was discovered that the thinning process would sometimes cause the adhesive to release on the corners, causing the thinned die to curl up. This was corrected by adding a 2 hour vacuum bake under an 800g load at 120°C to remove any remaining solvents from the adhesive.

Once individual die were thoroughly bonded, they were ready to be thinned to their final thickness. Using wafer grip adhesive, the die were adhered to an oxidized wafer, handle die down. The die were then cleaned with acetone, methanol, and DI water both on top as well as around the edges: once again to mitigate ridge formation. Following this step, the wafer was placed into oxygen plasma for 30 seconds to remove any organics still on the surface. An STS ASE deep reactive ion etcher was used to plasma etch the silicon die in 5 minute runs from 50µm to their final thicknesses. Between each run, the cleaning procedure was repeated. The number of runs required was a factor of how many die were run at a time, as more exposed silicon would require longer to thin.

Polyimide Substrate: The polyimide substrate in which the thinned die were embedded was comprised of three layers and two separate polyimides. The process began with a bare polished silicon wafer used as a processing wafer. In order for the process to work, the embedded die had to be released from the processing wafer at the end of processing. Since polyimide does not adhere to bare silicon, polyimide adhesion promoter was only applied to the processing wafer along the periphery of the top side. It was spun around the perimeter of the wafer and soft-baked. Once the adhesion promoter was in place, a layer of PI-2611 polyimide was spun on top at 3000 rpm. The wafer was then placed into a 120°C oven for a 5 minute bake before finally being cured at 350°C for 5 hours. Typically, after baking the polyimide was 5 to 6µm thick.

The second layer of polyimide was PI-2556, a much thinner layer than the PI-2611. The second polyimide layer was necessary in order to achieve good adhesion to the thinned die. In order for the two polyimides to be fully adhered, the surface of the bottom layer had to be roughened either using nitrogen or oxygen plasma. Once this was done, a thin layer (1-2µm) of PI-2556 was spun onto the PI-2611 on the process wafer. Since bare silicon does not adhere well to polyimide, the thinned die, still attached to its handle die, was coated with adhesion promoter. The die was then transferred from the DRIE holder wafer and then placed onto the uncured PI-2556 layer, handle die up. The same process was then used to cure the second polyimide layer with the die attached.

Next, the handle die had to be removed from the device die. Since the adhesive is dissolved in acetone, the processing wafer was placed into acetone with a stirring rod for approximately 30 minutes. This separated the handle die from the device die attached to the polyimide. It should be noted that after this step it was extremely important to do a long dehydration bake to purge any acetone from the polyimide. Otherwise it would bake out during the curing of the final polyimide layer, causing large bubbles between the layers.

After adhesion promoter was used to coat the topside of the thinned die, the final layer of polyimide was spun on. PI-2611 was used for this layer in order to achieve a layer thickness of approximately 6-7µm. After another soft-bake, curing was performed with the same process as previously described.

Contact Hole Via Creation: The next step was the creation of contact hole vias through the top polyimide layer to the wirebond pads on the embedded die. The polyimide wafer was masked and the top polyimide layer was oxygen plasma etched (STS AOE) to open the visa. Since etching was performed with DRIE oxygen plasma, a thicker photoresist was required. For this process, 4620 positive photoresist was spun onto the wafer at 1000rpm, resulting in a thickness of 18-20µm. This thickness was important since the etch process etched approximately 3µm of polyimide for every 5µm of photoresist. Once coated and soft-baked, the wafers were contact printed and exposed for three 30 second cycles, developed and then exposed under UV light for an additional 20 seconds.

Once properly masked, the wafers were placed in the etcher for three 9 minute etch runs. Measurements showed that approximately 2.5µm of polyimide were etched with each run. After the third run, the contact holes were open to the die aluminum pads. Then the remaining photoresist was stripped off. A photograph of a polyimide coated thinned PB6 die after the contact holes were patterned in the polyimide is presented in Figure 16.

Interconnect Formation: The daisy chain interconnect pattern for this test device was implemented using a standard Ti-Cu-Ni-Au process. A seed layer of 250Å Ti and 2500Å Cu was deposited over the entire wafer by electron beam evaporation for use as a plating seed layer. Channels for realizing the interconnections were then patterned in approximately 4µm of AZ9245 in preparation for plating 1µm of copper, 0.5µm of nickel, and 1µm of gold onto the exposed seed layer. After plating, the photoresist and the background seed layer were stripped, leaving the finished device on the processing wafer. A photograph of the plated traces connected to a thinned PB6 die is presented in Figure 17. The

fabricated device could then be pealed off of the processing wafer, yielding the completed device.

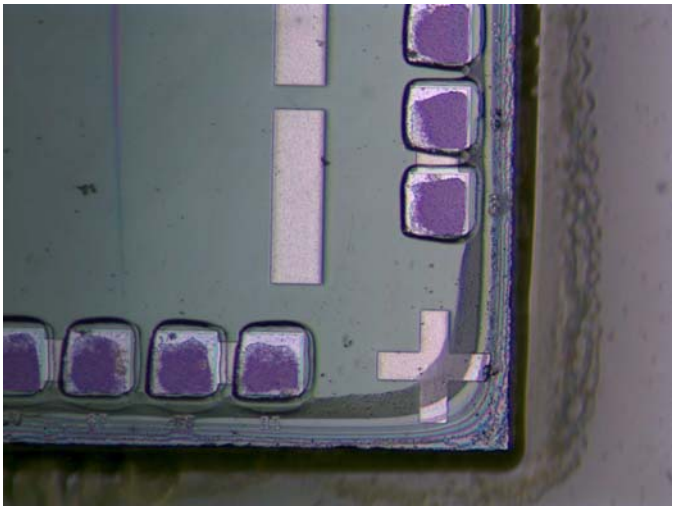


Figure 16. Photograph of the Pad Contact Holes in a Polyimide Coated Thinned PB6 Die.

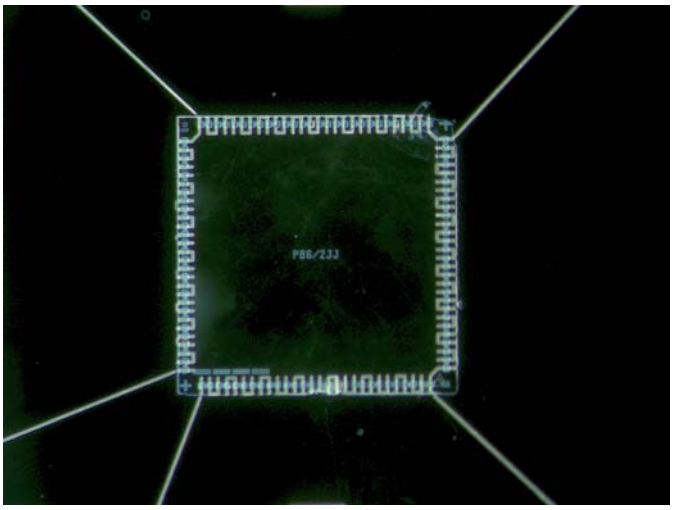


Figure 17. Photograph of a Fabricated Device.

Conclusions

Ultra-thin flexible microelectronics have many applications, including conformal and wearable electronics. A key to achieving this is the development of techniques to thin Si die to thicknesses less than 50µm. Three techniques have been developed to integrate ultra-thin die onto or into flexible polymeric substrates such as LCP and polyimide.

Acknowledgments

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