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Dynamic SDRAM SEFI Detection and Recovery Test Results

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***Abstract*—Single Event Functionality Interrupt (SEFI) results are presented for Hynix SDRAMS. SEFI response threshold is below LET 9.9 Mev-cm^2/mg and saturated cross section is 6x10^{-5}cm^2. Dynamic SEFI identification was made, and in-situ recovery restored functionality. Verification results of the identification algorithm are presented. An observed high current radiation response is also presented.**

Keywords-SEFI, SEU, SDRAM, Radiation Effects

I. INTRODUCTION

This paper covers single event functionality interrupts (SEFIs) on Hynix/Hyundai HY57V654020B SDRAMs. Although the data is provided, there are really two main issues of concern in this paper. The first is dynamic SEFI identification and recovery of the device after such an event. The second is observation of a SEFI mode whereby the device becomes unusable.

Device interrupt due to radiation will continue to be a major issue due to the competing demands on spacecraft architecture. To derive this, factor in minimal power cycling, minimal failure identification, ever-faster modern device structures and evolving system architectures. Designers are not usually interested in what causes these interrupts, but rather, how to deal with them. In a broader sense, however, while rates stay low enough and effects stay manageable enough, empirical results quantifying just how many SEFIs are occurring is sufficient. In order to spot the trends before entire device types, or even technologies, will no longer have manageable effects, it is useful to try to second-guess error modes such as SEFIs and measure their rates even though mitigation schemes are presently sufficient.

II. BACKGROUND

SEFI is something of a catch all phrase for device interrupt due to radiation. Classification systems sometimes separate observable signatures such as row or column hits, region-type failures, or current behavior. This work uses a definition of SEFI that is purely based on observation. If a memory device begins to show an error rate higher than expected due to uniformly distributed bit upsets, it is a SEFI. [1-5]

The work herein covers SDRAMs, which continue to be considered for space applications due to speed and density considerations. The complexity of mitigation systems for general SDRAM failure continues to grow due to complex failure modes on these devices. Thus a wide variety of failures might need mitigation. Using the generic definition of a SEFI, most such failures are usually detected, and any additional failures would require special testing.

SDRAMs are among the simplest devices with an internal state machine. Thus they are among the simplest where dynamic testing is necessary. Development and tuning of such a dynamic test is a useful way of isolating SEFIs as they occur in order to improve event and fluence counting.

SEFI mitigation in SDRAMs is often easy to handle. Koga et al have shown that periodically rewriting the mode register of the device basically removes the possibility of SEFI effects for many SDRAMs. Developing test data on this phenomenon is therefore not entirely necessary for particular applications if the circuit is flexible enough to follow their prescription. To understand the trends and follow possible scaling, voltage, and technology dependencies of the underlying phenomenon, masking of SEFIs is not desired. Also, SEFI susceptibility and behavior in these simpler devices may provide insight into test methods and mitigation schemes for more complex devices.

III. THEORY

A particle strike disruptive enough to upset the control structure of an SDRAM is the primary source of SEFI. There are several internal mechanisms that can potentially be affected. These include control latches that handle auto sequencing of data, transfer paths that might trigger actions not requested, and elements directly affecting the state machine of the device.

When such a strike occurs, if the result is observable, the output stream will eventually be affected. Since this effect might be delayed, a single SEFI might disrupt so much data it is misinterpreted as multiple SEFIs. Although it can be effective to look at device snap-shots for increased SEU density, a dynamic solution is desired.

In this paper an attempt is made to push SEFI identification closer in time to its occurrence. Since the output stream eventually shows increased SEU density following SEFI, recovery is triggered upon that sign. This allows better identification of the fluence to SEFI. It should be noted there was no attempt to identify SEFIs outside of the increased SEU density, except if the recovery did not work.

Only the recovery mechanism remains for examination here. The first issue concerning recovery is returning the

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device to a fully functional state. For the test devices there are two categories of this recovery: those where reinitializing the device was successful, and those where reinitializing failed. Provided reinitialization is successful, the device is reprogrammed, and the test resumes.

IV. Development Work

Modification of JPL's SDRAM test setup turned the system into a SEFI tester. The primary modification was the addition of a shifting buffer to track the number of addresses with errors seen out of the last *N* addresses, and to force a SEFI recovery if *n* of those addresses showed errors. Secondary modifications included SEFI reporting algorithms, and the ability to turn-off writing of data during read operations, possibly to limit fake SEFIs. For clarity, this algorithm declares a SEFI in the event the address error density reaches *n* in *N*.

Since SEFIs are identified based on upsets, it is particularly important to know what the susceptibility of the algorithm is to non-SEFI upsets. DRAM cells are known, in many cases, to upset in only one direction. Unfortunately, the upsettable direction is not always easy to determine, or worth the additional complication. To minimize pattern dependency, and possible memory type dependency, the algorithm implements a pseudo-random pattern when writing to the device, provided writing is enabled.

This pattern has the following inherent limitation. For a device with *x* data bits, there is a 1 in 2^x chance that none of the bits, in a particular address, will be visible during upset or SEFI. (Values for *x* range from 1 to 256, but for the Hynix part tested, *x* is 4.) Provided the settings for *N* and *n* are chosen appropriately, this missing portion poses a negligible correction to the SEFI cross section.

The ability of the SEFI detection system to provide quick identification and a minimum of erroneous results determines the merit of the system. Since this work did not have access to the full functional chart of the device, the actual extent to which these goals were met is unknown. For applicability to other test results, and perhaps for interpretation by designers, the test flow chart is included in Fig. 1.

Upset-based SEFIs were not the only type seen. The tested Hyundai devices also showed a high current mode. When that was observed during testing, modifications were made to the test system because these high current pseudo-SEFIs (since they didn't always recover) occurred more readily when the test program was not exercising the DUT.

V. Test Details

Two sets of test devices were used. All test devices were Hyundai HY57V654020B SDRAMs. For the first set, five bare dies were bonded into ceramic bond-out packages. The second set of devices, which totaled three DUTs, was based on plastic encapsulated parts that were either partially or completely acid decapsulated. Two were partial, and were thus expected to be useful for qualitative system checks since they have either plastic or lead-frame covering much of their dies. The final device was completely decapsulated and rebonded to mimic the devices in the first set.

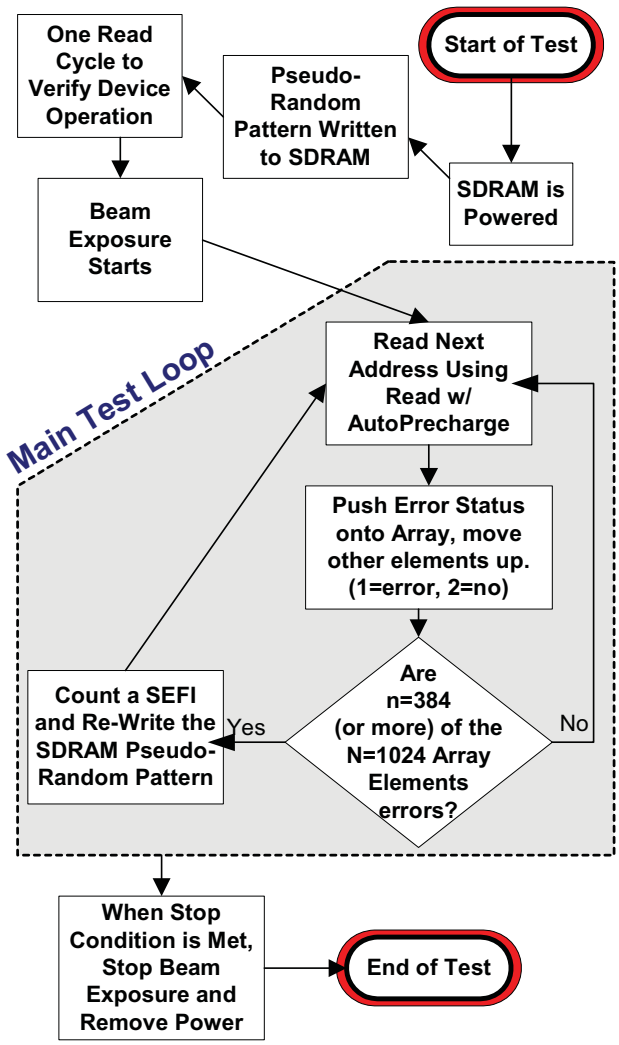

Figure 1. This flowchart shows the operation of the test algorithm. This is the normal test flow, and does not represent every test situation used. The main test loop portion has current monitoring, maximum passes, and test operator watchdog operations to allow exiting the loop.

SEFIs are expected to occur in the control circuitry only. Hence, it is expected that the sensitive regions of the devices are the control structures near the bond pads at the axial spine of the device, and therefore devices might not require full decapsulation. Unfortunately, these SDRAMs are known to behave very differently across both lot/date codes, and diffusion lots, and these categorizations are different for the two sets, so the test behavior was not expected to be identical.

The devices are arranged with 12 row bits, 10 column bits, and 2 bank bits. They have a 4-bit-wide data word. The usual testing arrangement was 12 row bits by 3 column bits by 2 bank bits, which reduced full cycle time from minutes to ~1.5 seconds.

Testing was conducted at the Lawrence Berkeley National Laboratory (LBL), and at Texas A&M (TAM). The results of the initial testing at LBL prompted the follow-up test at TAM. Basically the LBL results are the quantitative results while the

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TAM results provide evidence of the validity of the data, while attempting to spotlight the high current behavior discussed later. The list of ions and LETs used in this work is included in tables 1 and 2.

TABLE I. IONS USED FOR SEFI TESTING AT LBL

Ion	LET (MeV-cm^2/mg)	Range (μm)
^{18}O	2.2	230
^{22}Ne	3.4	179
^{40}Ar	9.9	129
^{65}Cu	21.6	108
^{86}Kr	30.0	111
^{136}Xe	53.6	110

TABLE II. IONS USED FOR SEFI TESTING AT TAM

Ion	LET (MeV-cm^2/mg)	Range (μm)
^{63}C	19.3	141
^{63}C	21.6	104
^{63}C	22.0	96
^{129}Xe	50.8	126
^{129}Xe	60.0	60

Fig. 2 shows the arrangement of test appliances for the testing at LBL, the TAM version of the setup is the same except that a vacuum system was not used. The DUTs were tested on a custom SDRAM test apparatus. Power delivery from an HP6629 power supply was provided on 40-pin ribbon cables. The standard JPL power supply control program operated, monitored, and logged the power supply. This system has 100 ms observation and shutdown control over the HP6629. For this testing, the devices were operated at 3.3V, at room temperature, with a latchup threshold starting at a current of 50mA. During the testing the latchup threshold was found to be inadequate due to false latchup events, therefore the threshold was raised to 100mA, and finally to 500mA. No latchups were observed, but device currents did wander as high as 250mA.

DUT operation signals originated from the test computer via a custom PCI digital I/O card. They connected on 40-pin ribbon cables as well. All signals, including the clock, were generated in the test computer. Due to the nature of PCI I/O, these signals are not generally regular, and in some cases have 100 ms of dead time between signals. In this arrangement, full refresh took about 50 ms of signal time, and is based on row address refreshing only. Rough study of these intervals suggests typical refresh is not likely to be longer than 250 ms. The manufacturer's specification is 64 ms at 70 degrees Celsius. Using a derating of 2x per 10 degrees Celsius, operation at room temperature is expected to be sufficient with a refresh of 1s. Operation was observed to be adequate at the expected 250 ms level.

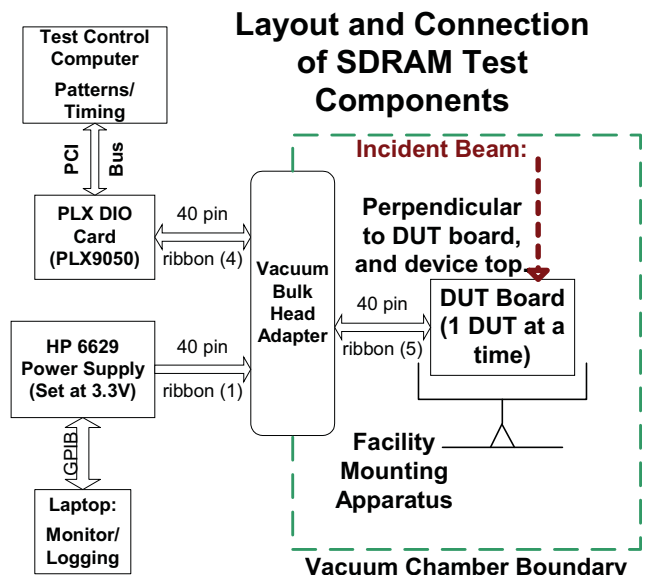

Figure 2. This is the layout of the test apparatus used. There are two test PCs (on left) which are connected via the bulk head adapter to the DUT board (on right).

One of the key goals of the TAM testing was verification of the test algorithm. To that end, several configuration modifications were tested. These include enabling device writing during irradiation, different buffer and SEFI threshold sizes, and different addressing schemes.

VI. RESULTS OF TESTING

The results presented here are separated into four areas. The first is the algorithm development and its goals, basically establishing foundation to the test method. The second is the primary goal of the testing which is obtaining SEFI cross section data. The third result is a quick listing of the single bit upset (SBU) parameters. The final portion of this section covers the wandering device current during irradiation (and possible permanent device failure).

A. Algorithm Development

Algorithm development made many assumptions that might affect data validity. Beyond assumptions were algorithmic and test variables that might also influence the test results. To address some of these the test was modified in a few different ways to look for dependencies on test conditions. The modifications included changing the definition of SEFI from (n,N) = (384,1024) to (96,256) and to (1536,4096). Also the system was checked to see if writing would cause modified SEFI cross section. The final algorithm modification was to change the addressing of the device to emphasize columns over rows. These results are presented in Fig. 3. Some other system validation notes are made in the wandering current portion of the results.

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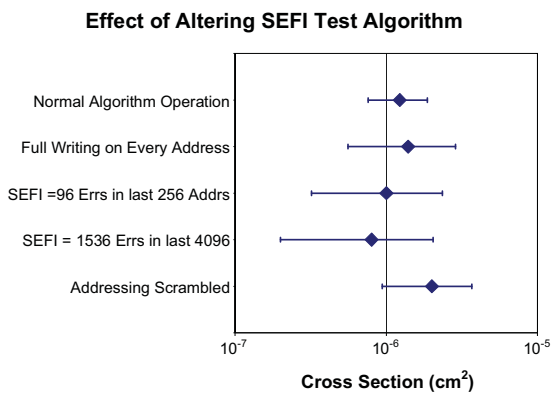

Figure 3. Results of altering the SEFI algorithm. The various methods of altering the algorithm result in statistically indistinguishable results. This data was taken with device H1 at TAM.

B. *Normal SEFIs*

The primary goal of the test was to produce data on recoverable SEFIs. The first result along these lines is the absence of any SEFIs where power cycle was required to return the DUT to normal operation. Implementing the manufacturer's warm-up and mode register program sequence recovered all recoverable SEFIs.

For the main SEFI results, multiple runs at a single LET are averaged for each part. This should promote the cancellation of random errors inherent with particle beam experiments, but still retain the part-to-part variations known to exist for SEE testing. However, this technique will not mitigate any biasing that systematic error or experimental limitations might introduce. The results are shown in Figs. 4 and 5 for the LBL and TAM testing. Note the large variation found in both data sets and between the data sets. Also recall that H1 and H2 are packaged differently than UCH1. The concentration around LET = 20 MeV-cm2/mg is due to the likelihood of high current failures in that region.

C. *Single Bit Errors*

During this testing, the SBU rate for these DUTs was recorded when possible. For comparison to other data, the SBU parameters are presented here. SBUs are defined as bits that read out opposite the value that was stored. The threshold for SBUs was about 3.4 MeV-cm^2/mg, and the saturated device cross section was around 5 cm^2.

D. *High Current Data*

Various high currents were observed during testing. Qualitatively different results for this phenomenon were found at LBL and TAM. Irradiating under static bias exacerbated the problem. At TAM the DUTs always returned to their pre-irradiation current draws by either exercising them (including state register reset) or power cycling. At LBL, in contrast, devices often had permanent changes in their operating currents some moving as high as 10 times their original operating currents. Also, at LBL, operation of two of the DUTs ("Device 4" with static bias and "Device 5" under dynamic operation) during long irradiations with more than 1e7 ions at greater than 20 LET resulted in permanent device failure. A strip chart for one of these high current irradiations is shown in Fig. 6.

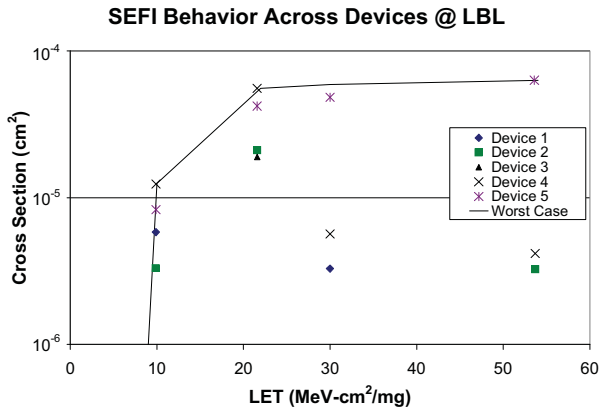

Figure 4. Cross section for SEFIs from data taken at LBL. The spread at high LETs could be due to device degradation, lot to lot variations, or even heating and environmental conditions. Note the worst case curve is based on a data point of no SEFIs at LET=8.4 MeV-cm2/mg courtesy of BAE Systems.

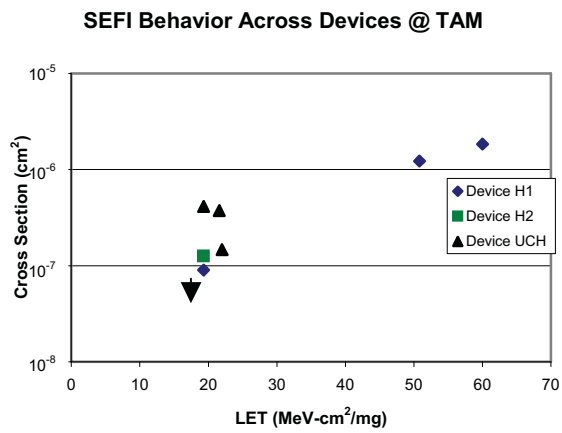

Figure 5. The TAM SEFI cross sections are a byproduct of test runs for high current failure, and are included for completeness. Notice, on the consistency of the data set, the UCH rebounded device behaved similarly to the partially acid decapsulated H1 & H2. Comparison to Figure 4 shows these results are an order of magnitude lower than the LBL results.

VII. Discussion of Results

The raw results are somewhat difficult to keep straight, as there were multiple probes in operation at once. This discussion of results will start by pointing out the limitations of the data. The validity of the algorithm will be covered. From there, the main goal of the investigation, SEFI results will be discussed. The remaining topic of the high current behavior is a separate issue and will be covered in the concluding portion of this section.

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A. Data Limitations

Besides the requisite SEE test data limitation of not having enough DUTs, there were other limitations that should be cataloged. Except for the results of the high current testing, these limitations are not expected to have greatly modified the results, since they probably only lead to scatter, which is already a key factor in all the results.

As an organizational aid, the first set of limitations follows from the differences in the two test facilities. The LBL devices were tested in vacuum. This immediately begs the environmental question whose answer is that no temperature control was used. Also the cabling was somewhat different, with the TAM cables being ~6 feet and the LBL cables being 60 feet. The impact of these is that the data sets cannot be directly compared. In fact, the high current failure seen at LBL might be a byproduct of the additional heat build-up in vacuum. The long cables are not expected to be a major concern because the signals were run through differential receiver-driver pairs, and never faster than 30 ns switching. Due to facility limitations and test goals, neither facility was requested to provide beams between LETs of 3.4 and 9.9 MeV-cm^2/mg.

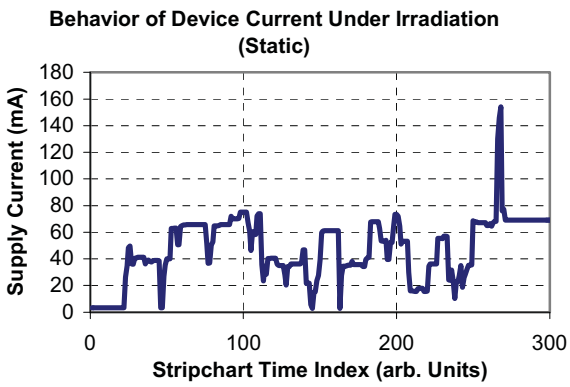

Figure 6. During irradiation at TAM under static bias, the device current was quite erratic (for LETs above 10 MeV-cm^2/mg). This current stripchart shows what such a run looks like. Similar runs were seen at LBL with some showing currents above 250mA. Two of the LBL devices failed in response to this behavior.

A second division in organizing the limitations is to look to the DUTs themselves. First and foremost are the differing decapsulation methods. The DUTs marked H1 and H2 were only partially decapsulated. Thus their results are likely to be different from the remainder of the DUTs. The fact that for SEFIs this appears to not be the case might be a very good result for this type of testing because preparation of H1 and H2 was easily ten times less expensive than the remainder of the DUTs. The second DUT related limitation is the severe dependence of this device type to both the lot/date code and diffusion lots of the tested devices. Unfortunately, although both are known for the devices tested at LBL, for the remaining devices this information was not tracked all the way through the rebonding process; and H1 and H2 are known to be different from those tested at LBL.

The final set of limitations to this test data is from the tester itself, and remaining variables in the algorithm that were not explicitly tested. There is the issue of the device size that was tested. Since the two tested configurations had the same number of address bits, none of the results presented here can be identified as intrinsic or extrinsic. Probably SEFI cross section is an intrinsic variable, like pressure, and changing how much of the device you are testing doesn't effect the result; but this was not tested. The tester also used a static address scheme of Z:Y:X where Z are bank bits, Y are column bits, and X are row bits. This means that SEFIs which wipe out all the columns in a particular row might not trigger a SEFI in the test algorithm. One other tester related issue is the method of device refresh. It is known that SEFIs can be different in different refresh modes. Only one refresh mode was used in this testing. The mode used is the passive refresh that occurs when the DUT's rows are addressed. Explicitly, no other self, auto, or other manual refresh was used. The final limitation related to the tester is the "static" bias testing used to provide much of the high current results. For the results presented, there was no clock under static bias, a situation that is probably unlikely for a real application.

B. Algorithm Results

The algorithm proved to be quite robust considering its simplicity. This may not be the case for other device types, or operational modes. The results presented suggest several things. First, the major region of the DUT die that causes SEFI is on the axial spine of the devices near the bond pads. Second, reading and writing made no statistically significant difference in SEFI behavior.

The last major result of the algorithm verification was to show that the definition of a SEFI was well behaved. Often when examining phenomena that are defined by a threshold (e.g. earthquakes), the definition of the object greatly changes how many you see (i.e. if you labeled a 1.0 or greater "seismic event" as an earthquake, you would say earthquakes happen all the time). The fact that the definition of a SEFI as an event where the number of errors n in a region of the DUT of length N does not depend much on the selection of n and N is a useful result. It should be noted, however, that the ratio n:N was held constant, however careful consideration of the algorithm should show that only n is really meaningful, but this could have been verified empirically.

C. SEFI Results

The spread in measurements makes it difficult to infer definitive conclusions from the data set, however it was decided that a worst case enveloping curve be used to calculate an upset rate. To do this, the LBL results were used as the basis since the TAM results were taken with only qualitative results in mind.

This worst-case curve is also shown in Fig. 4. The behavior of the enveloping line at the low end is due to the absence of SEFIs (with more than 1e8 fluence) at LET 3.4 MeV-cm^2/mg, and known threshold near LET = 8 MeV-cm^2/mg [6]. Based on this information, the inferred rate may or may not be conservative.

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Another conservative assumption in the rate calculation was the use of the worst-case angular response for the device. By using these assumptions, and the data shown in Fig. 4, the device SEFI rate is 2e-4/device-day for solar minimum GCR.

D. High Current Response

The DUTs showed a high current response that demands some investigation. Through the limitations and results section, much of what can be said about this problem has been said. Since two devices were non-functional following irradiation at LBL an attempt was made to reproduce the failures and possibly gain additional statistical significance. The attempt to do so at TAM was unsuccessful; and there are several possible reasons why.

The TAM results were promising toward understanding the problem, because they did provide some high current behavior. However the devices never failed to return to their original current draws following the high currents.

Ultimately the static bias results at TAM and the general high current results at LBL lead to some interesting questions. Static bias should probably not be used on these devices. Since the failures observed at LBL were likely due to both the standby current degradation that was observed and the momentary high currents observed at both locations, it is possible that controlling the amount of time the device is holding high current and the duration of exposure might be important for handling this issue. Also, no rates were measured for this phenomenon or any sub-classification of it, so no estimation of how likely a problem this might be based on length of mission can be provided.

VIII. CONCLUSION

Qualitative validation of a SEFI testing algorithm for SDRAMs showed the presented method of SEFI testing is fairly robust. Limitations of this testing, as presented, can be used for both improving the algorithm itself, and for further establishing its validity. In order to do this, to the level indicated in this paper, initial testing at LBL was followed by algorithm and exotic result (high current) testing at TAM.

The exotic result seen at LBL, the full failure of two of the test devices, was not corroborated by the TAM testing. There are several possible reasons for this, including heating and differing device lots. This phenomenon can be interpreted as the sequence: high current events lead to higher nominal operating current, which leads to device failure. In that sense, the TAM results agree with the LBL results on the first stage of this sequence, since high current behavior was observed at TAM.

Dynamic SEFI testing on the Hyundai HY57V654020B SDRAM is a viable way of estimating possible effects on more complicated devices. Similar testing might be necessary on other devices as complexity levels grow and contribute further SEFI modes. For these devices, SEFI identification where 384 of the previous 1024 addresses show errors provides a worst-case SEFI threshold around 8 MeV-cm^2/mg, with a saturated cross section of 6e-5cm2, for any mode fitting this definition. These numbers translate to a 2e-4/device-day SEFI rate in solar minimum GCR.

The devices proved to be always recoverable, provided they survived the radiation, by reprogramming the mode register. This is a useful result, because flight applications often cannot easily power-cycle devices. The high current and failure modes observed should also be of interest to flight applications.

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