

Transistor-Level Circuit Experiments Using Evolvable Hardware

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Abstract

The Jet Propulsion Laboratory (JPL) performs research in fault tolerant, long life, and space survivable electronics for the National Aeronautics and Space Administration (NASA). With that focus, JPL has been involved in Evolvable Hardware (EHW) technology research for the past several years. We have advanced the technology not only by simulation and evolution experiments, but also by designing, fabricating, and evolving a variety of transistor-based analog and digital circuits at the chip level. EHW refers to self-configuration of electronic hardware by evolutionary/genetic search mechanisms, thereby maintaining existing functionality in the presence of degradations due to aging, temperature, and radiation. In addition, EHW has the capability to reconfigure itself for new functionality when required for mission changes or encountered opportunities. Evolution experiments are performed using a genetic algorithm running on a DSP as the reconfiguration mechanism and controlling the evolvable hardware mounted on a self-contained circuit board. Rapid reconfiguration allows convergence to circuit solutions in the order of seconds. The paper illustrates hardware evolution results of electronic circuits and their ability to perform under 230°C temperature as well as radiations of up to 250 kRad.

1. INTRODUCTION

The Jet Propulsion Laboratory (JPL) performs research in fault tolerant, long life, and space survivable electronics for the National Aeronautics and Space Administration (NASA). JPL has been involved in Evolvable Hardware (EHW) technology research for the past several years. EHW can bring some key benefits to spacecraft survivability, adaptation to new mission requirements and mission reliability. The idea behind evolutionary circuit synthesis/design and EHW is to employ a genetic search/optimization algorithm that operates in the space of all possible circuits and determines solution circuits that satisfy imposed specifications, including target functional response, size, speed, power, etc. In a broader sense, EHW refers to various forms of hardware from sensors and antennas to complete evolvable space systems that could adapt to changing environments and, moreover, increase their performance during their operational lifetime. In a narrower sense here, EHW refers to self-reconfiguration of transistor-level electronic hardware by evolutionary/genetic reconfiguration mechanisms.

EHW can help preserve existing circuit functionalities, in conditions where hardware is subject to faults, aging, temperature drifts and high-energy radiation damage. The environmental conditions, in particular the extreme temperatures and radiation effects, can have catastrophic impacts on the spacecraft. Interstellar missions or extended missions to other planets in our solar system with lifetimes in excess of 50 years are great challenges for on-board electronics considering the fact that presently, all commercial devices are designed for at most a 10-year lifespan. Further, new functions can be generated when needed (more precisely, new hardware configurations can be synthesized to provide required functionality). Finally, EHW and reconfigurable electronics provide additional protection against design mistakes that may be found after launch. Design errors can be circumvented during the mission either by human or evolutionary driven circuit reconfiguration.

One clear example of a space exploration area where EHW can directly provide benefits is the extreme-environment operation of electronics for in-situ planetary exploration. It may require electronics capable of operating at low temperatures of -220°C for Neptune or moon, (-235°C for Titan and Pluto) and also high temperatures, such as above 470°C needed for operation on the surface of

Venus. Terrestrial applications may include combustion systems, well logging, nuclear reactors, and automotive industry requiring high temperature operation and dense electronic packages.

In this paper we propose the use of reconfigurable chips, which allow for a large number of topologies to be programmed in-situ, allowing adaptation to extreme temperatures and ionizing radiation. The experiments presented here illustrate hardware recovery from degradation due to extreme temperatures and radiation environments. A 2nd generation reconfigurable chip, the Field Programmable Transistor Array (FPTA-2) integrated circuit, developed at JPL, is used in these experiments. We separately subjected the chips to high temperatures and ionizing radiations using JPL facilities. Measurement results show that the original functionality of some of the evolved circuits, such as half-wave rectifiers and low-pass filters, could be recovered by again using the Evolutionary Algorithm that altered the circuit topologies to lead to the desired solutions. The Evolutionary Algorithms thus control the state of about 1500 switches, which alter the circuit topology. Using a population of about 500 candidate circuits and after running the Evolutionary process for about 200 generations, the desired functionality was recovered.

The paper is organized as follows. Section 2 reviews main aspects of EHW including reconfigurable devices and reconfiguration mechanisms for hardware evolution on a EHW testbed. Section 3 describes experiments on the evolutionary design of analog circuits. Section 4 describes experiments on electronic survivability through evolution, including evolutionary recovery at extreme temperatures and ionizing radiation. Concluding remarks are given in Section 5.

2. EVOLVABLE HARDWARE

Presently, the evolutionary search for a circuit solution is performed either by software simulations [1-3] or directly in hardware on reconfigurable chips [4]. However, software simulations take too long for practical purposes, since the simulation time for one circuit is multiplied by the large number of evaluations required by evolutionary algorithms. In addition, the resulting circuit may not be easily implemented in hardware, unless implementation constraints are imposed during evolution. Hardware evaluations can reduce by orders of magnitude the time to get the response of a candidate circuit, potentially reducing the evolution time from days to seconds [4].

Hardware evaluations commonly use commercial re-configurable devices, such as Field Programmable Gate Arrays (FPGA) or Field Programmable Analog Arrays (FPAA) [5-6]. These devices, designed for several applications other than EHW, lack evolution-oriented features, and in particular, the analog ones are sub-optimal for EHW applications.

2.1 Evolution-Oriented Reconfigurable Architectures

Many important aspects of evolution-oriented reconfigurable architectures (EORA) must be considered to best support the EHW. The granularity of the programmable chip is an important feature. A first limitation of commercial FPGAs and FPAA's is their coarse granularity. From the EHW perspective, it is interesting to have *programmable granularity*, allowing the sampling of novel architectures together with the possibility of implementing conventional architectures. The optimal choice of elementary block type and granularity is task dependent. From the point of view of experimental work in EHW, it appears that the reconfigurable hardware based on elements of the lowest level of granularity is a good choice to build. Virtual higher-level building blocks can be considered by imposing programming constraints. EORA should also be *transparent*, thereby allowing analysis and simulation of the evolved circuits. They should also be robust enough not to be damaged by any bit-

string configuration existent in the search space, potentially sampled by evolution. Finally EORA should allow evolution of both analog and digital functions.

With the granularity in mind, Field Programmable Transistor Array (FPTAs) chips were designed at JPL and particularly targeted for EHW experiments. The first two versions of the FPTA (FPTA-0 and FPTA-1) relied on a cell with 8 transistors interconnected by 24 switches [5]. They were used to demonstrate intrinsic evolution of a variety of analog and digital circuits, including logical gates, trans-conductance amplifiers, computational circuits, etc.

The newer version, FPTA2, is a second-generation reconfigurable mixed-signal chip consisting of an array of cells, each with 14 transistors connected through 44 switches. The chip is able to map different building blocks for analog processing, such as two- and three-stage OpAmps, logarithmic photo-detectors, or Gaussian computational circuits. Figure 1 shows the details of the FPTA-2 cell. As shown, these cells can be programmed at the transistor level. The chip architecture consists of an 8x8 matrix of re-configurable cells. The chip can receive 96 analog/digital inputs and provide 64 analog/digital outputs. Each cell is programmed through a 16-bit data bus/9-bit address bus control logic that provides an addressing mechanism to download the bit-string of each cell. A total of 5000 bits is used to program the whole chip.

2.2. Evolutionary Reconfiguration Mechanisms

The main steps of evolutionary synthesis are illustrated in Figure 2. The genetic search in EHW is tightly coupled with a coded representation that associates each circuit to a "genetic code" or chromosome. The simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. Each bit of the binary sequence refers to a particular switch location. The status of the switches (ON or OFF) determines a circuit topology and consequently a specific response. Thus, the topology can be considered as a function of switch states, and can be represented by a binary sequence, such as "1011...", where a '1' is associated to a switch turned ON and a '0' to a switch turned OFF.

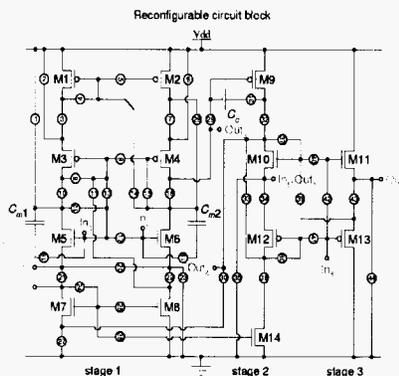


Figure 1. FPTA-2 cell topology with transistors M1 thru M14, connected through 44 switches. The chip has an 8x8 array of cells.

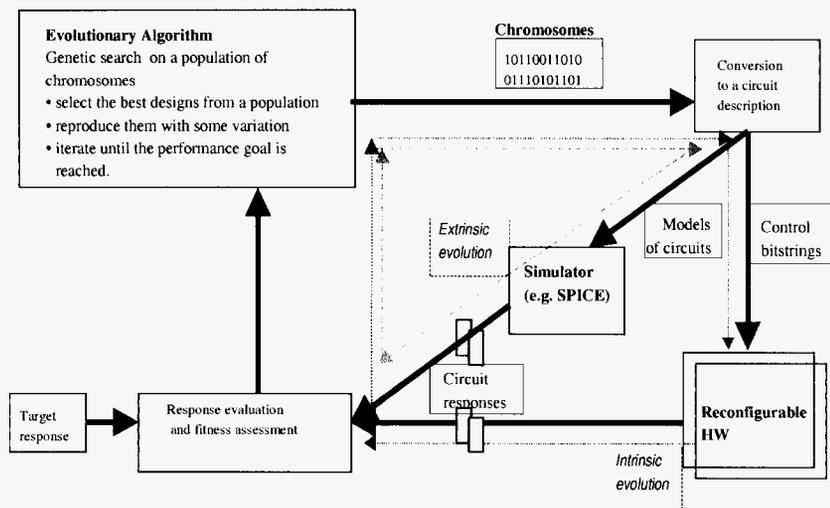


Figure 2: Main steps for the evolutionary synthesis of electronic circuits showing extrinsic and intrinsic evolution paths.

First, a population of chromosomes is randomly generated. The chromosomes are converted into circuit models for evaluation in SW (extrinsic evolution) or into control bitstrings downloaded to programmable hardware (intrinsic evolution). Circuit responses are compared against specifications, and individuals are ranked based on how close they come to satisfying them. In preparation for a new iteration, a new population of individuals is generated from the pool of best individuals in the previous generation. This is subject to a probabilistic selection of individuals from a best individuals pool, followed by two operations: random swapping of parts of their chromosomes, the *crossover* operation, and random flipping of chromosome bits, the *mutation* operation. The process is repeated for several generations, resulting in increasingly better individuals. Randomness helps to avoid getting trapped in local optima. Monotonic convergence (in a loose Pareto sense) can be forced by unaltered transference to the next generation of the best individual from the previous generation. There is no theoretical guarantee that the global optimum will be reached in a useful amount of time; however, the evolutionary/genetic search is considered by many to be the best choice for very large, highly unknown search spaces. The search process is usually stopped after a pre-selected number of generations, or when closeness to the target response has been reached to a sufficient degree. One or several solutions may be found among the individuals of the last generation.

2.3 Evolvable Hardware Testbeds

The JPL Evolvable Hardware Testbed was developed to support both SW and HW evaluations (extrinsic/intrinsic). The SW resources rely on a 128-processor parallel machine of SGI Origin running multiple copies of SPICE. The HW resources are built around National Instruments LabView, associated data acquisition boards, signal generators, and other equipment [8].

A Stand-Alone Board Level Evolvable System (SABLES), developed for autonomous portable experiments, is a stand-alone platform integrating the FPTA-2 and a digital signal processor (DSP) chip that implements the Evolutionary Programming (EP) code as shown in Figure 3. The system is stand-alone and is only connected to the PC for the purpose of receiving specifications and communicating back the results of evolution for analysis.

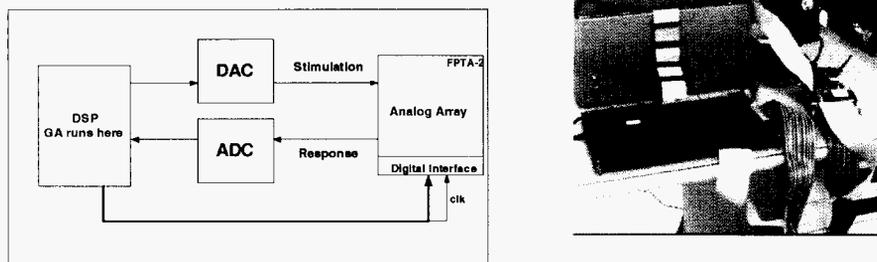


Figure 3. Block diagram of a Stand-Alone Board Level Evolvable System (SABLES). It consists of a DSP implementing the Evolutionary Programming (EP) and an FPTA-2 chip mounted on a circuit board that interfaces to a computer.

The evolutionary algorithm, implemented in a DSP that directly controlled the FPTA-2 provided with fast internal communication ensured by a 32-bit bus operating at 7.5MHz. Details of the EP were presented in Ref [9]. Over four orders of magnitude speed-up of evolution was obtained on the FPTA chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit).

3. EVOLUTION EXPERIMENTS OF ANALOG CIRCUITS

The first demonstration of SABLES was reported in Ref. [4,9]. A half-wave rectifier circuit was evolved in about 20 seconds after processing a population of 100 individuals running for 200 generations. The testing of candidate circuits was performed for an excitation input of 2kHz sine wave of amplitude 2V. A computed rectified waveform of this signal was considered as the target. The fitness function rewarded those individuals exhibiting behavior closer to target (using a simple sum of differences between the response of a circuit and target) and penalized those farther from it. In this experiment only two cells of the FPTA were allocated.

Figure 4 displays snapshots of evolution in progress, illustrating the response of the best individual in the population over a set of generations. Fig. 4 a) shows the response of the best individual of the initial population, while the subsequent ones (Fig. b, c, and d) show the best after 5, 50 and 82 generations respectively. The final solution response is shown on the right.

The evolution of other analog circuits is shown in [10].

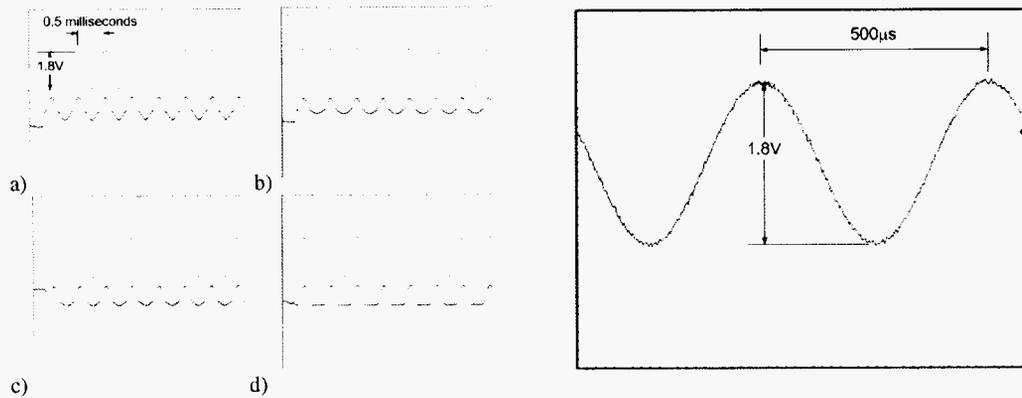


Figure 4. Evolution of a halfwave rectifier showing the response of the best individual of generation a) 1, b) 5, c) 50 and finally the solution at generation d) 82. The final solution, which had a fitness value less than 4500, is illustrated on the right.

4. EXPERIMENTS UNDER EXTREME ENVIRONMENT

4.1 Experimental Testbeds

Testbed for evolution at high temperatures: A high temperature testbed was built to achieve temperatures exceeding 350°C on the die of the FPTA-2 while staying below 280°C on the package. It was necessary to keep the package temperature below 280°C so as not to destroy the interconnects and preserve package integrity. Die temperatures were kept below 400°C to make sure die attach epoxy does not soften and that the crystal structure of the aluminum core does not degrade. To achieve these high temperatures the testbed includes an Air Torch system. The Air Torch forces out hot compressed air through a small hole within a temperature-resistant ceramic, protecting the chip. The temperatures were measured by attaching thermocouples to the die and the package.

High-energy electron radiation chamber: In the case of the radiation experiments, the radiation source used was a high-energy (1MeV) electron beam obtained using a Dynamitron accelerator. The electrons are accelerated in a small vacuum chamber with a beam diameter of 8". The flux in the chamber was 4×10^9 [electrons/(sec-cm²)], which is around 300 rad/sec.

Below we describe experiments for evolutionary recovery of the functionality of the following circuits: (1) Half-wave rectifier at 280°C temperature; (2) Low-pass filter at 230°C temperature; and (3) Half-wave rectifier at 175kRads.

4.2 Half-wave rectifier on FPTA-2 at 280°C

The objective of this experiment was to recover functionality of a half wave rectifier for a 2kHz sine wave of amplitude 2V using only two cells of the FPTA-2 at 280°C. The fitness function given below does a simple sum of error between the target function and the output from the FPTA.

The input was a 2kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for } (t_s < n/2) \\ R(t_s) - V_{\max} / 2 & \text{otherwise} \end{cases} \quad (1)$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{max} is 2V (the supply voltage). The output must follow the input during the positive half-cycle but stay constant at a level half-way between the rails (1V) during the negative half-cycle.

After evaluation of 100 individuals, they were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), (either among themselves or with an individual from the elite), followed by mutation (4% rate). The entire population was then reevaluated.

In Figure 5 the left graph depicts response of the evolved circuit at room temperature whereas the right graph shows degraded response at high temperature. Figure 6 shows the response of circuit obtained by running evolution at 280°C, whereby we can see that the functionality has been recovered.

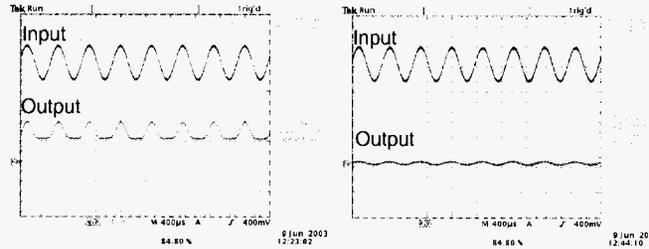


Figure 5: Input and output waves of the half-wave rectifier. On the left we show the response of the circuit evolved at 27°C. On the right we show the degraded response of the same circuit when the temperature was increased to 280°C.

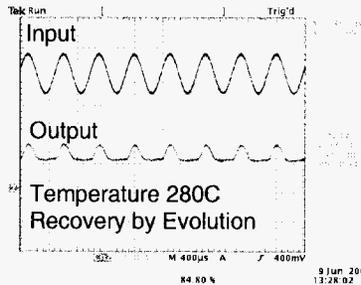


Figure 6: The response shows the recovery for the half-wave rectifier circuit at 280°C following successful evolution.

4.3 Low-Pass Filter on FPTA-2 at 230°C

The objective of this experiment was to recover the functionality of a low-pass filter using ten cells of the FPTA-2 chip. The fitness function given below performs a sum of errors between the target function and the output from the FPTA in the frequency domain.

$$F = \sum_{f_s=0}^{n-1} (R(f) - T(f)) \quad (2)$$

Given two tones at 1kHz and 10kHz, the circuit after evolution is to have at the output only the lowest frequency tone (1kHz). This evolved circuit demonstrated that the FPTA-2 is able to recover the functionality of the active filter circuit with some gain at 230°C. Figure 7 shows the response of the

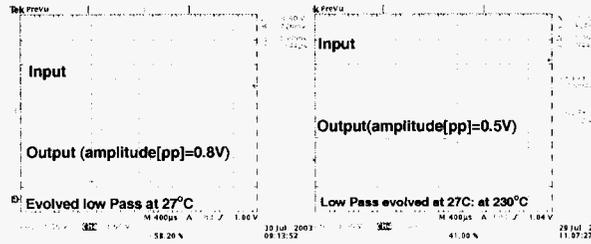


Figure 7: Low-pass filter response. The graph displays the input and output signals in the time domain when the FPTA-2 was used for evolution at room temperature (left) and at 230°C temperature (right).

evolved filter at room temperature and degradation at 230°C. Figure 8 shows the time response of the recovered circuit evolved at 230°C.

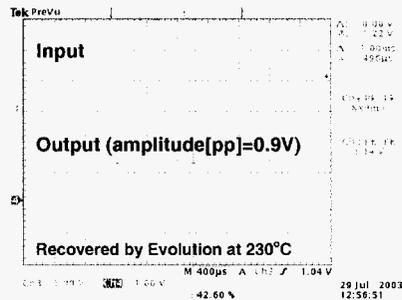


Figure 8: Recovered Low Pass Filter at 230°C.

At room temperature, the originally evolved circuit provided a gain of 3dB at 1kHz and a roll-off of -14dB/dec. When the temperature was increased to 230°C, the roll-off went to -4dB/dec and the gain at 1kHz fell to -12dB. In the recovered circuit at high temperature the gain at 1kHz increased back to 1dB and the roll-off went to -7dB/dec. Therefore the evolved solution at high temperature was able to restore the gain and to partially restore the roll-off.

4.4 Half Wave Rectifier at 175krads

This experiment was to evaluate the recovery of a half-wave rectifier after the FPTA-2 was subjected to radiation. Figure 9(a) illustrates the response of a previously evolved rectifier after the chip was exposed to a radiation dose of 50 krads. It can be observed that the circuit response was not affected by radiation. After exposure to radiation of up to 175Krad the rectifier malfunctions as the output response is identical to that of the input as shown in Figure 9(b). When the evolutionary mechanism was activated, the correct output response was recovered and retained as shown in Figure 9(c).

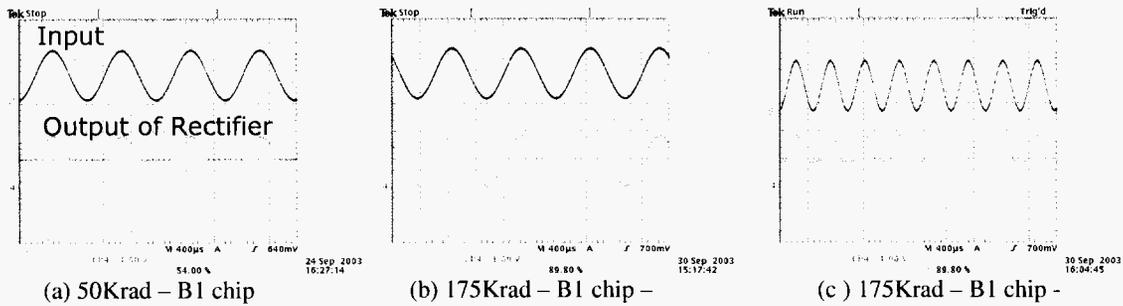


Figure 9: Response of the Rectifier circuit at (a) 50kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of rectification, followed by (c) recovery through Evolution.

5. CONCLUSIONS

The above experiments illustrate the power of EHW to synthesize new functions and to recover degraded functionality due to faults or extreme temperatures. A mechanism for adapting a mixed analog reconfigurable platform for high temperature and radiation induced faults was presented. Different experiments were carried out which exercised the reconfigurable device up to 280°C and 175Krad radiation dosages demonstrating that the technique is able to recover circuit functionality such as those of rectifiers and filters.

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