

Mitigating Upsets in SRAM-based FPGAs from the Xilinx Virtex 2 Family

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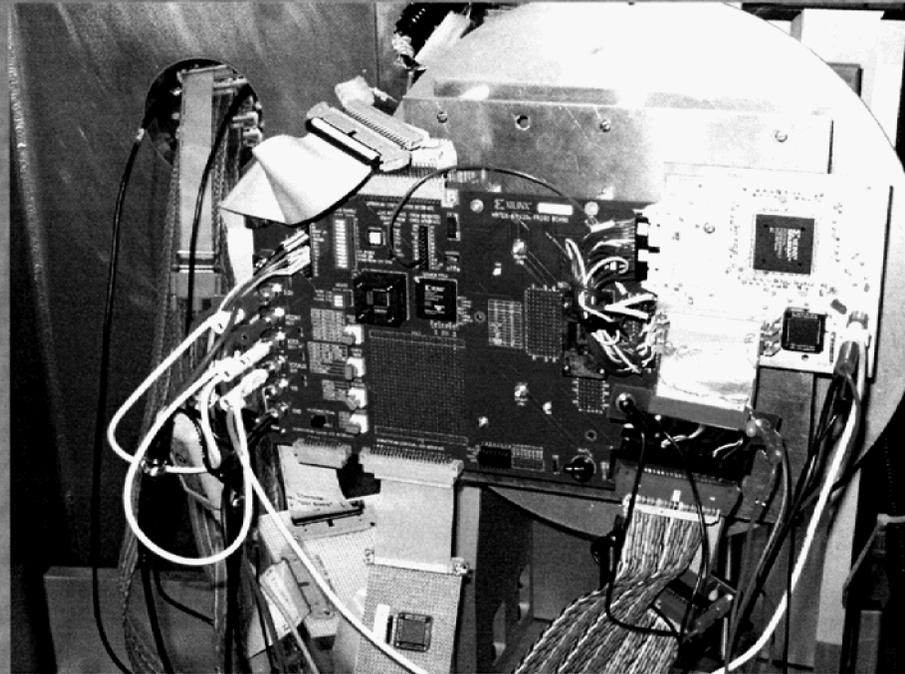
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Radiation Effects Testing on the Virtex II

- ▣ A joint effort between the Radiation Effects Group (Sec 514) and Carl Carmichael from Xilinx Inc. Later to include other organizations.
- ▣ Single-Event Upset static testing of the Virtex II has been completed
 - ▣ Upset rates for the configuration memory, block RAM and two SEFIs has been obtained
- ▣ Dynamic testing is currently underway to test functionality within the DUT during irradiation. Mitigation schemes such as partial reconfiguration and TMR are being implemented.
- ▣ A separate single-event latchup test at LET -104 MeV-cm²/mg for the XQR2V3000 showed no latchups

Experimental Details

- Device chosen for study is the X-2V1000
 - Virtex II 2V1000 device manufactured with QPro mask set and no epitaxial layer
 - Devices were radiation evaluation samples only
- Devices were tested in protons and heavy-ions



Test setup in the vacuum chamber at Lawrence Berkeley National Laboratory 88" cyclotron.

Static Test Results

- Upset rates for the configuration memory, block RAM, flip-flops and Single-Event Functional Interrupts (SEFIs) below were obtained using the Edmonds model*
- The power-on-reset (POR) and SelectMap SEFIs are low in occurrence and requires a full reset and reconfiguration before returning to normal operability
- The flip-flop data set shows wide scattering. More testing will be needed to verify flip-flop upset rates.

	Configuration Memory		Block Ram		Flip-Flops		POR SEFI		SelectMap SEFI	
	$L_{1/e}$ (MeV cm ² / mg)	σ_{sat} (cm ² / bit)	$L_{1/e}$ (MeVc m ² /mg)	σ_{sat} (cm ² / bit)	$L_{1/e}$ (MeV cm ² /mg)	σ_{sat} (cm ² /de- vice)	$L_{1/e}$ (MeV cm ² / mg)	σ_{sat} (cm ² /de- vice)	$L_{1/e}$ (MeV cm ² / mg)	σ_{sat} (cm ² /de- vice)
Test Data	8.5	5.5E-8	5	5E-8	5	1E-6	7	6E-6	7	5E-6
Upset Rates	4.4E-7/bit-day		1.1E-6/bit-day		2.1E-5/bit-day		7.0E-5/device-day		5.8E-5/device-day	

*L.D. Edmonds, "SEU Cross Sections Derived from a Diffusion Analysis," IEEE Trans. Nucl. Sci., 43, 3207-3217, Dec. 1996.

*Static data is taken from "C. Yui, G. Swift, and C. Carmichael, 'Single-Event Upset Susceptibility of the Xilinx Virtex II FPGA,' MAPLD, 2002."

Dynamic Test Results

┆ Test Design

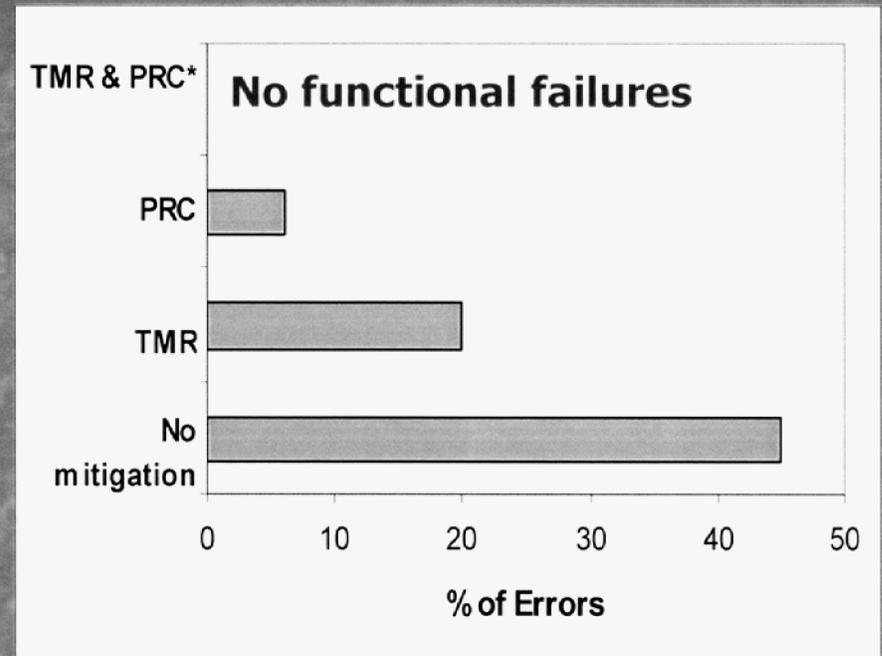
- Non-mitigated: Eight simple shift registers using 500 flip-flops each (40% of available flip-flops)
- Mitigated: Eight shift registers using 500 flip-flops each, four have triple module redundancy (TMR) implementation (80% of available flip-flops)
- Test vectors are chosen by the user: pattern of all zeroes, ones, or checkerboard

┆ Background

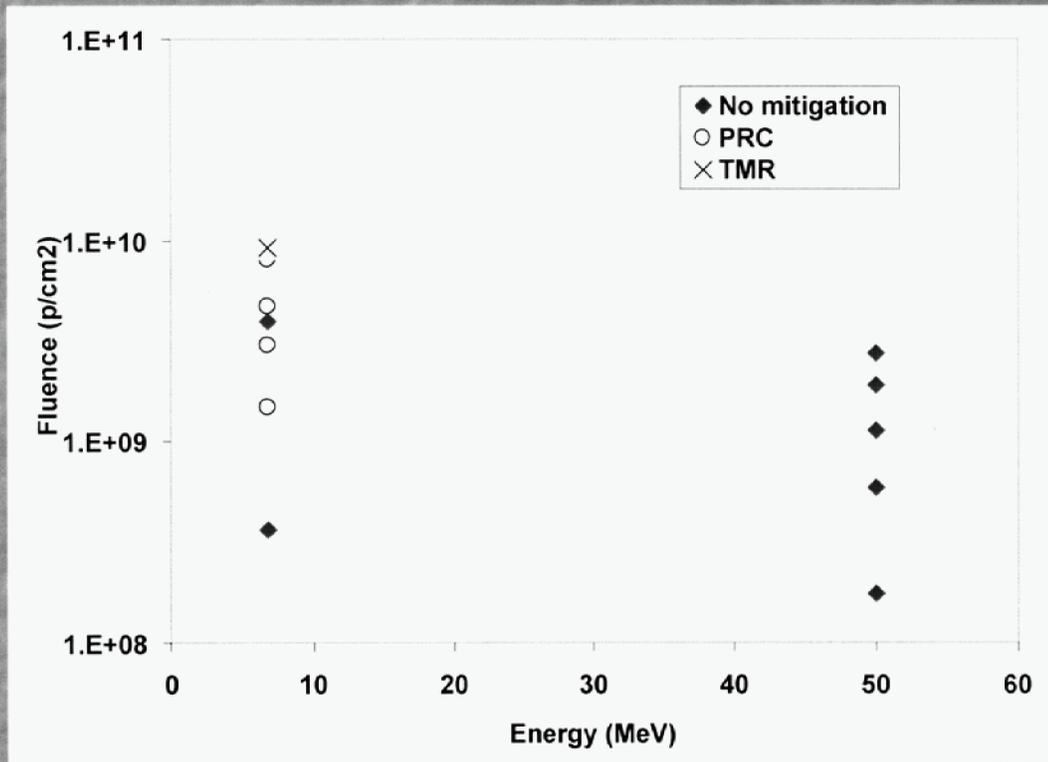
- 1st mitigation technique: Triple Module Redundancy (TMR)
 - ┆ Implements three full copies of the base design in the FPGA
 - ┆ SEUs and single-event transients (SETs) can be removed by performing a bit-wise "majority vote" on the output of the triplicate circuit (flip-flop or entire logic design)
- 2nd mitigation technique: Partial reconfiguration (PRC)
 - ┆ Partially reconfiguring the configuration bitstream prevents the accumulation of errors, a cause of functional failure in the programmed design
- Summary
 - ┆ Only recommended technique: TMR & PRC
 - ┆ This study shows that when both techniques are used in conjunction, the design is shown to be functionally immune to upsets
 - ┆ Functional failure is defined for the dynamic test to be a continuous stream of erroneous data from the shift register outputs, an indication that either configuration or user logic has been overwhelmed by SEUs

Dynamic Test Results 2

- The figure above show the average results from five runs for each design tested in protons
- The comparison shows an improvement of roughly 25% for the TMR design, 40% for the design implementing partial reconfiguration and no functional errors for the design employing both TMR and PRC
- However, although no functional errors were seen during the dynamic test of the TMR and PRC design, one single bit error for one shift register chain was noted during one beam run
 - Possible causes: Two simultaneous bit flips to the TMR voter circuit, ion strike to the input/output blocks



Dynamic Test Results 3



- Test vehicle first used at Crocker Nuclear Laboratory for proton testing
- All three mitigation designs were tested at 6.8 MeV
- A scatter plot of average first fluence to failure is shown in the figure to the left. It shows an approximate factor of two difference between the non-mitigated and mitigated designs
- Best results were obtained from the DUT programmed with the TMR and PRC design; no functional errors were observed

Dynamic Test Results 4

Additional testing allowed a more thorough understanding of SEFIs as well as better test methods (i.e. the use of JTAG in our test setup). This helped to categorize SEFIs and formulate the following table:

	POR
Effects	Clearing of configuration memory and loss of state data
Detection	Done pin transitions low, I/O becomes tri-stated, no user functionality available
Recovery	Standard configuration. No power cycle necessary.
	Select Map
Effects	Loss of communication with configuration logic. Configuration error detection and non-evasive correction unavailable.
Detection	No response to data readbacks
Recovery	Standard configuration. No power cycle necessary.
	JCFG
Effects	Loss of communication with configuration logic. Configuration error detection and non-evasive correction unavailable.
Detection	Read access to configuration memory returns constant value.
Recovery	Standard configuration. No power cycle necessary.

Dynamic Test Results 5

- The dynamic test vehicle had two SEFI detection mechanisms
 - POR detection was made possible by constantly monitoring the state of the "DONE" pin of the device
 - Simple feed-through signals in the DUT placed in close proximity can indicate when the configuration memory has accumulated excessive errors
 - No Select Map detection was provided since only JTAG was used
- Two SEFI events were recorded during dynamic testing in heavy ions:
 - POR: DONE pin transition to low, functionality is lost
 - JCFG: Unable to read or write to the configuration memory, scrubbing is disabled
- The mechanism of SEFIs are independent of mitigation and are inherent in the device. Proper mitigation and device redundancy can be used to remove all possibilities of single-event upset and produce a robust system for critical flight applications

Summary

- ❑ Upset rates have been calculated for configuration memory, block RAM and the POR and SelectMAP SEFIs
- ❑ Dynamic testing has shown the effectiveness and value of TMR and partial reconfiguration used in conjunction
- ❑ Continuing dynamic testing for more complex designs and other Virtex II capabilities (i.e. I/O standards, digital clock managers (DCM) , etc.) is scheduled for Texas A&M cyclotron, Aug. 23, 2003.