

Band-to-Band Tunneling (BBT) Induced Leakage Current Enhancement in Irradiated Fully Depleted SOI Devices

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Abstract— We propose a model, validated with simulations, describing how band-to-band tunneling (BBT) affects the leakage current degradation in some irradiated fully-depleted SOI devices. The dependence of drain current on gate voltage, including the apparent transition to a high current regime is explained.

Index Terms—fully depleted SOI, total ionizing dose, high current regime, GIDL, band-to-band tunneling.

I. INTRODUCTION

THE introduction of the insulating buried oxide layer makes silicon-on-insulator (SOI) devices more susceptible than bulk transistors to total ionizing dose (TID) damage in ultra deep submicron processes (≤ 130 nm) [1-8]. This is because TID causes positive charge to be trapped in the buried oxide as evidenced by the negative shift in the back-gate I - V characteristics [1-6]. The positive trapped charge can invert the back-channel interface of n -channel transistors, forming a conductive path that leads to an increase in drain current [3-5]. As dose levels increase, for NMOS devices with floating bodies, the drain current tends to increase as the gate bias becomes more negative. For some technologies, at high doses the current increases abruptly and may enter a high current condition that has been described as a “latched” state [1, 2, 5-6]. The precise underlying mechanism of this effect is still a matter of debate, particularly the role of impact ionization [1, 2, 5-6].

Fig 1 shows an example of the variations in I_d vs. V_{gs} characteristics with total dose for an NMOS transistor, fabricated in a 0.25 μm fully depleted (FD) SOI technology at MIT Lincoln Laboratory (HYSOI6) [5]. This transistor is a closed-geometry (edgeless transistor). Thus the increase in leakage current is not caused damage to the STI. As shown on the figure, for doses below 1 Mrad, the data show an increase in the drain current as the gate bias becomes more negative. This current increases with dose. This effect is due to gate-induced drain leakage (GIDL). GIDL is created as the high electric field under the gate/drain overlap region generates carriers via band-to-band tunneling (BBT), which transport to the floating body (holes) and drain (electrons) thereby inducing of GIDL current (from band-to-band tunneling (BBT) [7]. The abrupt increase in drain current between 500 krad(SiO_2) and 1 Mrad(SiO_2) has been described as a “total dose latch” mechanism [1, 2, 5-6]. To date, none of the proposed models considered separately or in combination completely explain the observed results [1, 2, 5-6].

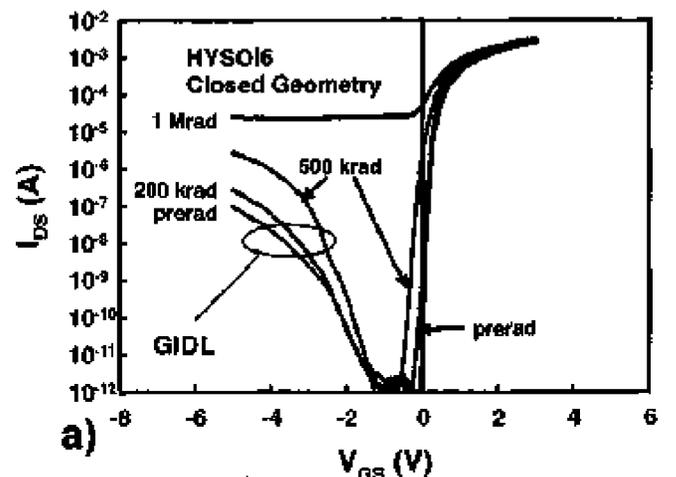


Fig. 1. Experimental results about the total dose effects on the I_d vs. V_{gs} characteristics fabricated in a 0.25 μm FD SOI technology at MIT Lincoln Laboratory (HYSOI6) [5].

In this work, we propose a model, validated with simulations, that explains the increases in drain current at

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negative gate biases. Band-to-band tunneling (BBT) is identified as *the* critical mechanism that determines the dependence of drain current on gate-to-drain voltage, including the apparent transition to the high current state.

II. TOTAL DOSE SIMULATION RESULTS: IMPACT OF BAND TO BAND TUNNELING

A. Mechanism for Gate Induced Drain Leakage (GIDL) current: band-to-band tunneling (BBT)

The mechanism responsible for gate-induced drain leakage (GIDL) current in MOSFETs is band-to-band tunneling in the gate-to-drain overlap region, as illustrated in Fig. 2. The combined application of positive drain and negative gate biases result in a high electric field region within the widened drain-body depletion region near the front-gate interface.

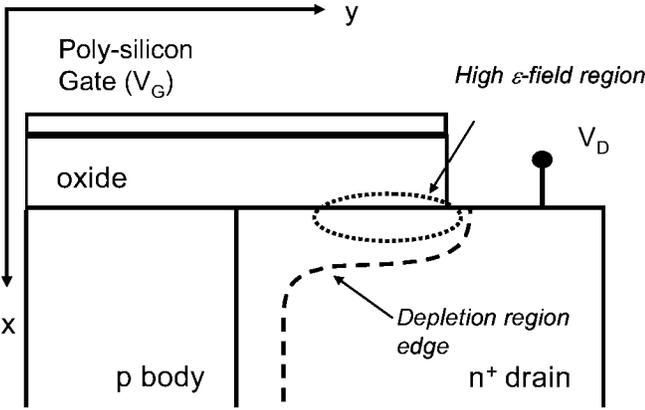


Fig. 2. When the gate voltage (V_G) is significantly lower than the drain voltage (V_D), a large electric field region exists in the drain region, underneath the gate-drain overlap.

When \mathcal{E}_s (the electrical field at the silicon surface) is sufficiently high and band bending is larger than the energy band-gap, E_g , the band-to-band tunneling (BBT) process can be initiated. A first order expression for the minimum surface electric field required for BBT is:

$$\mathcal{E}_s \approx \frac{-V_{GD,\min} - \frac{E_g}{q}}{3T_{ox}}, \quad (1)$$

where T_{ox} is the gate oxide thickness in the overlap region, $V_{GD,\min}$ is the smallest magnitude gate-to-drain voltage required to induce sufficient band-bending, and the scale factor, 3, accounts for the dielectric constant ratio between Si and SiO₂.

Physically, BBT is characterized by electron tunneling across the silicon bandgap from the inverted drain sur-

face across the Si bandgap into the quasi-neutral drain, as illustrated in Fig. 3. Valence band holes, left behind by the tunneling process, are then free to transport into the body region of the device.

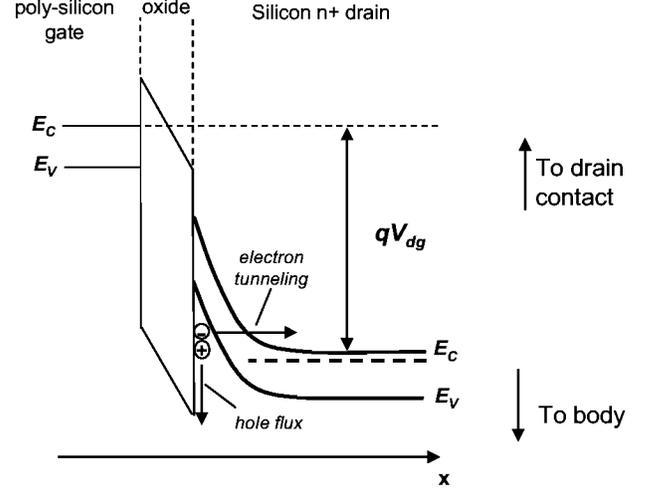


Fig. 3. Illustration of the band-to-band tunneling process across the drain-body junction in a n-channel fully depleted SOI transistor. Diagram indicates that for a high electric field condition, valence band electrons will eventually tunnel into the conduction band. Electron will transport from body to drain [10]. Hole will transport into the body.

Mathematically, the BBT process can be modeled as field dependent carrier generation rate in the high field region, i.e.,

$$G_{BBT} = A \mathcal{E}^\sigma \exp\left(-\frac{B}{\mathcal{E}}\right), \quad (2)$$

where A is a constant related to the effective mass of the electron ($4 \times 10^{14} \text{ V}^{-2} \cdot \text{s}^{-1} \text{ cm}^{-1}$), σ is the transition constant (≈ 2.5 for Si), \mathcal{E} is the magnitude of the local electric field, and B is the tunneling probability constant ($\approx 30 \text{ MV/cm}$) [7]. Figure 4 gives a schematic representation of the two current densities ($J_{p,BBT}$ for holes and $J_{n,BBT}$ for electrons) resulting from the BBT-induced carrier generation (Eq. 2).

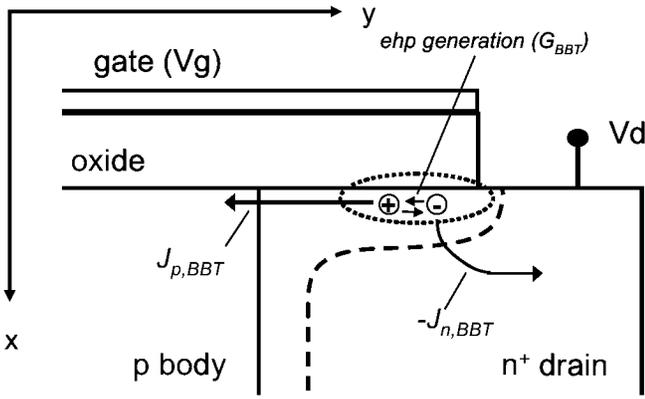


Fig 4. When the gate voltage (V_G) is significantly lower than the drain voltage (V_D), a large electric field (E_x) exists in the drain region, underneath the gate-drain overlap.

It should be noted that not all FD SOI transistors exhibit susceptibility to BBT. Previous studies have shown that gate-induced BBT is a strong function of the drain doping below the gate overlap [10]. However, for those devices that exhibit BBT prior to irradiation, GIDL current is primarily proportional to the electron current component, $J_{n,BBT}$. It will be shown that after radiation exposure, the primary impact of BBT on increased drain current for negative V_{GD} , becomes more related to the hole current density, $J_{p,BBT}$, which alters the carrier concentration and potential in the floating body. This hole current density into the body can be expressed as

$$J_{p,BBT} = q \int_W G_{BBT} dx \cong qWG_{BBT}, \quad (3)$$

where W is the width of the high field region [7].

B. Simulation of TID effects in n-channel FD SOI transistors with/without the band-to-band tunneling.

To study the impact of BBT on the total dose response of the I_d vs. V_{gs} characteristics, we performed 2D simulations on a FD SOI n-channel transistor. The device simulator used was ATLAS, from the SILVACO suite of TCAD simulation tools. The transistor characteristics are as follows: gate length = 0.1 μm , buried oxide thickness = 100 nm, gate oxide thickness = 2 nm, and silicon film thickness = 20 nm. The floating body had uniform doping of $1 \times 10^{16} \text{ cm}^{-3}$, the source/drain doping was $1 \times 10^{18} \text{ cm}^{-3}$ and lightly doped drain (LDD) regions were included.

A first set of simulations was performed to compare the pre-rad and post-rad I_d vs. V_{gs} characteristics without using the BBT model in the simulator. In these simulations, the level of total dose damage was fixed by adding a uniform layer of sheet charge (with a density of $2 \times 10^{12} \text{ cm}^{-2}$) at the interface between the thin silicon film

and the buried oxide as previously done in [5]. The drain voltage was 1 V and the source and backgate were grounded. The impact ionization model was turned off. Simulation results, shown in Fig. 5, indicate that there is a negative-shift of the I_d vs. V_{gs} characteristics (i.e., a threshold-voltage shift) with increasing dose resulting from a coupling effect between the front and the backgate as previously reported in [6, 14]. Moreover, the results also reveal an increase in backgate leakage as a result of the placement of sheet charge as the backside Si/SiO₂ interface. However unlike the experimental data shown in Fig. 1, the simulation results obtained with trapped charge but without the band-to-band tunneling model do not show the monotonic increase of the leakage current for negative V_{GD} .

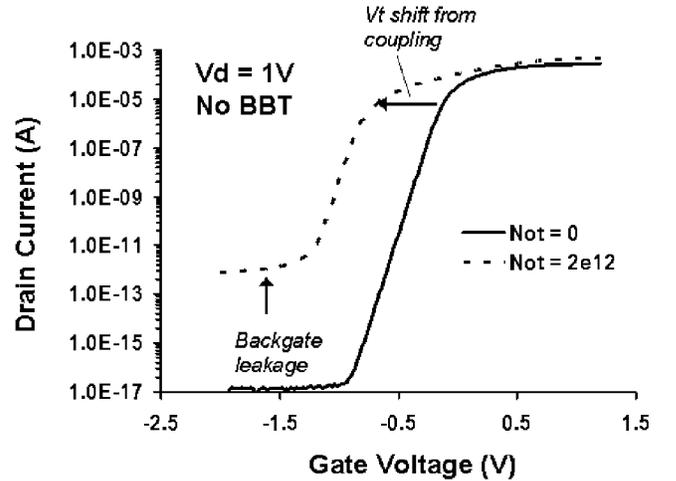


Fig 5. Modeling of TID effects without BBT reproduces the front-gate voltage threshold voltage shift due to the coupling effect between front and backgate. The increase of the backgate leakage with total dose is illustrated. No BBT has been included.

In order to observe the impact of BBT on an FD SOI device degraded by total dose, the tunneling model, expressing the field dependent generation rate in Eq. 2, was turn on during device simulation. The back interface charge density was fixed at $2 \times 10^{12} \text{ cm}^{-2}$ for this simulation. All terminal bias conditions were the same as the first simulation set and the impact ionization model was turned off. The resulting I_d vs. V_{gs} characteristics are shown in Fig. 6 for device simulations with identical levels of buried oxide charge ($2 \times 10^{12} \text{ cm}^{-2}$) with and without BBT model activated.

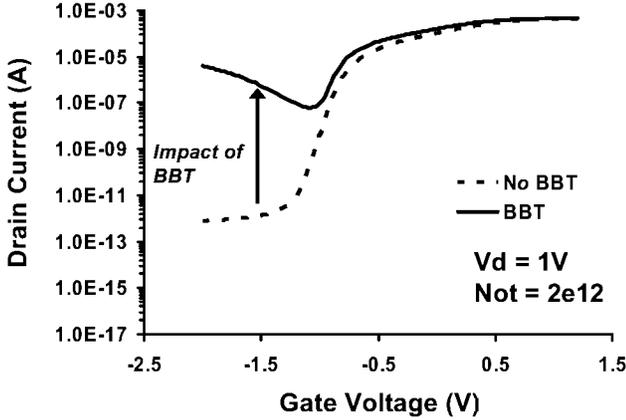


Fig. 6. Simulated FD SOI I_d vs. V_{gs} characteristics for a charge trapped density of $2 \times 10^{12} \text{ cm}^{-2}$ with and without BBT. Impact ionization is turned off and $V_D = 1 \text{ V}$.

The results clearly indicate that BBT must be included to simulate the experimentally observed drain current increase (Fig. 1) for increasingly negative gate-to-drain voltages.

Further simulations were conducted to examine the impact of increased radiation exposure on a FD SOI device. These simulations were performed by increasing the buried oxide trapped charge density values at the silicon-on-insulator interface. The BBT model was turned on and the bias conditions were the same as the previous simulations. The impact ionization model was turned off. The results are plotted in Fig. 7 and show that drain current increases exponentially with charge density up to $8 \times 10^{11} \text{ cm}^{-2}$. For charge densities $\geq 5 \times 10^{12} \text{ cm}^{-2}$, the drain current has entered the high current regime, characterized in previous studies as a “total dose latch” [1, 2, 5 -6]. However, since this high current does not seem to require avalanche (e.g., impact ionization) and bipolar feedback processes, it is unlikely to be a latch effect. As will be discussed in subsequent sections, the likely mechanism for the high current characteristics observed in this study is strong inversion along the back-side interface caused by the combined effect high positive trapped charge densities in the BOX and band-to-band tunneling processes.

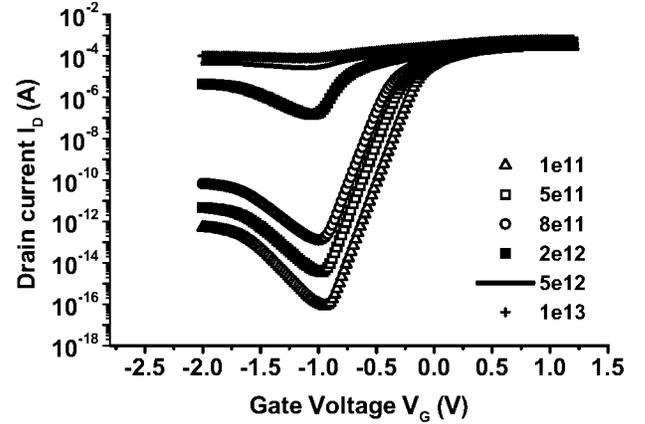


Fig. 7. Simulated FD SOI I_d vs. V_{gs} characteristics for trapped charge densities of 10^{11} , 5×10^{11} , 8×10^{11} , 2×10^{12} , 5×10^{12} and 10^{13} cm^{-2} with band-to-band tunneling. Impact ionization is turned off. $V_D = 1 \text{ V}$

As the simulation results shown in Fig. 7 suggest, BBT provides an explanation of the increase in drain current observed at negative gate biases. In the next two sections, we first discuss the limitations of previous explanations about the dependence of drain leakage current degradation on gate voltage as well as the transition to a high current regime, i.e., previously characterized as “total dose latch”. Then, a new model is described to explain this effect.

III. DISCUSSION OF MECHANISM

There is strong evidence that simple back channel inversion caused by trapped charge buildup in the BOX is a limited explanation for the high-current state at negative gate bias, as suggested in [5]. One important point is that the onset of the high current state depends strongly on gate length, as shown in [6]. It was reported that a gate length reduction from $0.25 \mu\text{m}$ to $0.2 \mu\text{m}$ is sufficient to cause the drain current to increase four orders of magnitude at a total dose of 100 krad (SiO_2). If increased drain current were only due to back channel inversion, the current would scale roughly with $1/L$ which clearly is not large enough to explain any “sudden” increase. A second reason offered by Paillet et al. [2] is that for “deca-nanometer” FD SOI devices, “total dose latch” was observed in both the front-gate and back-gate I-V sweeps. If drain leakage were only due to back-channel inversion from N_{ot} buildup, high negative biases on the back-gate would be sufficient to “overcome” the BOX charge and therefore would suppress leakage current. However, this was not observed in these aggressively scaled parts. A third reason to which some researchers point for doubting the “simple” model is that it seems somewhat questionable that the charge-induced back channel inversion would be enough to

trigger transition to the high current regime. A trigger of this sort would suggest the existence of secondary process that either initiates a high gain condition, a feedback, or a suppression of a response control mechanism. Impact ionization is often suggested as a secondary mechanism that when coupled with trapped charge buildup in the box would explain “total dose latch”.

Researchers advocating impact-ionization as the key triggering mechanism offer the following explanation. Electrons diffusing to the drain along the weakly inverted back-channel (arising as a result of TID-induced N_{ot} buildup in the BOX) generate electron-hole pairs near the drain junction as a result of impact ionization. The generated holes drift into the body as a result of the high electric field at the drain body junction. These holes transport back to the source where they reduce the potential barrier across the source-body junction. This causes electrons from the source to be back-injected into the body and transport to the drain where they contribute to an increase in drain current or cause more impact ionization, leading to a positive feedback condition that further increases the drain current [2, 5, 6]. This explanation is very plausible in light of the fact that this type of “parasitic bipolar” response would be amplified significantly by reductions in gate length as discussed in [6]. However there are strong pieces of evidence that call the impact ionization theory into question as well. First, impact ionization at the drain depends strongly on the presence of an electric field large enough to trigger avalanche. This field would likely require a large drain bias relative to body potential, i.e., the high field condition required for impact ionization typically requires a high drain bias. However, results presented in both [5, 6] showed that high levels of leakage current could arise even with low drain biases for which the probability of impact ionization would be very small.

Moreover, the fact that our simulations show large increases in leakage current without the implementation of impact ionization models provides further evidence for doubting that impact ionization completely explains the observed response. It should be noted that we are not claiming the impact ionization can not contribute to the response. Indeed, measurements taken on irradiated parts fabricated in slightly different FD SOI technologies exhibit “latching” and hysteresis which are possible signatures of avalanche mechanisms. However some irradiated FD SOI transistors responses, including those shown in Fig. 1, do not exhibit these signatures [2, 3].

Given the clear limitations in the “simple” N_{ot} -induced back channel inversion theory or the coupling of back-channel inversion with an impact ionization-triggered mechanism, researchers have identified another potential explanation for radiation-induced leakage that postulates the cause as being related to a non-uniform build-up of

trapped charge in the buried oxide [2]. While non-uniform charge build-up along the back-side interface is highly plausible, especially owing to the high variability in the electric field in the near interfacial BOX, the complexity of this explanation makes it somewhat unappealing. Moreover, the fact that our simulations utilizing a uniform sheet charge model effectively reproduce the trends observed in the data further discounts the charge non-uniformity hypothesis. Indeed the model implemented in our simulation needs only to have uniform charge buildup in the BOX, coupled with BBT, to simulate the leakage current dependence on both TID and gate bias. In the next section, we provide a more detailed description of a proposed model that shows how the electrostatic effects of N_{ot} buildup in the BOX and gate-voltage-induced band-to-band tunneling combine to impact the negative gate bias leakage current response in irradiated FD SOI floating body devices.

IV. PROPOSED MODEL

The explanation proposed here is based on uniform charge buildup in the BOX, coupled with BBT, to describe the drain current dependence on both TID and gate-to-drain bias. It correctly describes the leakage current characteristics at both low and high doses, without requiring the inclusion of impact ionization. The processes related to the proposed model are summarized in Fig. 8, which illustrates an n-channel FD SOI MOSFET cross-section. In this figure, the device source and back side contacts are grounded while the drain bias and gate bias are varied. These conditions represent the bias configuration used when characterizing device response after radiation exposure, i.e., V_D is set to a positive voltage, 1 V in the case of the simulated curves in Fig. 3, while V_G is swept between -2 V and 1.25 V. The figure also illustrates the TID-induced buildup up of charge in the buried oxide as a sheet of positive charge at the Si-BOX interface. The arrows in the Si layer represent the fluxes of holes and electrons that result from negative bias applied to the gate and positive charge buildup in the BOX.

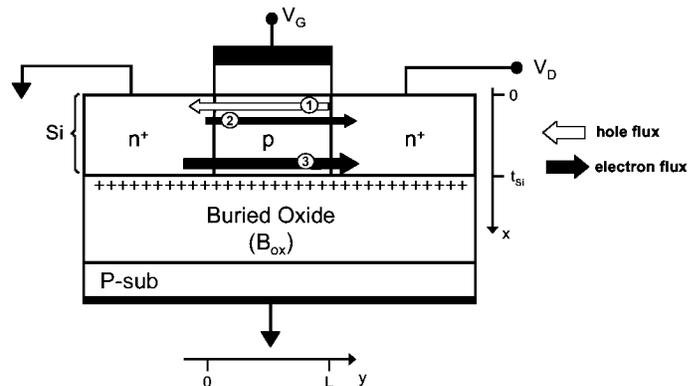


Fig. 8. Proposed model describing the three current processes related to drain current degradation with total dose in a FD SOI transistor.

Process 1: The arrow labeled “1” represents the hole flux, i.e., current density ($J_{p,BBT}$), induced by band-to-band tunneling. As discussed in section IIA, $J_{p,BBT}$ arises from an increase in BBT-induced carrier generation in the high-field region below the gate-drain overlap. Fig. 9 plots the generation rate within this region (in the y-direction) for simulations performed with 1) $N_{ot} = 2 \times 10^{12} \text{ cm}^{-2}$ and no BBT model, 2) $N_{ot} = 0 \text{ cm}^{-2}$ and with the BBT model, and 3) $N_{ot} = 2 \times 10^{12} \text{ cm}^{-2}$ and with the BBT model. For these simulations, the drain is fixed at 1v while the gate is -1.5 V. The figure illustrates that even with trapped charge at the BOX interface, simulations performed without BBT exhibit a negligible rate of carrier generation compared to the simulations for which BBT is modeled. Moreover, when BBT is employed, the presence of $N_{ot} (= 2 \times 10^{12} \text{ cm}^{-2})$ at the BOX interface increases carrier generation by nearly two order of magnitude over simulations without trapped charge. These results suggest that not only does excess carrier generation via BBT depend on electric field (Eq. 2), but moreover the field is altered (increased) by the presence of trapped charge in the buried oxide. Eq. 2 can then be rewritten as

$$G_{BBT}(N_{ot}) = A \varepsilon (N_{ot})^\sigma \exp\left(-\frac{B}{\varepsilon(N_{ot})}\right), \quad (4)$$

where now BBT-induced generation reflects a functional dependence on radiation damage in the buried oxide. Through Eq. 3, one observes that the hole flux (process 1) into the body via BBT is thus significantly impacted by radiation exposure.

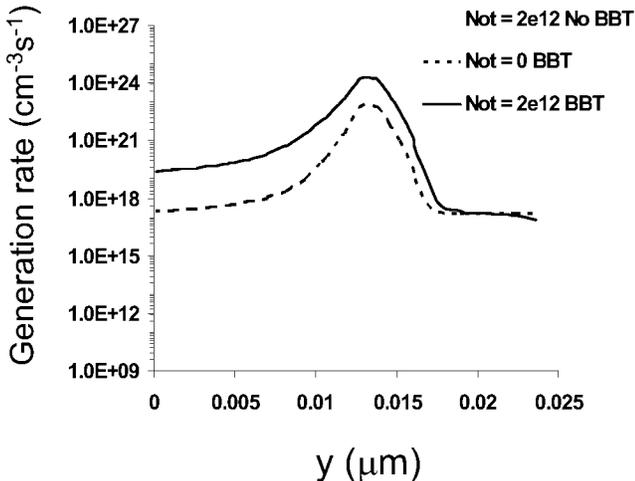


Fig. 9. Generation rate within high-field region (in the y-direction) for simulations performed with 1) $N_{ot} = 2 \times 10^{12} \text{ cm}^{-2}$ and no BBT model, 2) $N_{ot} = 0 \text{ cm}^{-2}$ and with the BBT model, and 3) $N_{ot} = 2 \times 10^{12} \text{ cm}^{-2}$ and with the BBT model.

Analysis of the device simulation results indicates that the majority of the BBT-generated holes transports laterally (in the negative y direction) near the top-gate interface. As a result, in steady state, the holes will transport across the body through the source-body junction (at $y = 0$ and $x = 0$), thereby forward biasing the junction, leading to process 2.

Process 2: The arrow labeled “2” represents electron flux near the top-gate surface that arises as a result of back-injection of electrons into the body across the forward-biased body-source junction. Fig. 10 plots the electron concentration (in log scale) within the p-type body at the top-gate interface ($x \approx 0 \text{ μm}$) for simulations with and without the BBT model implemented. The BOX interface charge density for these simulation was fixed at $2 \times 10^{12} \text{ cm}^{-2}$, the gate and drain biases were -1.5 and 1 V respectively, and all other terminals were grounded. The electron concentrations decrease monotonically from source to drain for both simulations. This decrease is the characteristic minority carrier gradient for MOS devices biased below threshold with $V_{DS} > 0V$. However, as the figure shows, the electron concentration for the simulation with BBT included is almost five orders of magnitude greater than the simulation without BBT. This excess electron concentration is due to the back-injection of electrons from the source in response to the flow of holes across the body-source junction.

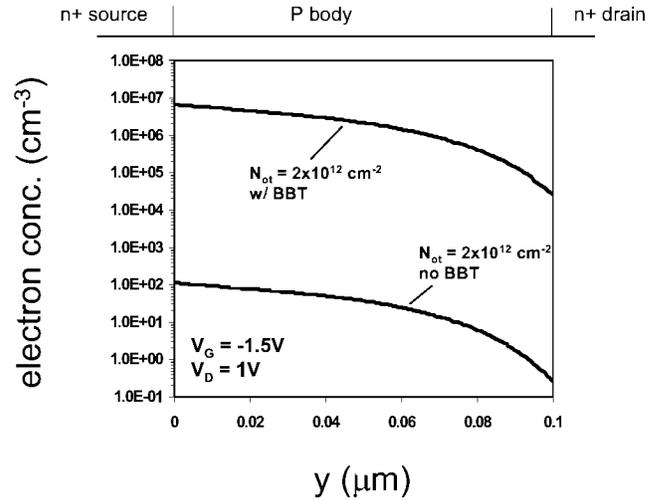


Fig. 10. Electron concentration across the p-type body at the front gate interface for simulations with BOX N_{ot} of $2 \times 10^{12} \text{ cm}^{-2}$ with and without the BBT model implemented

Using the standard diode equation, the electron concentration at the top-gate interface ($x \approx 0$) on the body side of the source-body junction ($y = 0$) can be estimated as:

$$n(x \approx 0, y = 0) \approx \beta \times J_{p,BBT}, \quad (5)$$

where

$$\beta = \frac{1}{q} \frac{W_S N_D}{D_p p_0}, \quad (6)$$

q is electronic charge, D_p is the hole diffusion constant, W_S is approximately the distance between the source-body junction and the source contact, N_D is the source doping concentration (assumed uniform), and p_0 is the hole concentration at ($x \approx 0$ and $y = 0$) [12].

The back-injected electrons will diffuse laterally toward the drain junction (**Process 2** in Fig. 8). If the body is assumed to be quasi neutral in the lateral dimension (i.e., $\varepsilon_y = 0$ V/cm), the top-gate interface electron concentration across the body, from $y = 0$ to L can be approximated as [11]

$$n(x=0, y) \approx \frac{n(x=0, y \approx 0) \sinh\left(\frac{L-y}{L_n}\right)}{\sinh\left(\frac{L}{L_n}\right)}, \quad (7)$$

where L is the gate length and L_n is the diffusion length for electrons. With appropriately chosen parameters, the electron distribution of the model in Eq. 7 compares well to the results of the device simulation (Fig. 11, linear scale). As Eq. 3, 5, and 7 demonstrate, the electron concentration at the front-gate interface increases linearly as a function of the BBT-induced generation in the drain.

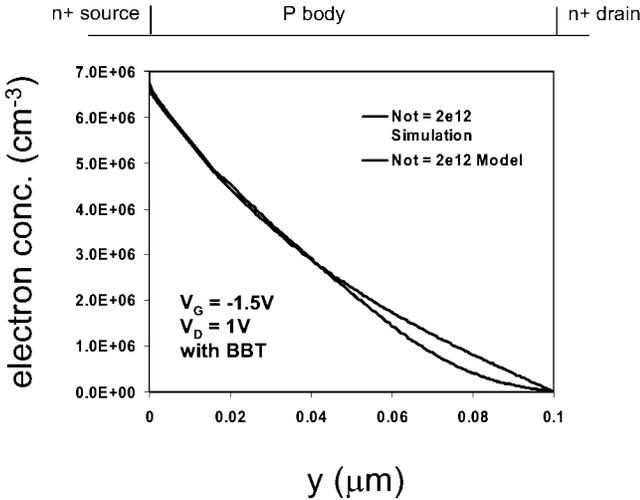


Fig. 11. Electron concentration across the p-type body at the front gate interface for simulation and model with BOX Not of $2 \times 10^{12} \text{ cm}^{-2}$ with the BBT model implemented.

Process 3 (shown in Fig. 8) is the electron flow along the back-gate interface that arises as a result of the charge buildup in the BOX and, as we shall demonstrate,

negative gate biases applied to the front gate. A general expression for the back-gate electron current is

$$I_{n3} = \mu \frac{W}{L} \int_0^{V_{ds}} [-Q_n(V)] dV, \quad (8)$$

where μ is the electron mobility, W is the n -channel gate width, and Q_n is the electron charge in the body (sometimes denoted as inversion layer charge in bulk applications) [2]. Eq. 8 shows that an increase in Q_n along the channel will increase the magnitude of back-channel electron current in an FD SOI device, at a given lateral location, y , in the body:

$$\int_0^{t_{Si}} n(x, V(y)) dx = -q \int_0^{t_{Si}} n(x=0, V(y)) \exp\left(\frac{q\psi(x, V(y))}{kT}\right) dx, \quad (9)$$

where kT is the thermal energy and ψ is the potential in the Si film. At a fixed y , the change in potential from 0 to x can be expressed as

$$\psi(x) - \psi(x=0) = \frac{kT}{q} \ln\left(\frac{n(x)}{n(x=0)}\right). \quad (10)$$

Thus, an exponential increase in the electron concentration corresponds to a linear increase in the potential. Fig. 12 plots the electron concentration in the Si from the front-side ($x = 0$) to the back-side ($x = t_{Si} = 20$ nm) for a BOX sheet charge density (N_{ot}) of (0 and 10^{12} cm^{-2}) and gate biases of (-1.2 V and -1.5 V). As the figure indicates, for a gate voltage of -1.2 V, an increase of N_{ot} from 0 to 10^{12} cm^{-2} significantly increases the electron ratio and therefore, by Eq. 10, increases the potential change across the silicon layer. A comparison of the two curves also reveals that the addition of N_{ot} by itself will also increase the electron concentration of the front gate. The combination of the increase in these two terms, i.e., $n(x=0)$ and $\psi(x)$, increases the electron charge in the body and through Eq. 10, the back-channel electron current. These two curves demonstrate the critical impact of BOX charge on drain current in FDSOI devices.

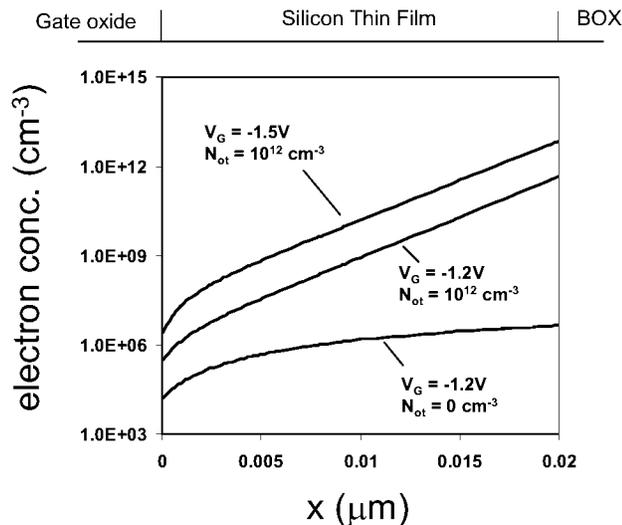


Fig 12. Simulated electron concentration in the Si film from the front-side ($x = 0$) to the back-side ($x = t_{Si} = 20$ nm) for BOX sheet charge densities (N_{ot}) of 0 and 10^{12} cm^{-2} and gate biases of -1.2V and -1.5V. $V_D = 1$ V and impact ionization is turned off

These effects are consistent with the “simple” model originally proposed by Schwank [5]. However, the third carrier profile given in Fig. 12, obtained by fixing N_{ot} at 10^{12} cm^{-3} and reducing the gate voltage to -1.5 V, clearly shows how a negatively biased gate couples with N_{ot} to further enhance back-channel current. As the third curve illustrates, the application of the gate voltage leads to an even greater increase in the electron concentration at the front gate; thereby further increasing electron charge and back-channel current. The reason for this increase in the front channel electron concentration is BBT current, as explained above.

V. CONCLUSION

A new analytical model validated with 2D simulation demonstrates that band-to-band tunneling is the critical mechanism responsible for the increase of leakage current (drain current) in irradiated fully depleted SOI transistors. It demonstrates that the drain current dependence on TID and negative gate bias results from the combination of BBT and charge buildup in the BOX, including the transition to the high current state.

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