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Testing and Qualifying Linear Integrated Circuits for Radiation Degradation in Space

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Abstract – This paper discusses mechanisms and circuit-related factors that affect the degradation of linear integrated circuits from radiation in space. For some circuits there is sufficient degradation to affect performance at total dose levels below 4 krad(Si) because the circuit design techniques require higher gain for the pnp transistors that are the most sensitive to radiation. Qualification methods are recommended that include displacement damage as well as ionization damage.

I. INTRODUCTION

Total dose effects in linear integrated circuits have been studied in great detail during the last ten years [1-11]. Much of the work has concentrated on enhanced damage at low dose rate (ELDRS), using elementary comparators, op-amps and test structures to determine how the different types of transistors used in linear integrated circuits are affected by ionizing radiation at the low dose rates that are encountered in space. Although a great deal is known about how individual transistors are affected by radiation, new integrated circuits have been developed that can operate over a wide range of operating conditions with higher performance and improved specifications compared to the older types of linear ICs that have been the focus of most of the work. The complexity of these designs also impacts radiation performance, making it far more difficult to characterize radiation damage compared to the relatively simple circuit designs that are typical of older circuits.

This paper discusses these issues for those classes of circuits, developing recommendations for testing and qualification for the natural radiation environment in space. The paper only considers degradation from ionizing radiation and displacement damage, not single-event transients [12-14].

 Manuscript submitted September 9, 2005.

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The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA).

One of the consequences of design evolution is much wider variability in the sensitivity of linear ICs in space. Fig. 1 shows the response of two different channels of an instrument that uses a low-dropout regulator during the first 140 days of operation in a 705 km, 98 ° earth orbit (the “step” at 35 days is due to temperature and a change in operational conditions, not radiation damage). Despite the very low total dose level, changes in output voltage are large enough to affect the application, requiring frequent re-calibration of the instrument in which the circuit is used. With the higher load condition, the changes will be large enough after about 3 years to seriously affect instrument performance.

In principle there is nothing new here; this device used the same types of internal transistors that have been the focus of earlier studies. However, unlike older circuits (LM111, LM124 and LM139) that used more conservative designs, the low dropout regulator depends directly on the gain of a lateral pnp transistor for its operation. The result is a circuit that is extremely sensitive to degradation from space radiation, particularly when the load is close to the rated maximum.

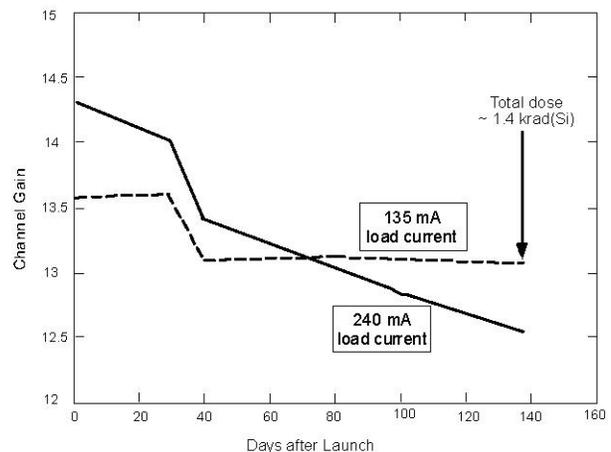


Fig. 1. Change in channel gain of an instrument with a low-dropout regulator in a 705 km, 98 ° earth orbit.

II. TRANSISTOR PROPERTIES

Although advanced processes are available for linear integrated circuits, the majority of such devices are made with an older process that provides design flexibility along with very low fabrication cost. This “standard linear” process is intended for low cost circuits that can operate at power supply voltages up to ± 18 V. Several different types of internal transistors are available with that process, along with some additional transistor types that can be obtained by adding extra processing steps. Their basic properties are shown in Table 1.

Table 1. Some Properties of Transistor Types Used in Bipolar Linear Integrated Circuits

Transistor Type	Approximate dose rate where degradation is no longer affected by dose rate	Typical emitter-base oxide thickness in processing	Processing
Vertical npn	1 rad(Si)/s	10 – 15 nm	Standard
Super- β npn	0.2 rad(Si)/s	15 – 20 nm	Requires extra steps
Substrate pnp	5 mrad(Si)/s	70 – 90 nm	Standard
Lateral pnp	5 mrad(Si)/s	70 – 90 nm	Standard
JFET	~ 1 mrad(Si)/s	~ 130 nm	Requires extra steps

The basic process is optimized for npn transistors. It also provides lateral and substrate pnp transistors with no additional processing steps, with lower performance – reduced gain and much lower frequency response - that is still acceptable for many linear designs. The approximate thickness of oxides over the emitter-base region – the critical region for charge trapping that affect gain - is shown in the third column of Table 1. The oxide thickness is much lower for npn transistors.

Fig. 2 shows the cross section of a substrate pnp transistor. The oxide over the emitter-base region is grown for the initial processing step to create the p⁺ isolation regions. It must be thick enough to avoid penetration of boron during subsequent processing steps. The same oxide layer is present in the lateral pnp transistor, but not over the emitter-base region of npn transistors.

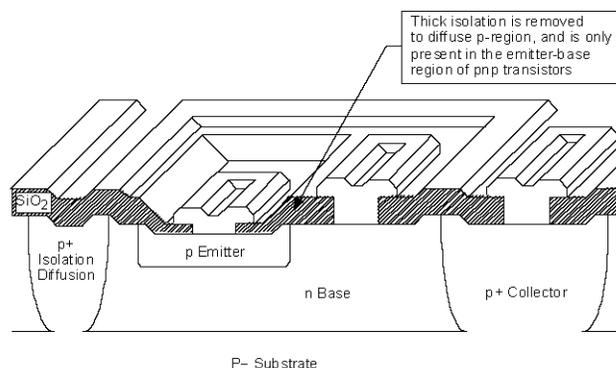


Fig. 2. Diagram of a substrate pnp transistor showing the thick oxide over the emitter-base region.

Circuits that use super- β or JFET structures require additional processing steps, with thicker isolation oxides to prevent boron penetration during the additional high-temperature processing steps. Consequently when either of those structures is used it affects the properties of other transistor types. The thicker oxide can cause such circuits to remain sensitive to dose-rate effects below 5 mrad(Si)/s, and may also increase the sensitivity of pnp transistors to total dose damage because of increased charge trapping.

III. LOW-DOSE RATE DAMAGE IN MODERN CIRCUITS

A. Basic Considerations

The increased sensitivity of some types of bipolar transistors at low dose rate was first reported by Enlow, *et al.* in 1991 [14]. They showed that the gain of npn transistors was approximately twice as great when tests were done at low dose rate, with the dose rate dependence leveling out at about 1 rad(Si)/s. Many subsequent studies on linear IC processes have shown that the damage at low dose rates can be a factor of ten or more higher for low dose rates compared to high dose rates.

If we only had to deal with basic transistors this problem could be easily dealt with by simply adding additional margins to total dose test results at high dose rate. However, linear integrated circuits depend on the interaction of several different types of transistors (see Table 1) which may be affected differently by the enhanced damage that occurs at low dose rate. The relative increase in damage that occurs in pnp transistors with thick emitter-base oxides can be considerably higher than the enhanced damage in npn transistors. This often introduces different circuit failure mechanisms when tests are done at very low dose rates because

the relative damage of different types of internal transistors does not “track” with dose rate. In extreme cases the circuit failure level at low dose rate can be as much as two orders of magnitude lower compared to tests at high dose rate [6]. Such extreme differences in failure level occur because acceptable circuit performance is related to internal transistor gain in a highly nonlinear way.

B. Input Stage Degradation: Bipolar Input Transistors

Input parameters are often the most sensitive characteristics of a linear integrated circuit when it is degraded by radiation. Input bias currents of older circuits such as the LM111, LM124 and LM139 depends directly on the gain of a basic transistor, usually a substrate pnp. If we assume that the emitter current of the input transistors is unaffected by radiation, then the change in input bias current can be used to determine the effect of radiation on the gain of the input transistor.

This characteristic has been used for many years to evaluate the performance of internal transistors, including evaluation of the relative damage that is produced at different dose rates. Fig. 3 shows an example for an LM124 op-amp. For three of the irradiation conditions the input bias current increases linearly with total dose, allowing us to determine the relative damage of the input transistor at different dose rates. At 5 mrad(Si)/s the damage is about six times higher than at 50 rad(Si)/s. However, at lower dose rates the situation is more complex, even at the relatively low total dose levels where these experiments were done. Unlike the results for the other three dose rates the data at 2 mrad(Si)/s becomes superlinear above 5 krad(Si). This is caused by the interaction of other transistors within the input stage, which causes the emitter current of the input substrate pnp transistor to change during irradiation. This is an excellent example of the way that circuit factors introduce nonlinear behavior, even in circuits with simple input stage designs.

Many new linear designs use a compensated input stage, where a current source -comprised of lateral pnp current mirrors - nearly compensates the base current of the npn transistors used at the input stage, reducing the input bias current while allowing the npn transistors to operate at relatively high currents. Fig. 4 shows a representative circuit.

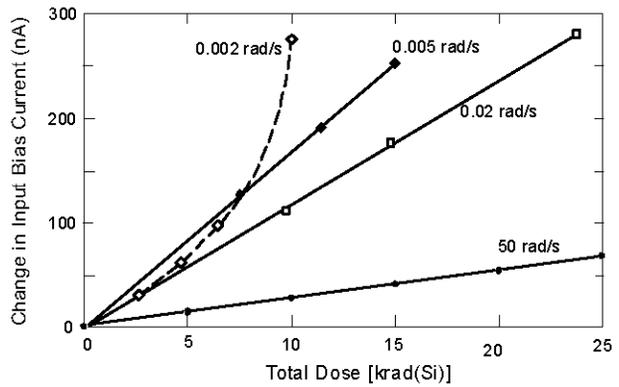


Fig. 3. Change in input bias current of an LM124 op-amp at various dose rates.

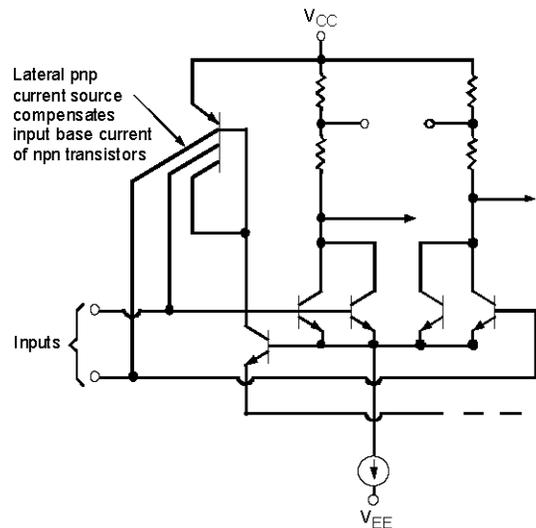


Fig. 4. Diagram of a compensated input stage using pnp current mirrors.

Although this circuit technique reduces input bias current by several orders of magnitude, circuits that use it often have highly nonlinear responses to total dose, as shown in Fig. 5 for the OP-97 op-amp. At low total dose levels, the input bias current increases slightly due to degradation of the npn input transistor. Although the lateral pnp transistor is inherently more sensitive to ionization damage, the current mirror circuit depends on the common-base gain, α , ($\alpha = h_{FE}/h_{FE} + 1$), which is relatively unaffected until h_{FE} falls below 10. Once the gain falls below 10, the mirror current changes very rapidly. When the mirror current decreases, the input current reverses sign, and changes in a highly nonlinear manner, as shown in Fig. 5.

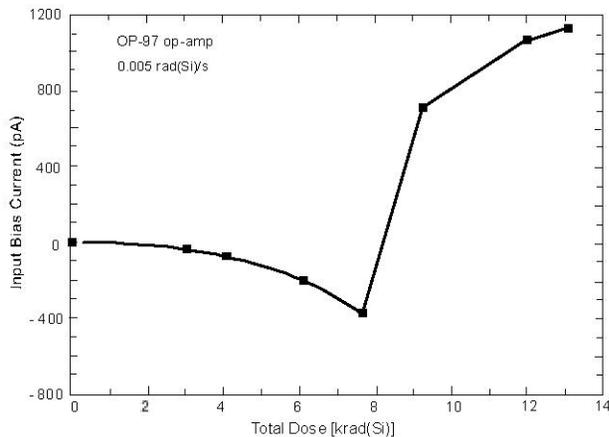


Fig. 5. Degradation of input bias current of an OP-97 op-amp showing the extreme non-linearity that occurs for compensated input stages.

This sign reversal occurs at a relatively low total dose level. When it occurs, the input bias current has increased approximately 50 times over the pre-irradiation value. Furthermore, currents at the inverting and non-inverting inputs no longer “track”, causing very large changes in input offset current. The total dose level at which this sign reversal occurs varies more than a factor of two for different devices from the same date code.

The OP-97 can be used over a wide range of power supply voltages. The total dose level at which the sign reversal occurs is more than a factor of two higher when the device is electrically tested with power supply voltages of ± 12 V compared to results at ± 2.5 V because the internal current sources are slightly dependent on power supply voltage. Consequently radiation tests that evaluate the device with higher power supply voltage will seriously overestimate the radiation level for acceptable performance with lower power supply voltage. For circuits with this type of compensated design it is necessary to include electrical tests at several different power supply conditions in order to overlap the wide range of power supply voltages that are possible. In most cases a low power supply voltage is the worst-case condition.

In nearly all cases input offset voltage remains very low for linear circuits with bipolar input stages, even for devices with very small specification limits. To first order, input offset voltage depends on the mismatch in collector current of the first and second amplification stages. Fig. 6 shows how input bias current and input offset voltage are degraded for a micropower op-amp, tested at 0.01

rad(Si)/s. Despite the relatively large changes that occur in I_b , input offset voltage changes very little.

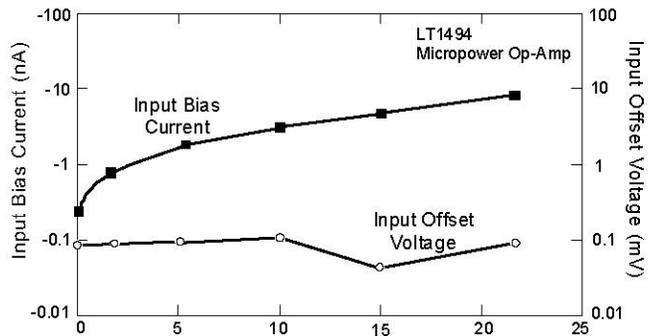


Fig. 6. Degradation of input bias current and input offset voltage for a micropower op-amp.

Although not shown in the figure, catastrophic failure occurs for the LT1494 at total dose levels between 15 and 32 krad(Si). The device shown in Fig. 6 continued to function at 22 krad(Si), but several other devices in the test group stopped functioning at 15 krad(Si). Devices that failed at the lowest radiation level had much lower initial values of power supply current, and also exhibited larger decreases in power supply current after irradiation compared to the devices from the same lot that continued to operate at higher radiation levels. Thus, power supply current is an important diagnostic parameter for some types of linear integrated circuits.

C. Input Stage Degradation: JFET Input Transistors

Op-amps with JFET input stages have very different failure modes from conventional op-amps with bipolar inputs. The JFET input effectively masks the operation of bipolar devices within the circuit that are ultimately responsible for radiation degradation. The parameter that is typically the most sensitive to radiation damage is input offset voltage, which, as discussed earlier, changes very little for linear circuits with bipolar input stages. Older results for the OP-42 op-amp show extreme sensitivity to dose-rate effects. Parametric changes continue to increase as the dose rate is reduced. Dose rates of approximately 1 mrad(Si)/s are required before the sensitivity to dose rate levels off. The total dose level for parametric changes of 5-10 mV – relatively large changes in that critical parameter – is approximately two orders of magnitude lower for tests at very low dose rate compared to results at high dose rate [6].

In addition to the strong influence of the ELDRS effect, the large increase in V_{os} for op-amps with JFET inputs also has a very strong dependence on electrical measurement conditions. This is shown in Fig. 7, which plots the change in V_{os} for an AD823 op-amp that was irradiated to 22 krad(Si) at 5 mrad(Si)/s as a function of the total power supply voltage. Very large changes occur for power supply voltages $> \pm 5$ V, but the effect essentially disappears for lower power supply conditions.

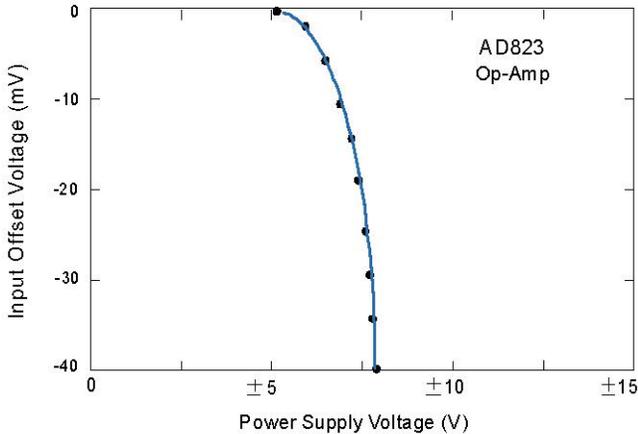


Fig. 7. Input offset voltage for the AD823 op-amp vs. power supply voltage during post-irradiation measurements. The very large increases only occur for differential power supply voltages above ± 5 V.

Thus, for devices with JFET input stages the worst radiation damage occurs with high power supply voltage conditions. This is the opposite condition for maximum radiation damage in devices with bipolar input stages, where the largest radiation damage usually occurs for low power supply voltage conditions.

D. Output Stage Degradation for Operational Amplifiers

Although most studies of linear ICs have emphasized input parameters, other parameters can also cause circuit failure in specific applications. Fig. 8 compares output sink current degradation for the widely studied LM124 op-amp with the LT1494, a low-power op-amp. Output drive current degradation in the LM124 is relatively low, with little effect on most circuit applications. However, for the LT1494 output stage degradation is very severe, causing the device to become inoperable even at very low load conditions at approximately

20 krad(Si). For that device, output stage degradation is far more important than degradation of input stage parameters (V_{os} , I_B , I_{OS}) that are usually considered the most important parameters for op-amps.

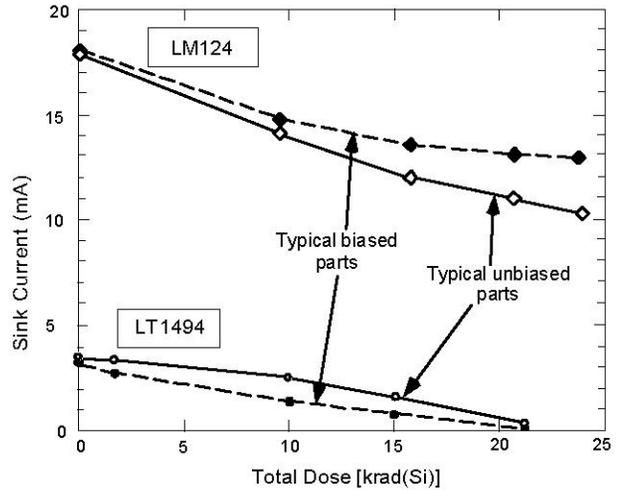


Fig. 8. Output sink current degradation of the LM124, tested at 0.01 rad(Si)/s, and LT1494, tested at 0.005 rad(Si)/s.

Note in addition that more degradation occurs in the output stage of the LT1494 for parts that are biased during irradiation compared to the unbiased case, which is the opposite of what is observed for many linear ICs. Output stage failure takes place at a total dose that is about 40% lower for biased devices. If radiation tests were only done on unbiased parts, the results would overestimate the radiation level at which the part can be used. Radiation testing needs to address both biased and unbiased conditions in order to assess the overall impact of space radiation on these types of devices.

IV. DISPLACEMENT DAMAGE

The environment in space consists of energetic electrons and protons that introduce displacement damage as well as ionization damage. Although displacement damage is usually unimportant for npn transistors in these bipolar processes, the wide base region of substrate and lateral pnp transistors causes them to be sensitive to displacement damage as well as ionization damage [12,13]. Fig. 9 compares high-dose rate tests with cobalt-60 gamma rays with tests at equivalent total dose levels with 50-MeV protons for the LM117 voltage regulator. The difference between these results is caused by displacement damage.

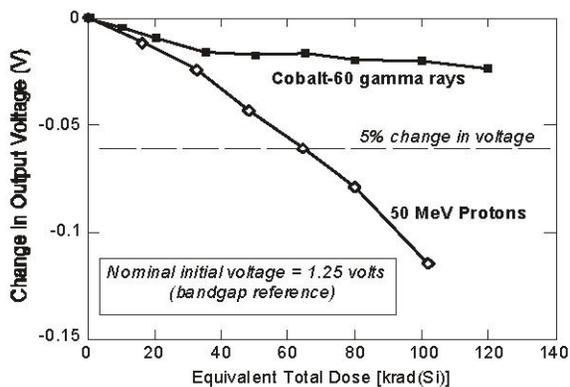


Fig. 9. Degradation of the LM117 voltage regulator to equivalent total dose levels with gamma rays and 50-MeV protons.

The effect of proton damage on circuits that operate at low currents is potentially more important than for the example in Fig. 9. The radiation level at which such effects become important is linked to the specific circuit design as well as to the sensitivity of the pnp transistors to ionization damage. The approximate proton fluence (normalized to 50 MeV) where proton damage starts to become important is 5×10^{10} p/cm² for circuits that rely on lateral pnp transistors for key parameters (at that fluence, the post-radiation gain is approximately 10), but the net impact of such severe gain degradation is circuit dependent.

The damage factor of the substrate input transistor of the LM124 op-amp is compared for 1-MeV equivalent neutrons and 50-MeV protons in Fig. 10. The ratio of the damage factors is 1.9, which is in good agreement with published values for NIEL [15].

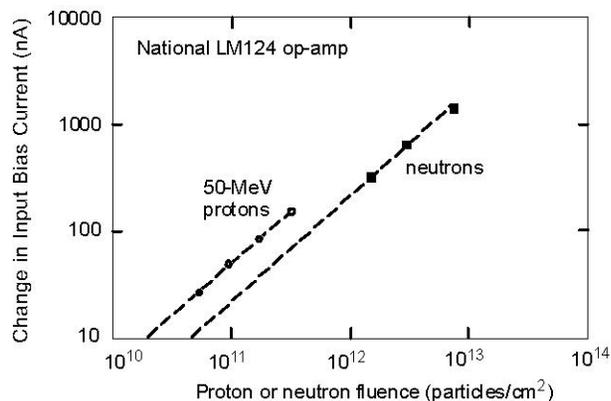


Fig. 10. Change in input bias current for the LM124 from neutrons and protons.

Experimental damage factors for 1-MeV equivalent neutrons are shown in Table 2 for four

types of transistors that are used in linear circuits, along with the neutron fluence that will reduce the initial gain by a factor of two. The damage factors are based on measurements from input current degradation of ICs that use those transistors at the input stage. The damage factors in Table 2 can be used for first-order calculations of the effect of displacement damage on linear ICs, adjusting the damage factor for the NIEL of protons or electrons that correspond to the space environment for a particular spacecraft. This generally requires integrating the damage factor over the particle spectrum.

Table 2. Neutron Damage Factors for Typical Transistors in Linear Integrated Circuits

Transistor Type	Approx. h_{FE}	Damage Factor (cm ² /neutron)	Neutron Fluence for 50% Gain Reduction
npn	300	1.02×10^{-15}	6.5×10^{12}
Super- β	2000	1.82×10^{-15}	5.6×10^{11}
substrate pnp	120	2.82×10^{-14}	5.9×10^{11}
lateral pnp	80	3.40×10^{-14}	5.5×10^{11}

For example, many earth-orbiting spacecraft fly at a high-inclination 705 km orbit. For that case the peak in the differential proton energy spectrum is typically between 20 and 35 MeV (depending on shielding). Integration of the silicon values for NIEL over the proton spectrum yields equivalent neutron fluences of 8.2×10^{10} n/cm² for a 60 mil spherical aluminum shield, and 4.0×10^{10} n/cm² for a 200 mil aluminum shield for a five-year mission. Those fluences are high enough to cause significant damage in three of the four transistor types in Table 2. Missions with higher altitudes will have higher equivalent neutron fluences.

D. Issues for Linear Voltage Regulators

Key Parameters and Failure Modes

Voltage regulators are an important class of linear integrated circuits. Degradation of voltage regulators is more involved than for op-amps and comparators. Some of the characteristics that degrade after radiation, such as minimum start-up voltage, require special measurements [2, 12].

Linear voltage regulators rely on a minimum gain value for the series pass transistor. The output of the regulator will suddenly fall below the regulated output voltage if the series pass transistor

gain falls below that critical value. Thus, nearly all voltage regulators are susceptible to catastrophic failure at high load conditions. New designs that can operate with low differential voltage between input and output may exhibit such failures at very low total dose levels because they use lateral pnp transistors – which are very sensitive to total dose damage – as series pass transistors [16].

In addition to load-dependent catastrophic failure, the internal reference voltage of voltage regulators degrades from radiation. Those changes are relatively small, but may still be important for low dropout regulators.

Mixed Environments

Low dropout regulators are also affected by displacement damage. Table 3 shows calculated values of the combined effects of ionization damage at low dose rate with proton displacement damage. Displacement damage for these devices was measured experimentally with protons; those tests were done at high dose rate because of the prohibitive cost of low dose rate irradiations with protons. The experimental results for protons were combined with experimental results with gamma rays at a dose rate of 0.005 rad(Si)/s assuming that displacement and ionization effects are additive. The additional effects of displacement damage cause the failure level to be significantly lower compared to evaluations based only on ionization damage.

Table 3. Reduction in Failure Level of a Low Dropout Voltage Regulator Due to Displacement Damage from Protons

Load Current (mA)	Failure Level from Total Dose Alone	Failure Level from Combined Environments [1/2 of dose from protons]	Failure Level from Combined Environments [all dose from protons]
250	9.0	6.1	5.0
225	13.2	7.8	7.4
200	18	12	9.8
175	23.5	16	13.3

V. CHARACTERIZATION RECOMMENDATIONS

Characterization of linear integrated circuits is far more complex than implied by basic studies of elementary transistors because of the interplay of circuit design, bias conditions, and displacement damage. Although the importance of using low dose rate irradiations to simulate ELDRS is widely recognized, the other factors are often overlooked during radiation characterization.

Bias conditions during irradiation must include both biased and unbiased samples. The example shown earlier for output current degradation of the LT1494 op-amp illustrates how some parameters may be more degraded for biased devices.

Electrical measurements must extend over a wide range of conditions. This is particularly important for op-amps that have a wide range of power supply voltage. For conventional designs with bipolar input transistors degradation is usually more severe with low power supply voltage. However, the offset voltage failure mode for op-amps with JFET input stages only takes place for higher power supply voltages. The extreme difference in radiation degradation that can occur for some device types under different measurement conditions underscores the importance of including a wide range of power supply conditions during testing. The parameter set must overlap actual use conditions in order to assess radiation damage.

Displacement damage must also be considered, particularly for applications with total dose levels above 15 krad, but it is also important for some types of circuits at lower radiation levels if they use lateral pnp transistors in critical applications. Displacement damage is particularly important for hardened devices that use the wide-base transistors that are typical of mainstream linear technologies. Most of these devices are only hardened against ionization damage, and may fail at much lower levels when displacement damage is taken into account. One such example is the RH1056 op-amp, which meets a 100 krad(Si) requirement for tests with cobalt-60 gamma rays, but fails at about 50 krad(Si) when it is tested with high-energy protons [12].

VI. SUMMARY AND CONCLUSIONS

The results discussed in this paper show that testing and qualification of linear integrated circuits is much more involved for many new types of circuits because the circuit designs are more sophisticated, with more aggressive use of substrate and lateral pnp transistors in critical regions of the circuit compared to older designs. Although gradual degradation occurs for some parameters, many others – including catastrophic failure mechanisms - are strongly nonlinear, exhibiting abrupt changes once the gain of internal transistors drops below a critical threshold level. Consequently, the effect of ELDRS can be far more significant for circuits than for individual transistors.

Another important factor is the wide range of power supply voltages that can be used for many circuits. It is essential to include a much broader range of electrical conditions when radiation testing is done on such circuits to assure that critical response mechanisms, such as the large input offset voltage changes in JFET op-amps, are identified.

Many circuits exhibit abrupt parametric changes after the degradation reaches a critical threshold level, unlike the more gradual degradation of older circuits. This increases the potential risk in spacecraft designs, particularly if available test data does not overlap the specific use conditions. Some of these mechanisms are due to specific circuit design techniques, including compensated input stages, JFET inputs, and use of low-performance pnp transistors in output stages.

These factors can be dealt with by careful planning and extension of the number of test samples and conditions that are used for radiation testing. Although this increases testing costs, it is critically important when unhardened commercial designs are characterized for use in space.

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