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Frequency Dependence of Single-Event Upset in Advanced Commercial PowerPC Microprocessors

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***Abstract*—Single-event upset (SEU) from heavy ions is measured for advanced commercial microprocessors in a dynamic mode with clock frequencies up to 1 GHz. Frequency and core voltage dependence of SEUs in registers and D-Cache are discussed. The results of our studies suggest the SEU in registers and D-Cache tend to increase with frequency. This might have important implications for the overall SEU trend as technology moves toward higher frequencies.**

***Index Terms*—Cyclotron, heavy ion, microprocessors, silicon-on-insulator.**

I. Introduction

TYPICALLY single-event upset (SEU) testing involves writing a test pattern into the storage elements (such as registers and cache), irradiating with heavy ions, and then reading the storage element states to determine the number of SEUs. Obviously, clock frequency has no effect on static measurements of this kind. However, in dynamic measurements, if the memory is continuously written to and read during irradiation, clock frequency is expected to affect the cross section because there is a larger probability that transients from combinational and logic operations will overlap clock edge transitions.

With clock frequencies constantly increasing, the concern about dynamic SEUs is becoming an important factor. Therefore, it is important to understand the mechanisms responsible for dynamic SEUs in integrated circuits (ICs), as well as their dependence on clock frequency. These dynamic measurements are difficult to perform, primarily because of the difficulty of isolating dynamic SEUs in ICs exposed to ion beams at accelerators.

Recent experiments have demonstrated that the occurrence of SEUs in ICs increases with increasing clock frequency [1]–[3]. In fact, there is some evidence that at high frequencies the dynamic SEU rate may be dominated by errors generated in combinational logic rather than in sequential logic [1], [3]. (In combinational logic, the output of the logic element is dominated by the inputs at that time, whereas in sequential logic, the output depends on the switching of a clock.)

Static measurements with ion beams reveal that the SEU increases with increasing linear energy transfer (LET), eventually reaching a saturation level at high LETs [4]–[6]. The gradual increase in cross section has been attributed to the varying SEU threshold across the sensitive area, such that at low LETs only a small fraction of the total sensitive area contributes to SEUs, whereas at high LETs a majority of the sensitive area contributes. For combinational logic circuits, the dependence of the dynamic SEU rate arrives from two sources: the varying of the sensitive area and varying the sensitive time. The sensitive period around a clock edge increases as the amount of energy deposited increases (higher LET). If the upset occurs just prior to the clock transition, less charge will be needed than if it occurs at an earlier time. It is the goal of this paper to demonstrate that the dynamic SEU changes with increasing LET.

Previously, we reported SEU measurements for silicon-on-insulator (SOI) commercial PowerPCs with a feature size of 0.18, and 0.13 μm [4], [5]. These results show an order of magnitude improvement in saturated cross section compared with complementary metal–oxide–semiconductor (CMOS) bulk counterparts. Those measurements were done while the processor was in a static mode.

Recently, we have extended our SEU studies to dynamic conditions; varying the clock frequency. Only limited data is available in the literature for the clock frequency dependence of the SEU of microprocessors. In [7] and [8] the clock frequency dependence of the SEU of the Alpha and AM2901 microprocessors under use conditions has been investigated. These measurements were limited to a clock frequency of 400 MHz and focused on the different failure trends for random core logic and the cache. Also, a direct comparison of SEU sensitivities of the same generation of SOI and CMOS bulk microprocessors has been made [9]. They performed their measurements in dynamic mode for a clock frequency of 133 MHz.

This paper examines SEUs in advanced commercial SOI microprocessors in a dynamic mode, studying SEU dependence of general purpose registers (GPRs), floating point registers (FPRs), and D-Cache on clock frequency. Results are presented for SOI processors with feature sizes of 0.18 μm and two different core voltages.

II. Experimental Procedure

A. Device Descriptions

The Motorola 7455 is the first generation of the PowerPC family to be fabricated with SOI technology. It is built on a partially depleted technology without body ties. The 7455 has a feature size of 0.18 μm with a silicon film thickness of 110 nm

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and internal core voltage of 1.6 V. A low power version of this processor operates with an internal core voltage of 1.3 V. These devices are packaged with "bump bonding" in flip-chip ball grid array (BGA) packages.

Table I shows how the recent SOI generations of the PowerPC family compare with previous bulk generations. The feature size of the SOI Motorola PowerPC is reduced from 0.29 to 0.13 μm, with the core voltage reduced from 2.5 to 1.3 V. The larger die sizes of the SOI PowerPCs are due to the more advanced design. The processors tested are highlighted in gray in Table I.

TABLE I
SUMMARY OF MOTOROLA'S POWERPC FAMILY OF ADVANCED PROCESSORS

Device	Feature Size (µm)	Die Size (mm^2)	Core Voltage (V)	Maximum Operating Frequency (MHz)
750 (G3)	0.29	67	2.5	266
7400 (G4)	0.20	83	1.8	400
7455 (SOI)	**0.18**	**106**	**1.6**	**1000**
7455* (SOI)	**0.18**	**106**	**1.3**	**800**
7457 (SOI)	0.13	98	1.3	1000

*This is a special low power version of the Motorola SOI PowerPC 7455.

B. Experimental Methods

Radiation testing was performed at the Texas A&M cyclotron. Because of the "flip-chip" design of the Motorola PowerPC, irradiations were done from the back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. The thickness of die is about 850 μm. Irradiations were done in air utilizing 40 MeV/u ^{20}Ne and ^{40}Ar ions. Both ions have enough range to penetrate the die. A LET range of 1.7–15 MeV-cm^2/mg was covered in the measurements.

Radiation testing was done using the "Sandpoint" development board designed by Motorola. This eliminated the large engineering effort required to design a custom test board for the processor. It also provided a basic PROM-based system monitor instead of a complex operating system. This provides better diagnostics and control of processor information during SEU testing compared to more advanced operating systems. The external communication channel on this board is a simple serial connection used as a "dumb" terminal and a joint test action group (JTAG) port. More detailed information about "Sandpoint" development board is available on Motorola's website. An Agilent Technology 5900B JTAG probe was used for our tests. This probe made it possible to interrogate the processor even after unexpected events occurred (such as operational errors during irradiation).

Register tests were done in two methods with special "loop" software. In the first method for example the loop performed the following steps for testing of GPRs:

1) Method 1:

1) Load a GPR with the operand $0 \times 55\,555\,555$ (multiplicand).
2) Load the next GPR with operand 0×2 (multiplier).
3) Multiply the registers together and write the result into the first register.
4) Increment the register pointer (now the second becomes the multiplicand and a third GPR is the multiplier) and repeat the Steps 1 to 3, until all the GPR hold multiplication results.
5) Read the entire GPR and check that the result agrees with expected value of $0 \times$ aaaaaaaa.
6) If not, then log the result to external memory as a strip chart (to be utilized in offline analysis).

This test has three possible outcomes:

1) The test passes and no upset is recorded.
2) The results do not match the expected value, but only one or two bits are wrong so this is counted as a register upset.
3) The result does not match the expected value, but many bits are erroneous which is counted as a processing unit upset because it occurred, for example, in the arithmetic logical unit (ALU) or in the register addressing logic.

In this method the GPRs are continuously being read and written and the ALUs are kept busy. Similar steps were performed for FPRs measurement.

In order to eliminate the contribution from the core logic to dynamic measurement of registers, we also test the FPRs and GPRs by the following method.

2) Method 2: The registers are filled with a known pattern prior to irradiation. In a small loop, the registers are read and checked for upsets, continuously. In the case of an upset, a counter is incremented and registers are reloaded with the initial pattern.

The adopted method for measuring of D-Cache SEUs utilized the upper fourth (8 K byte) of the D-Cache. The D-Cache is filled with a known pattern prior to irradiation. In a small loop, the processor continuously writes a snapshot of the D-Cache to a strip chart in the physical memory. After irradiation, an external interrupt triggers a program to compare the cache contents with the pattern initially loaded and counts state changes in the D-Cache. In this method we heavily exercise the data cache, which is likely to make the largest contribution to upset rates for most real applications.

These upset results and discussions of their implications are the focus of the present paper. In particular, the results at two frequencies (350 and 1000 MHz) and two operating voltage (1.6 and 1.3 V) are compared. Additional data were taken on the functionality of the test program under irradiation and results follow on failures due to processor malfunctions (hangs) at both frequencies and voltages.

III. TEST RESULTS

A. Clock Dependence

Fig. 1 shows the results of the SEU measurements for the Motorola SOI PowerPC 7455 GPRs in dynamic mode. The clock frequency for this measurement was 350 MHz and the operating voltage was 1.6 V. In this figure we display the upsets from the registers, ALU, and total upsets (sum of upsets from registers and ALU). Clearly, the primary contribution to the cross section was from the upsets in the registers. However, there was

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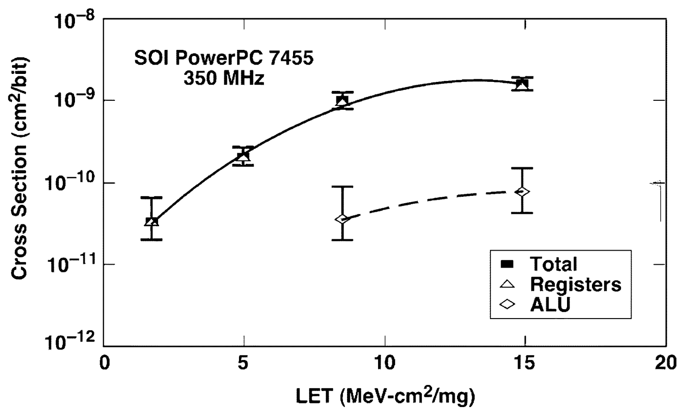

Fig. 1. Heavy-ion cross sections of GPRs of the Motorola SOI PowerPC 7455 for dynamic mode (Method 1).

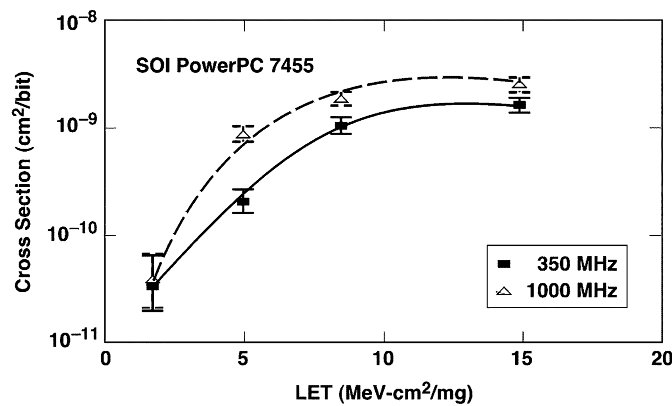

Fig. 2. Comparison of SEU for GPRs with clock speed of 350 and 1000 MHz (Method 1).

also some contribution from the ALU unit to the SEUs at higher LETs.

Static measurements reveal that the SEU increased with LET, eventually reaching a saturation level at high LETs [4], [5]. The same trend was seen in the dynamic measurements.

In Fig. 2, we compare the SEU measurements for the Motorola PowerPC 7455 GPRs taken by Method 1 at two clock frequencies: 350 and 1000 MHz. At very low LET, counting statistics prevent conclusive interpretation. However, for the higher LETs the results with 1000 MHz clock frequency are systematically larger by almost a factor of 2 compared with the results for a clock frequency of 350 MHz. This implies that there is a clock dependency in SEU measurement of the registers.

We also repeated SEU measurements on a special version of the Motorola PowerPC 7455 which operates with a lower internal core voltage specification of 1.3 V. Similar clock frequency dependence was observed for the registers and ALU contribution.

Fig. 3 compares the SEU measurements for the Motorola PowerPC 7455 registers (FPR+GPR) taken by Method 2 at two clock frequencies: 350 and 1000 MHz. These measurements were done by continuously reading and reloading of the registers. In these measurements, the effect of core logic unit is eliminated. The results with clock speed of 1000 MHz are systematically larger compared with the results for clock speed of 350 MHz which is consistent with results shown in Fig. 2.

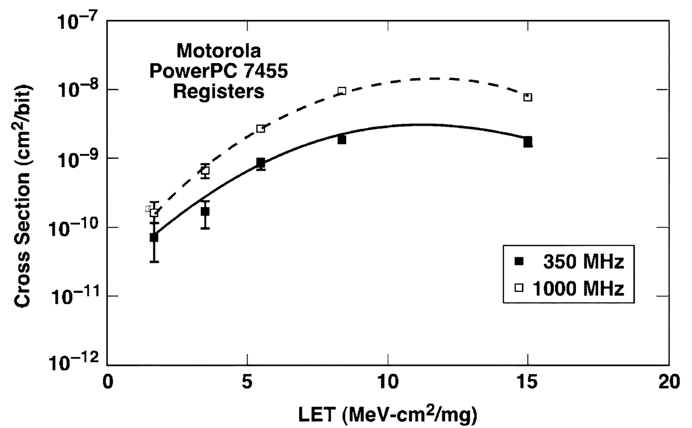

Fig. 3. Comparison of SEU for registers (FPR + GPR) with clock speed of 350 and 1000 MHz (Method 2).

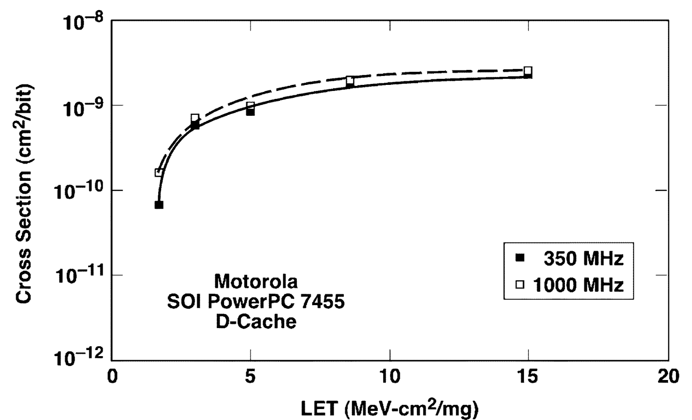

Fig. 4. Comparison of SEU for D-Cache with clock speed of 350 and 1000 MHz.

Fig. 4 compares the SEU measurements for the D-Cache of the Motorola PowerPC 7455 at two clock frequencies: 350 and 1000 MHz. The statistical error bars are not shown; they are smaller than the size of the plotting symbols. These measurements are done by continuously reading one fourth of the D-Cache. Since we are continuously monitoring one fourth of the D-Cache, there are some static SEU contribution from bits that are not read. Thus our measurement is an admixture of static and dynamic contribution. In fact, there is more contribution from static than dynamic. The results with clock speed of 1000 MHz are slightly larger compared with the results for clock speed of 350 MHz. This might be due to an increase in the SEU contribution of the dynamic portion of the admixture at clock speed of 1000 MHz. It is possible to continuously read a very small portion of the D-Cache to increase dynamic contribution; however it requires large amounts of beam time to reach proper statistics. Nevertheless, our measurement suggests that the SEU in D-Cache increases with frequency.

B. Core Voltage Dependence

Fig. 5 compares the result of the dynamic SEU measurements on the Motorola PowerPC 7455 GPRs with a core voltage of 1.6 V with the results of the Motorola PowerPC 7455 with a core voltage of 1.3 V. Because of beam time restrictions, we did not take measurements at lower LETs with a core voltage of

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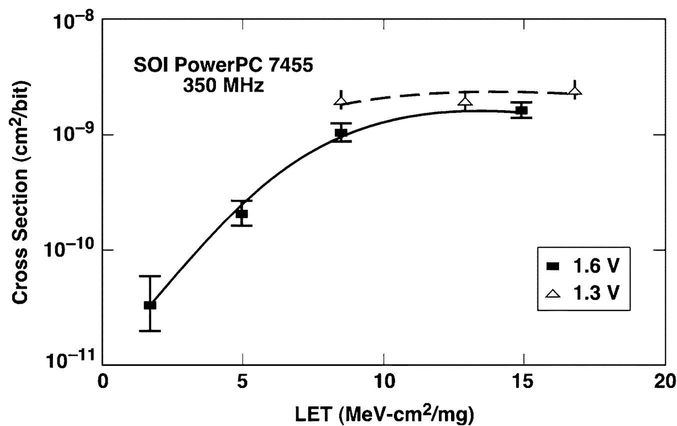

Fig. 5. Comparison of SEU for GPRs with internal core voltage specifications of 1.3 and 1.6 V at clock speed of 350 MHz.

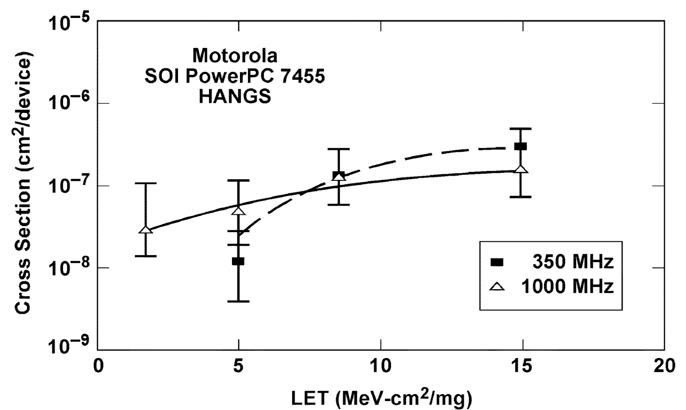

Fig. 6. Comparison of SEU for "hangs" with clock speed of 350 and 1000 MHz.

1.3 V. Although two processors have the same feature size, the SEU for lower operating voltage, 1.3 V, is larger than the SEU for operating voltage of 1.6 V at high LETs.

C. Functional Errors ("Hangs")

We also examined complex functional errors ("hangs") where the processor operation is severely disrupted during irradiation. We detected "hangs" by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, it was still operational to the point where normal software means could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a "hang." In nearly all cases, it was necessary to temporarily remove power from the device in order to recover, and reboot the device.

In order to evaluate "hangs," we calculated the "hang" cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed, including runs with no observed "hangs." This was done for each LET. Fig. 6 compares estimated cross sections for "hangs" at two clock frequencies: 350 and 1000 MHz during heavy-ion SEU measurements of the PowerPC 7455. The threshold LET appears comparable to that obtained for register and errors. The SEU for the two measured clock speeds are statistically consistent and no clock dependence can be made from current measurements.

Although the threshold LET for "hangs" is low, the cross section is small enough so that the expected incidence of "hangs" is not very high in typical space environments.

IV. Discussion

Seifert *et al.* measured the frequency dependence of alpha-particle induced SEU in the 21164 Alpha microprocessor [7]. They found that the SEUs in the cache (which has no dynamic latch nodes) increase with frequency. However, their results suggest that SEUs in the Alpha core logic decrease with increasing clock rate and are dominated by the contribution from dynamic latch nodes. While the SEU increases with clock frequency for reading the content of memory cells, it decreases for upsets generated in level-sensitive transmission gate type latches. This is consistent with our results for the registers and D-Cache. It is also consistent with the expectations and explanation of Buchner *et al.* [1], that errors are caused by single-event transients in coincidence with vulnerability windows associated with clock edges and that increase proportionally with frequency. The latter observation (an increase in SEUs for higher frequencies) appears to be the result of the lowering of the critical charge for upset for storage elements implemented in dynamic logic, at least as implemented by the 21164 Alpha designs.

If the ion strike occurs at a finite time prior to the clock edge, an upset may still occur, provided sufficient charge has been liberated by the ion so that the voltage transient will still be above the threshold for upset when the clock pulse arrives. If the ion strike occurs well before the clock edge, the transient will have decayed by the time the clock transitions, and no SEU will be registered. In summery, SEUs originate in combinational logic if the ion strike occurs in a period just prior to the clock transition from high to low, where the period depends on the amount of charge deposited by the ion [1].

Also, previous work has shown [10] that at high frequencies (more than 50 KHz) and in presence of ions with large LETs, gates in logic circuits may be sensitive to upsets during a large fraction of their duty cycle. Ions with large LETs will have a greater probability of producing an upset in a logic circuit gate than ions with small LETs because the window during which the gate is sensitive widens as the ion LET increases. Therefore, there will be more time during the clock cycle for which the circuit is sensitive. It is essential to know this information for circuits that operate at very high speeds and that contain gates whose upset sensitivity is clock-dependent, because the higher the speed the more chance there is of an upset occurring.

Consider what dynamic upset testing of a processor really measures. Typical use of the term "dynamic" implies running a program and comparing the expected result with the actual result, counting an error when they are not the same. In practice, such a test measures both the static cross sections of the bits that it uses (i.e., clock-independent errors) and the dynamic cross sections of logic units (i.e., clock-dependent errors). Note, however, that not all bits within a microprocessor are used in typical programs. Further, the bits are actually storing data only for a portion of the time that the program takes to run. Thus a dynamic test is an admixture of static and dynamic contributions. Dynamic contribution changes depending on the experimental method of measurement.

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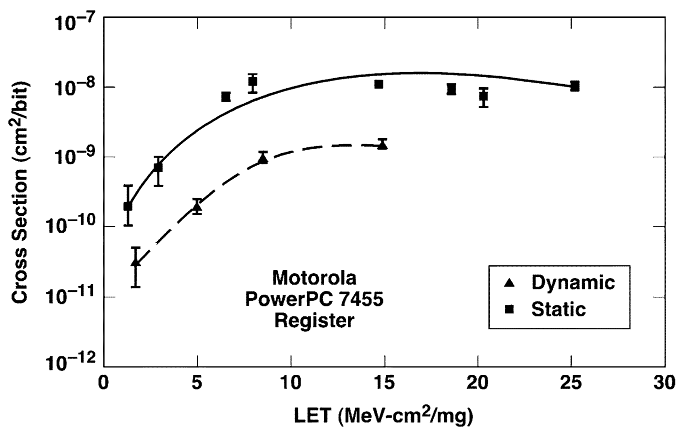

Fig. 7. Comparison of the dynamic and static SEU for registers at 350 MHz.

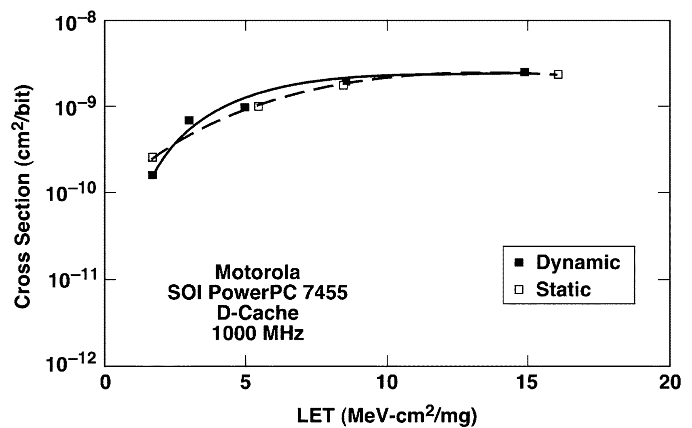

Fig. 8. Comparison of the dynamic and static SEU for D-cache at 1000 MHz.

Our previous static SEU for registers [4], [5] were measured by a test program designed to yield near the ideal case of 100% register duty cycle. In Fig. 7 we compare static and dynamic measurement of registers for PowerPC 7455 microprocessor. Results from our new dynamic test program provide per bit cross sections that are only about 15% of the "full" static results reported previously. This is consistent with our estimated register duty cycle of the dynamic test program. The register duty cycle depends on the design of the experiment.

In Fig. 8 we compare static and dynamic measurement of D-Cache at 1000 MHz for PowerPC 7455 microprocessor. As it was stated before, our method of measurement collects an admixture of static and dynamic contributions. In our method of measurement, static contribution dominates the dynamic contribution. Consequently, there is no difference between static and dynamic measurements and statistically both data measurements agree.

Although it is useful and instructive to make comparisons of SEU results between static and dynamic measurements, one must remember that these are complex devices, not test structures. Other factors in the processor design may also affect the way that processors respond to radiation in static and dynamic mode.

There are also different requirements for various registers and functions within the device. For example, access time is a critical requirement for on-board cache, but cache SEU results may not be representative of other types of registers within the device. Therefore, it is important to evaluate the SEU for different types of internal and storage elements because the overall upset rate of an operational program in real live application depends how the various types of storage elements are used as well as their cross sections.

V. Conclusion

This paper has evaluated SEU at different clock speeds using a dynamic test program at clock frequencies up to 1 GHz. The cross section for registers increases by as much as a factor of two at maximum clock frequency. The upset cross section in registers is dominated by the registers; the ALU contributes very little to the SEU. Similar results were obtained for two versions of the PowerPC with different core voltages. The cross section for D-Cache slightly increases with frequency. No clock dependence in the estimated cross section for "hang" was observed in our measurements.

These results have important implications as clock frequencies are increased to even higher levels. At this point the dependence on dynamic operation—at least for this particular processor—is relatively small, with little overall impact to system SEU rates. However, the frequency dependence may become larger for future generations or other specific circuits. Dynamic tests should be included in SEU tests of microprocessors or other complex circuits.

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