Re-configurable Electronics Characterization Under Extreme Thermal Environment

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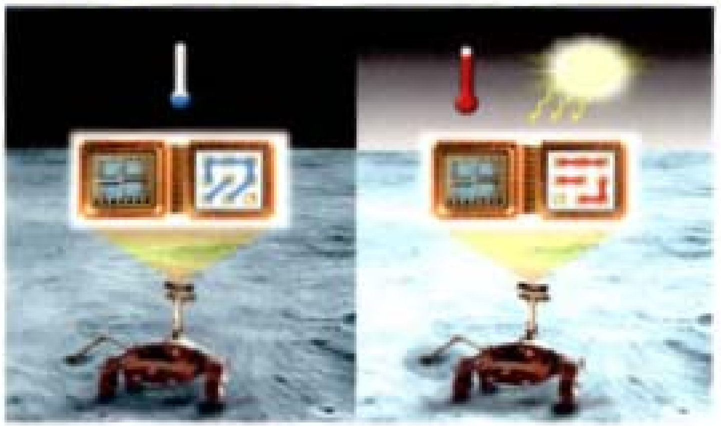

Outline

- Objectives
- Compensation of degradation in extreme environments
- Evolvable hardware, reconfigurability, & potential solution.
- DSP extreme temperature testing, results, conclusions
- FPGA extreme temperature testing, results, conclusions
- Reconfigurable Analog Array (RAA) Development, tests in extreme temperatures, results, and conclusions

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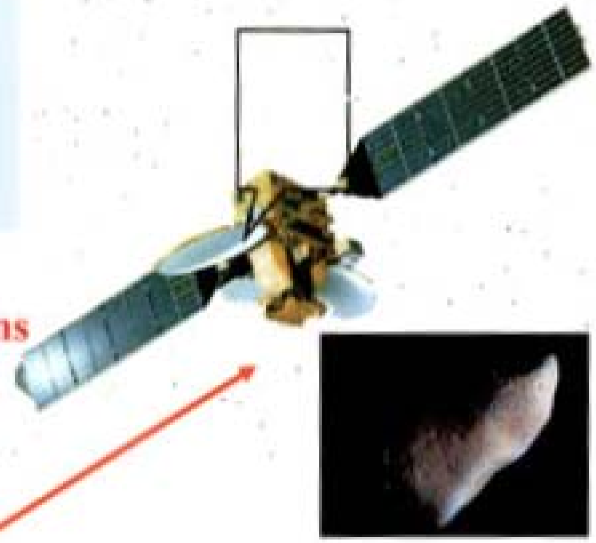
Objective: Surviving longer missions (10+ years) and harsher environments

Dramatic changes in hardware/environment, e.g. in case of faults or need for new functions, may require in-situ synthesis of a totally new hardware configuration.

Survivability:
Maintain functionality coping with changes in HW characteristics

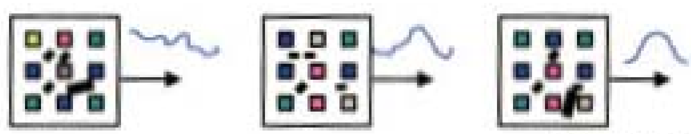
- Radiation impacts
- Temperature variations
- Aging
- Malfunctions, etc.



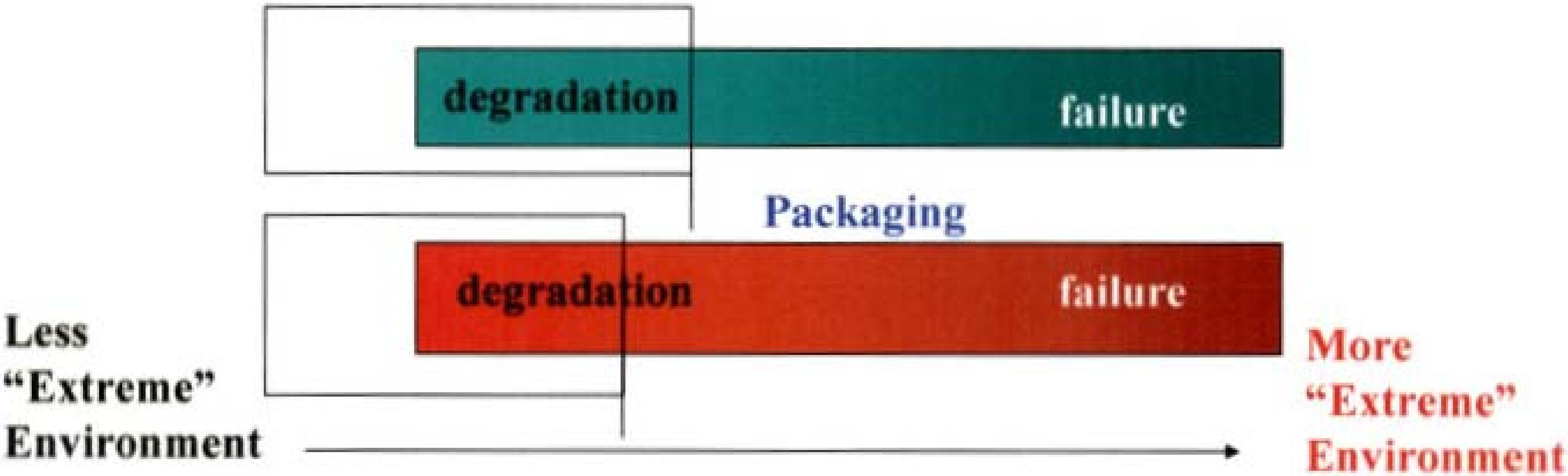
Versatility: Create new functionality required by changes in requirements or environment

New functions required for new mission phase or opportunity

Develop space HW that can evolve



How? Compensation of Degradations in Extreme Environments (EE)

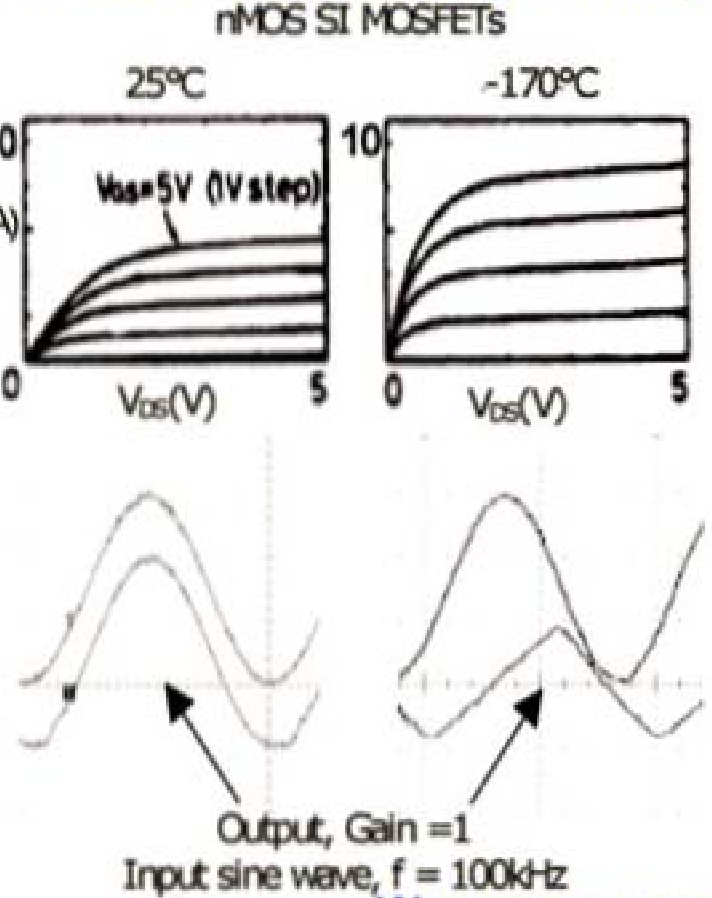


- Compensation by reconfigurable electronics:
  - of degradations in electronics – keep same function for electronics
  - or degradations at another subsystem/ or system level – adapt electronics functionality to maintain same function at system level

Many times failure is due to packaging, but before that point degradations could possibly still be compensated.

What? Effects of EE on electronics

Circuits are designed to exploit device characteristics within a certain Temperature/Radiation range; when that is exceeded, the circuit function gradually degrades…



offset voltage, current leakage...

Temperature changes device characteristics; device is still operational.

Influence may be different between various areas/circuits/components on same chip. It can also change with function.

Changes cause degradation in circuit response of a commercial Op Amp.

If a circuit design is changed to take in consideration the modified device characteristic the response may be corrected.

We can map a new circuit design in a reconfigurable chip

How? Hardening-By-Reconfiguration

- Idea of Hardening-By-Reconfiguration (HBR): mitigate drifts, degradation, or damage on electronic devices in EE by using reconfigurable devices and an adaptive self-reconfiguration of circuit topology.
- related to HBD - in-situ (re) design
- benefits from HBD for the resources available on the reconfigurable chips.
- work well with HBP, - extra layer of protection, for expansion of limits of operation in EE: HBP provides survivability to keep devices operational at higher EE limits, while HBR provides adaptation to changes in device characteristics needed for precise functions, specially for analog.
- Degenerated HBR: multiplexed/switched in fixed circuits, each optimally designed for a temp range
- Simple HBR: circuit configuration predetermined and memorized for access when needed,
- HBR configurations are determined *in-situ*

How? Evolvable Hardware Solutions

Evolvable hardware (i.e. hardware that self-configures under control of adaptation/ evolutionary algorithms) can preserve/ recover system functionality by reconfiguration/ morphing.

If device characteristics change with radiation/temperature, one can preserve the function by finding a different circuit solution, which exploits the altered/modified characteristics

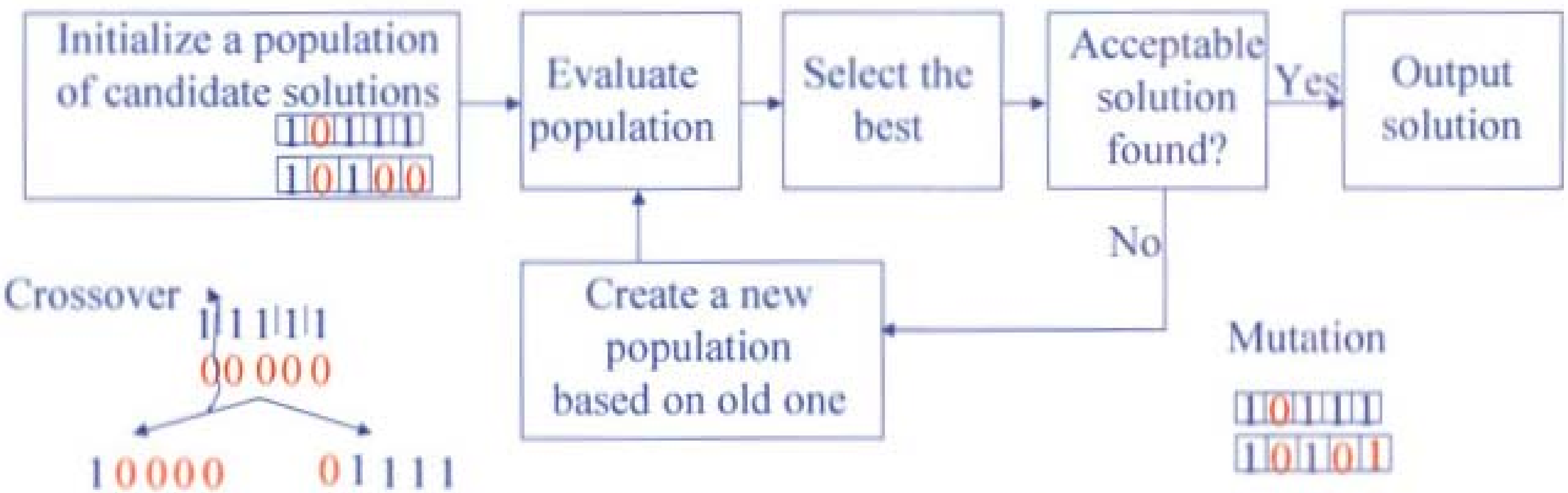
- **Degraded components can be salvaged**
- **Completely damaged components can be bypassed**

How? Reconfiguration Mechanisms

- Most popular searches: population based, use "generate and test" strategies. Evolutionary/Genetic algorithms are most used technique.

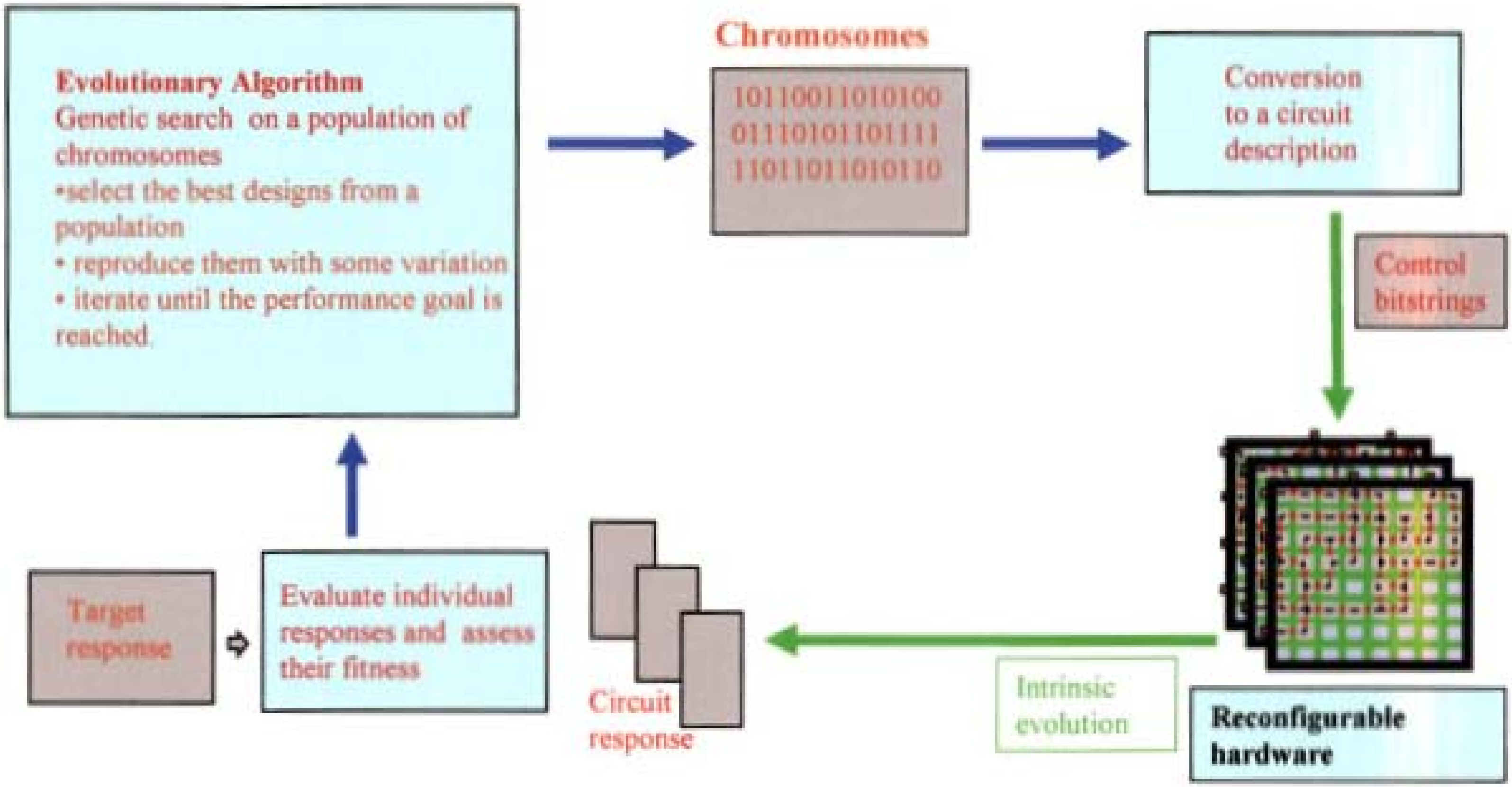
Sketch of a simple Evolutionary/Genetic Algorithm

A "chromosome" may simply encode the control of switches…eg 10100



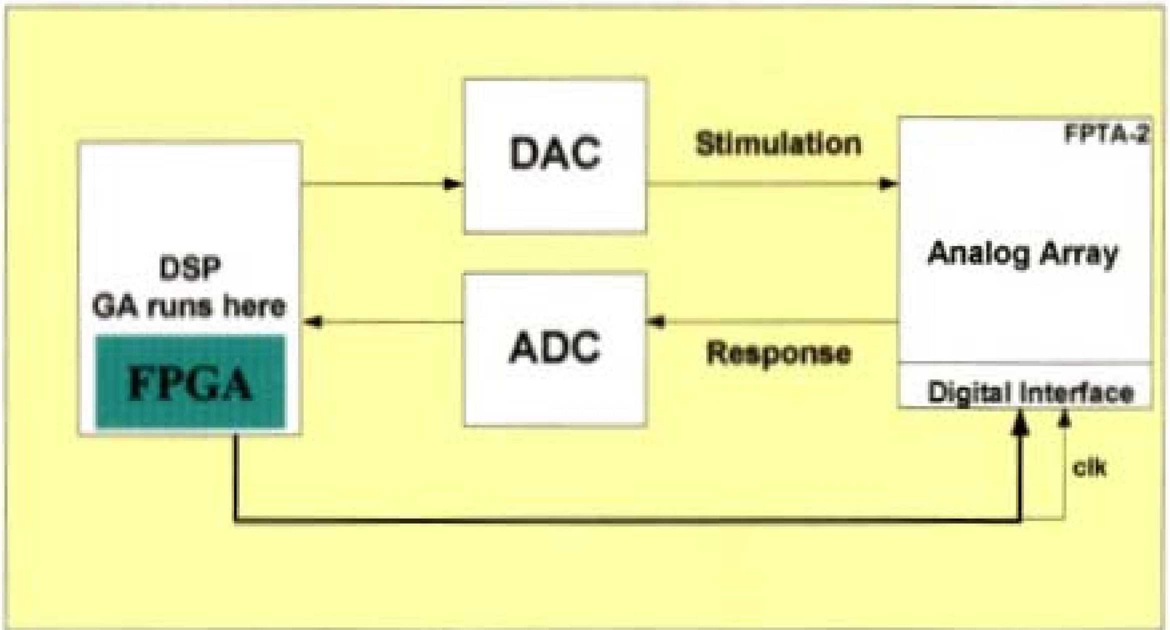
Crossover and mutation are two common genetic operators used in creating a new population.

How? Evolutionary adaptation of field programmable devices



Potential electronic designs/implementations compete;
the best ones are slightly modified to search for even more suitable solutions

Solution: A Stand-Alone Board-Level Evolvable System (SABLES)

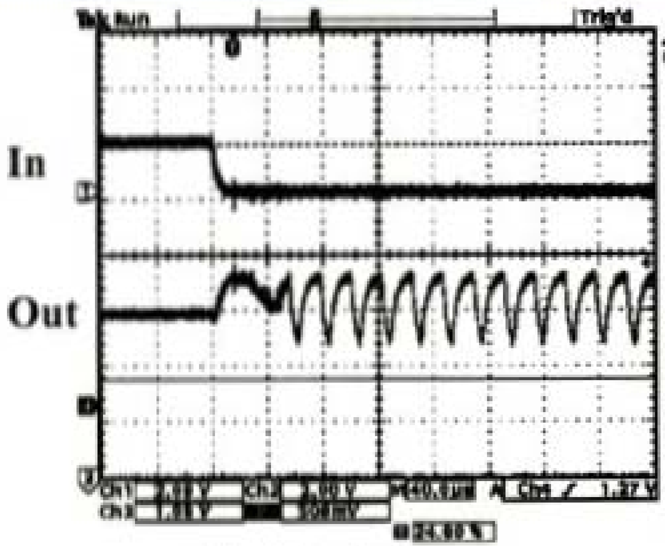


- DSP + FPTA
  - Fast download for evaluation of individuals
  - Good architecture for moving to a self-reconfigurable system-on-a-chip

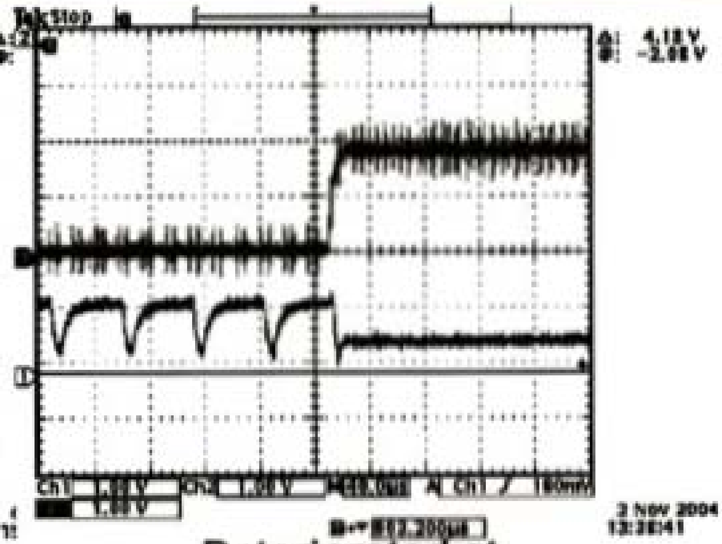
- Fits in a box 8" x 8" x 3".

- DSP board;
  - TMS320C6701processor
  - 16 analog inputs and outputs at 100 kSamples;
  - 32 Digital I/O at 7.5MHz

Recovery of temperature-degraded circuits – Controllable Oscillator

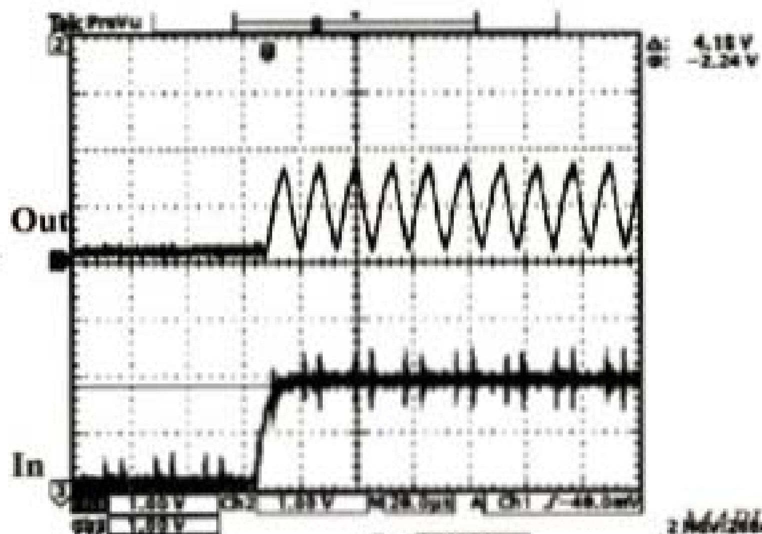


Evolved at room temperature



Deteriorated at -196.6°C

Recovered at -196.6°C



Summary of Evolvable Hardware

- HBR (hardening-by-reconfiguration), based on evolvable hardware is a technique that extends the range of usability of electronics in extreme environments. The capability of adaptive self-configuration was demonstrated for low and high temperatures.
- The challenge of conventional design is replaced with that of designing a recovery (e.g. evolutionary) process that automatically performs the (re)design in our place. *This may be harder than doing the design directly*, but makes autonomy and adaptation possible.

Testing of DSP (TI) under Extreme Temperatures

Objective

- Assess the electrical behavior of the Innovative Integration board containing a Digital Signal Processor (DSP) with its JTAG (Blackhawk) connector at extreme low temperatures to develop *Self-Reconfigurable Electronics for Extreme Environments (SRE-EE)*.
- The objective of the experiment is to determine the lowest temperature at which the DSP component can operate.

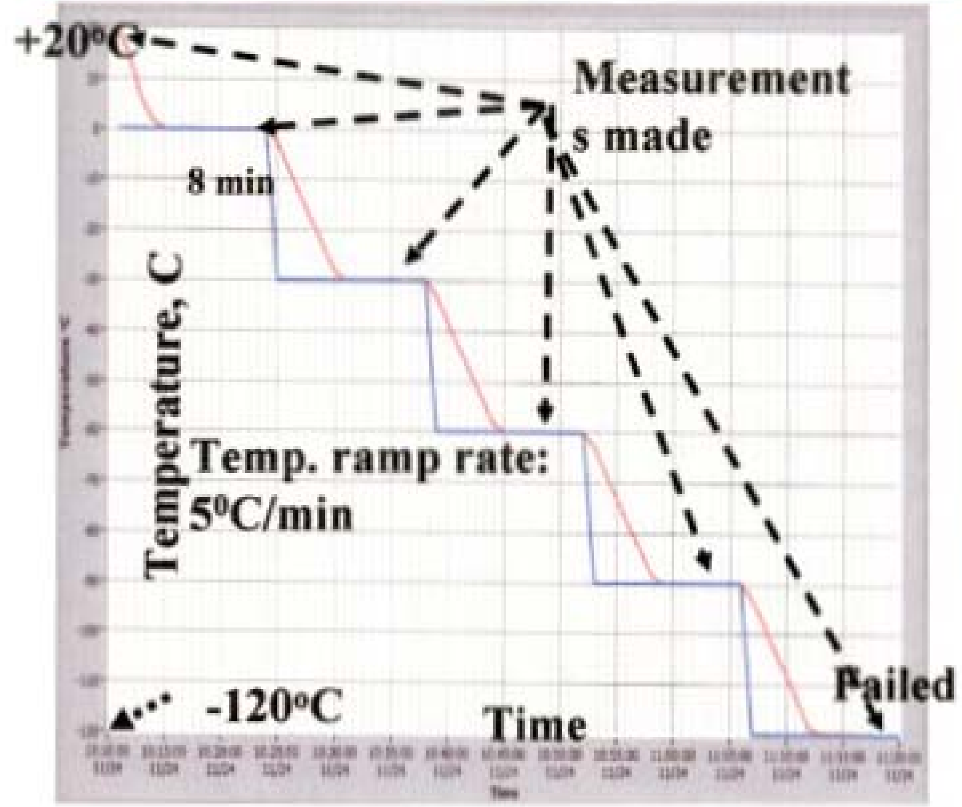
DSP chip

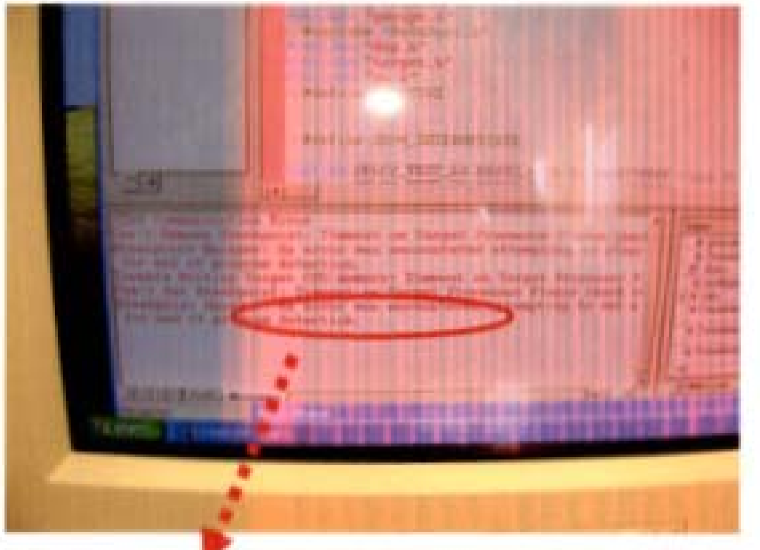
JTAG Connector

- DSP was tested by running a simple Genetic Algorithm (GA) whose target was the maximization of the number of '1's in the chromosomes
- Problem is solved in less than 1 minute, after 464 generations

Test profile 1

DSP Failure





- Test was repeated again for –90°C, –100°C, –110°C and –120°C to narrow the temperature range.
- Failure was observed during the testing in a temperature range of –110°C to –120°C.

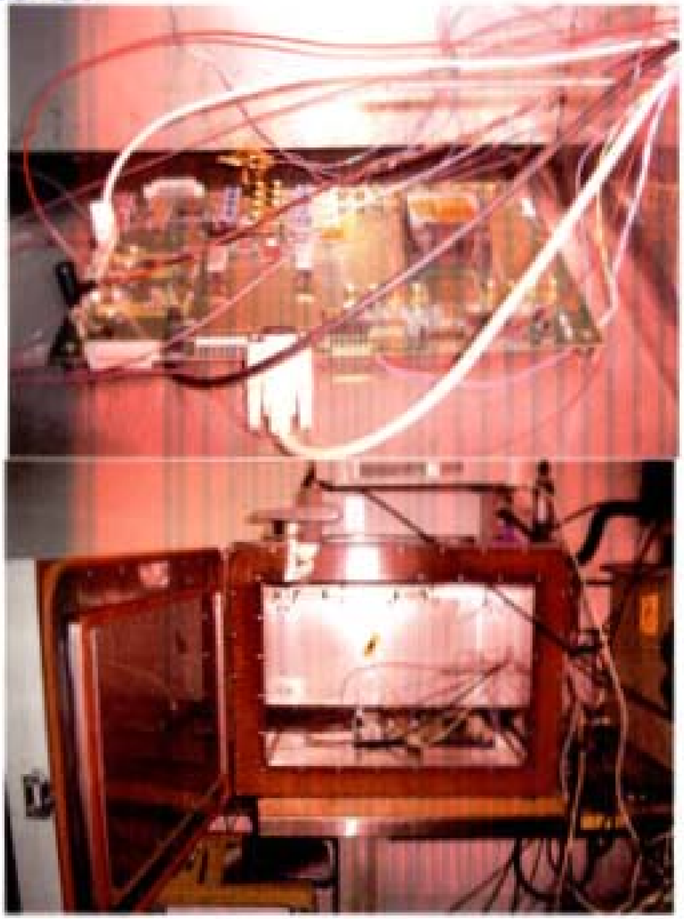
✓ Failure occured when PC is downloading GA into the DSP (JTAG communication error);

✓ The PC-DSP communication failure prevents the read-out of the DSP status/outputs.

- DSP Board works down to -110°C but failed for lower temperatures

Xilinx Virtex-II Pro FPGA

Objective: The purpose of testing this board at extreme temperatures is to initially find out whether the evaluation board and the Virtex-II Pro FPGA would survive and continue operating at different temperature ranges down to –180°C and up to 120°C.



The Virtex-II PP Board was tested at different temperatures. The temperature range covered in this experiment was from -180°C to 120°C.

The board was powered using 3 power supplies. They were set up at the following voltages:

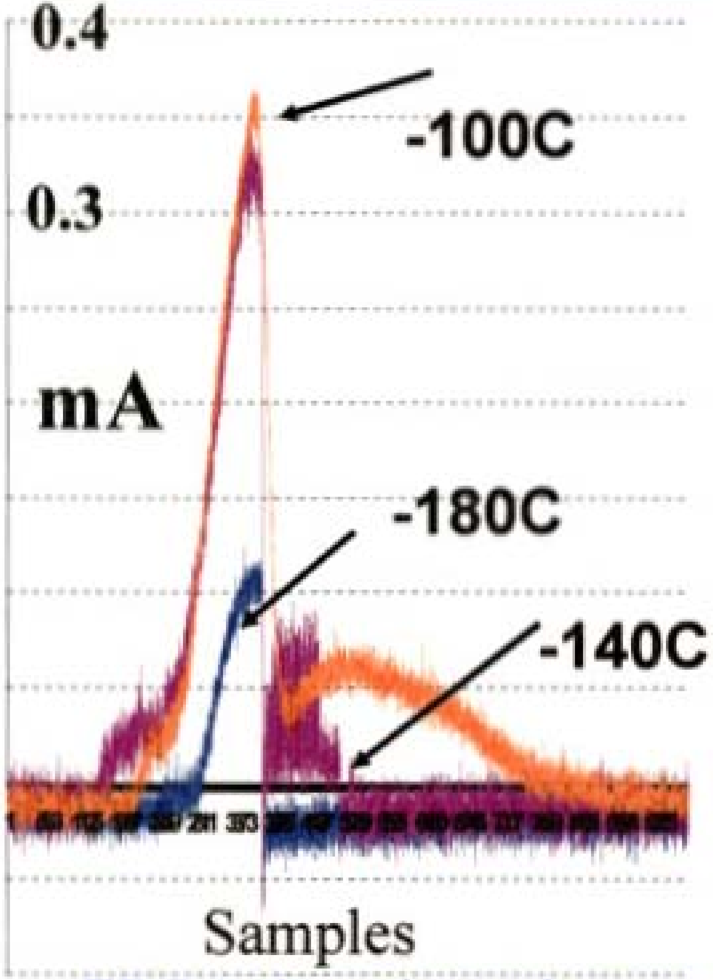
- 3.3V DC (to electronics in the board)
- 2.5V DC (to I/O's, banks, Rocket I/O Transceivers)
- 1.5V DC (supplied to the FPGA Core)

Surge current (in rush current) was measured on the 1.5V supply.

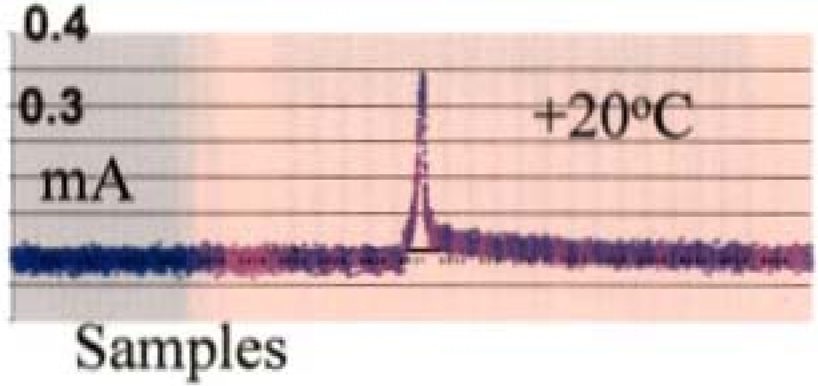
The test FPGA circuit runs self-checking firmware on 2 embedded processors, monitored via RS232 port

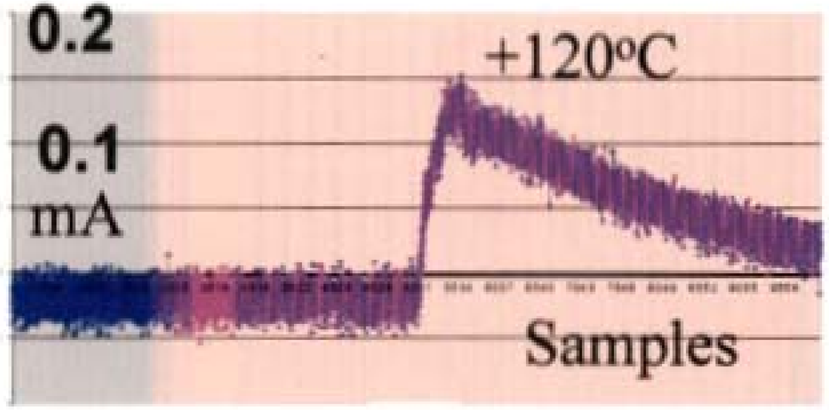
Extreme Temperature Test for the Virtex-II PP Board

- Reset switch to reset the logic
- Program switch to load the program PROMS to FPGA configuration
- "Hello World" program used to monitor the performance of FPGA
- The board was never shut down as the temperature was decreased in steps.
- Once it reached -180°C, the temperature was brought back up. At intervals, we power cycle the board and measure the in rush current.
- It was found as temperature ramped up that the board always powered on using reset program switches.



FPGA Core in rush current monitored as a function of temperature





FPGA core in rush current monitored as a function of high temperature

Summary: Extreme Temperature Test for the Virtex-II PP Board

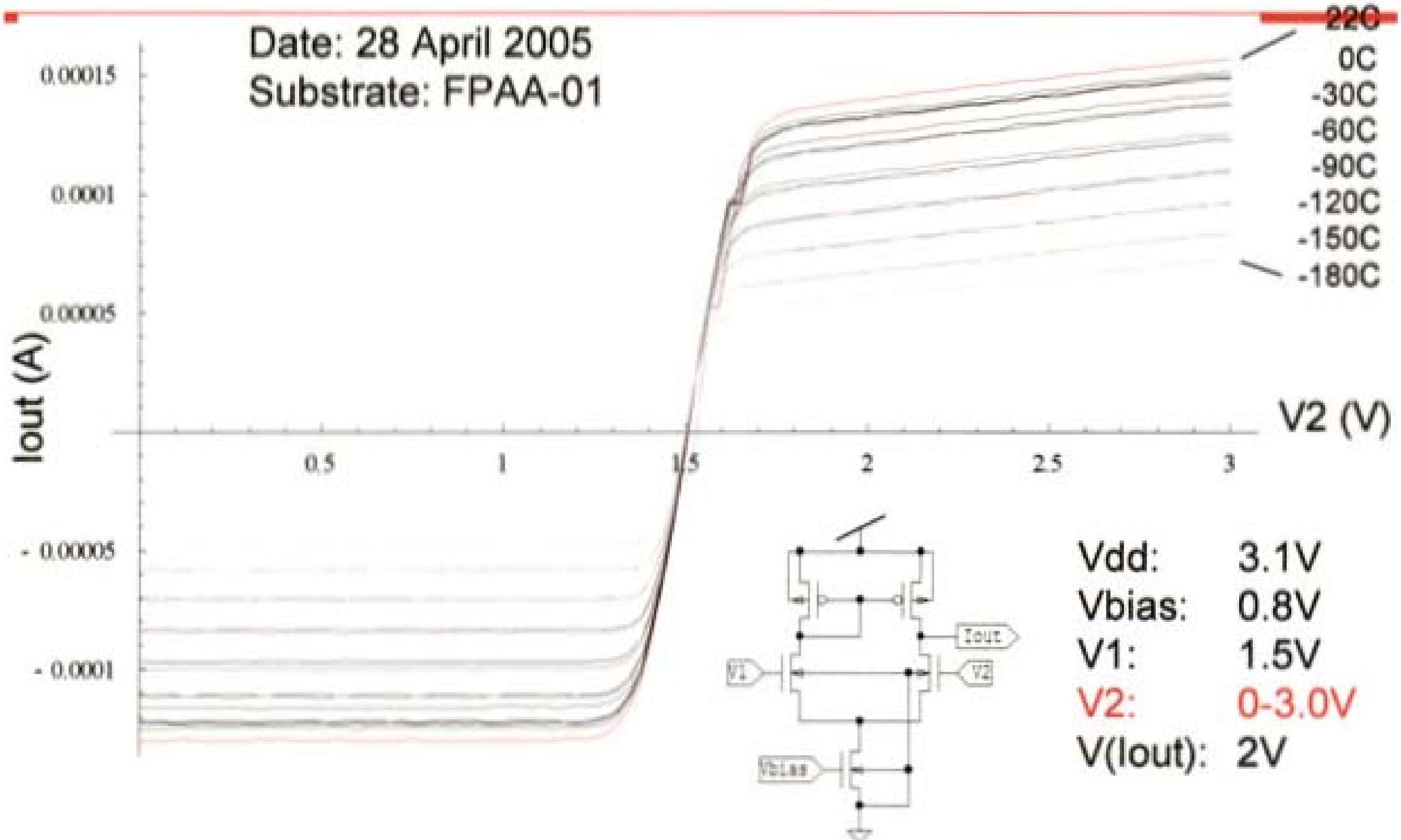
- The Virtex II Pro functioned correctly at temperatures down to –180°C and up to 120°C.
- The Virtex II Pro FPGA did not show a large in rush current at –180°C and also at 120°C.
- All temperatures, voltages, and current registered normal as well as power (on/off) cycling.
- Over all the high temperature in rush current transient have sharper current and last less than the cold temperature. (~25-30 msec)

Objectives: Reconfigurable Analog Array (RAA) Development

- Assess the behavior of G_m-C filters building blocks at extreme temperatures (from -180°C to 120°C);
- Perform preliminary tests on the functionality recovery through changes in the voltage bias;
- Components tested (Designed by SPAWAR using TSMC 0.35μm technology):
  - Operational Transconductance Amplifier (OTA);
  - Wide Range OTA (WRTA);
  - Differential pairs.

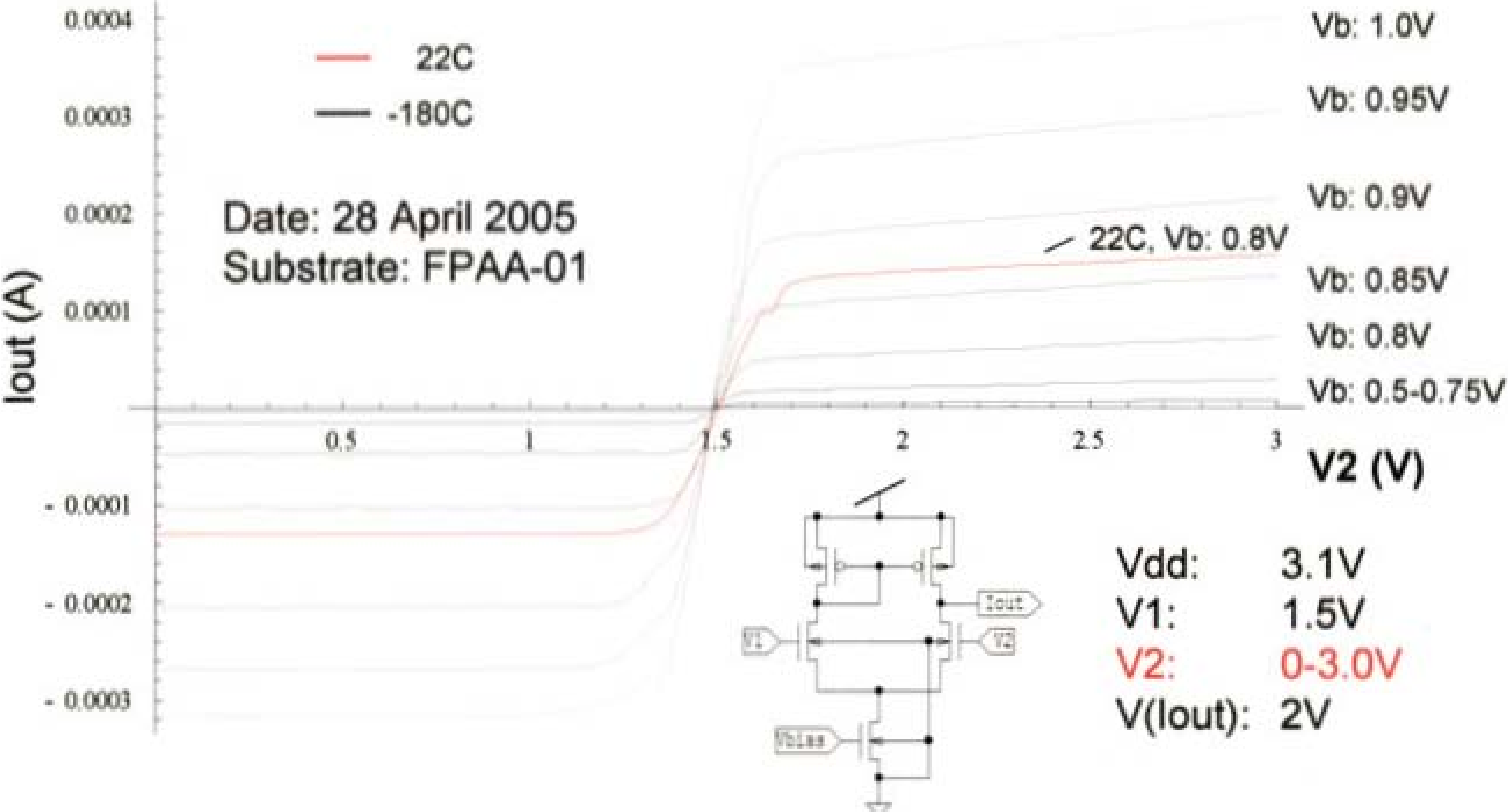
- Simulate and test single-ended first order G_m-C filter.

OTA Sweep Down (23°C to -180°C)



- ***Current lower and upper limits reduce as the temperature reduces.***

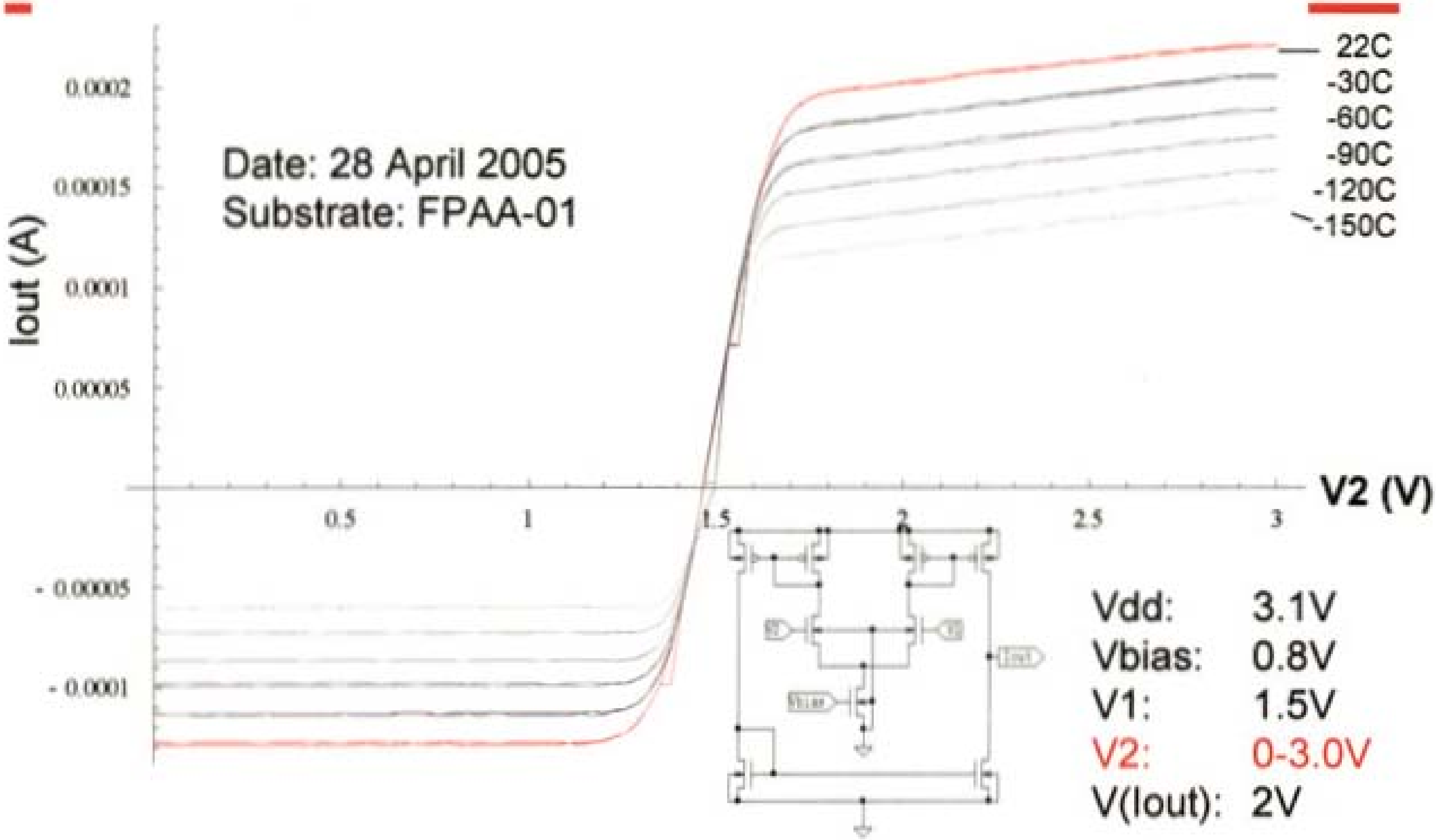
OTA Bias Sweep at -180°C



Vdd: 3.1V
V1: 1.5V
V2: 0-3.0V
V(Iout): 2V

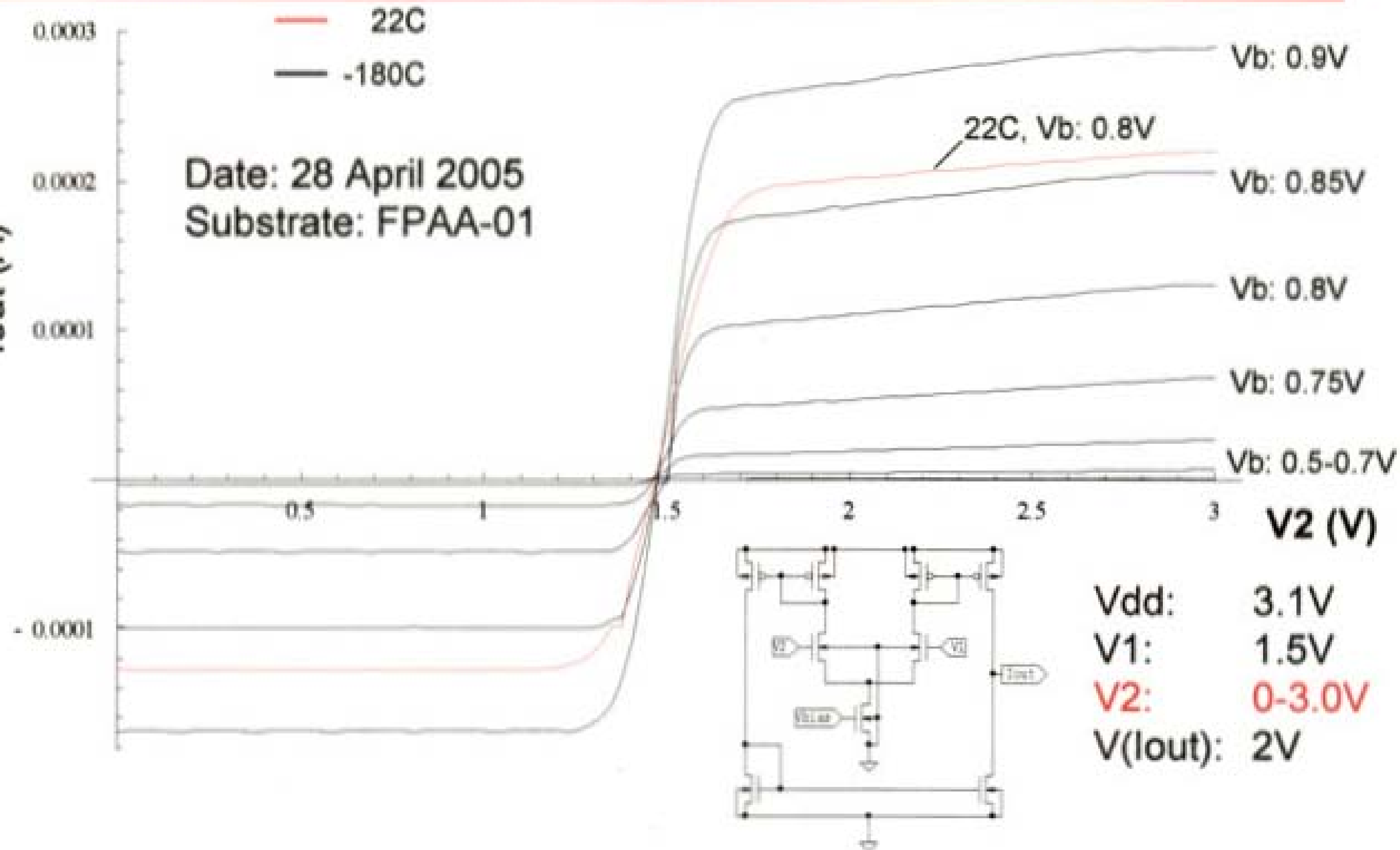
- ***Device function can be recovered by increasing Vb from 0.8V to 0.85V.***

WRTA Sweep Up (-180°C to 22°C)



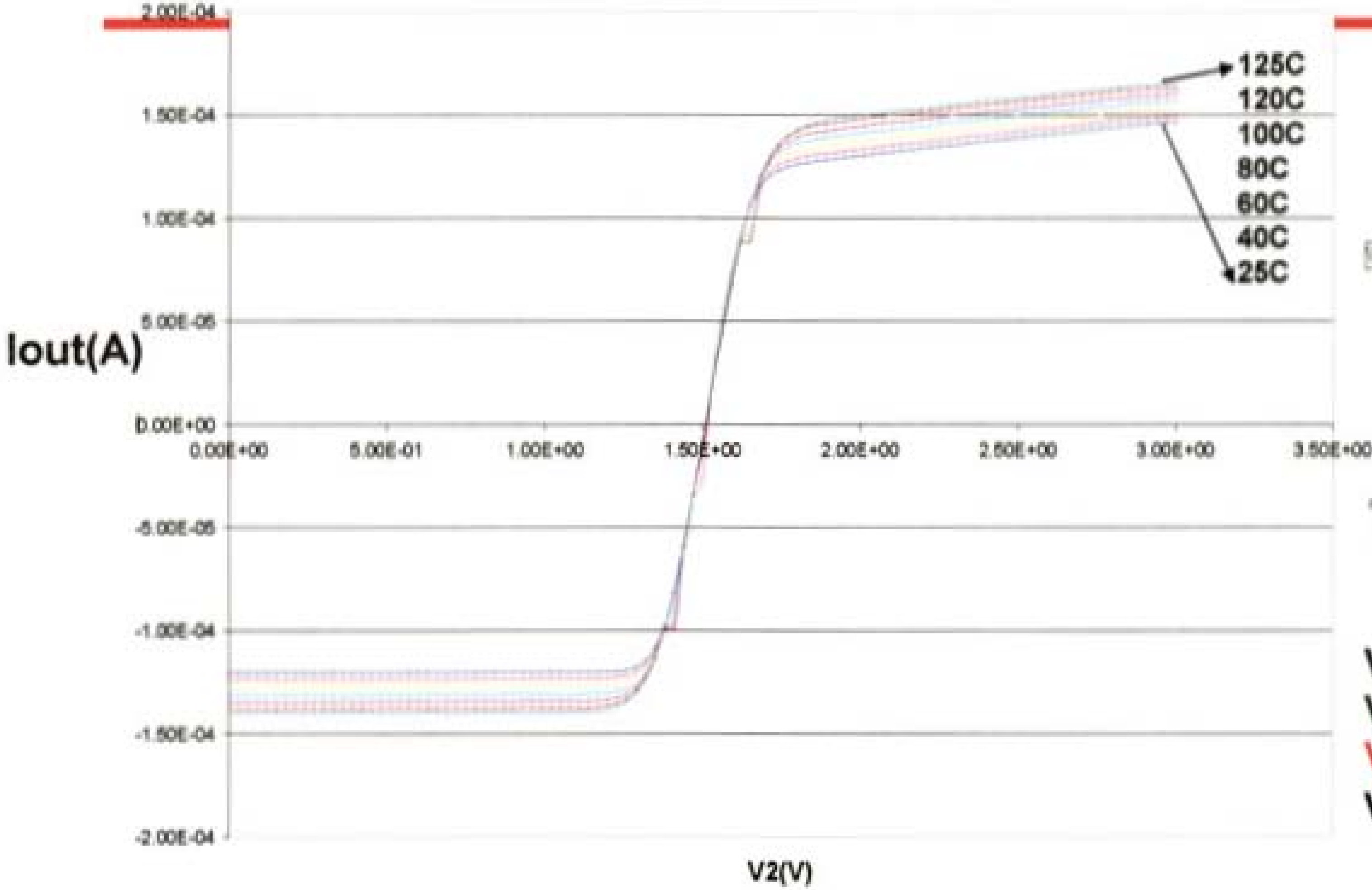
- ***Current lower and upper limits reduce as the temperature reduces.***

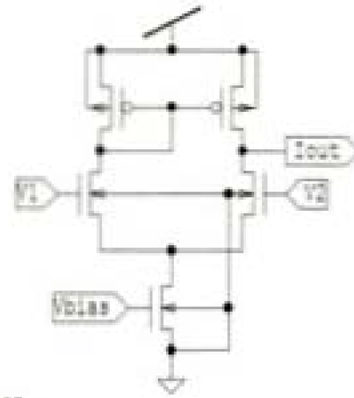
WRTA Bias Sweep at -180°C



➢ ***Device function can be recovered by increasing Vb from 0.8V to 0.85V.***

OTA Sweep Up (25°C to 125°C)



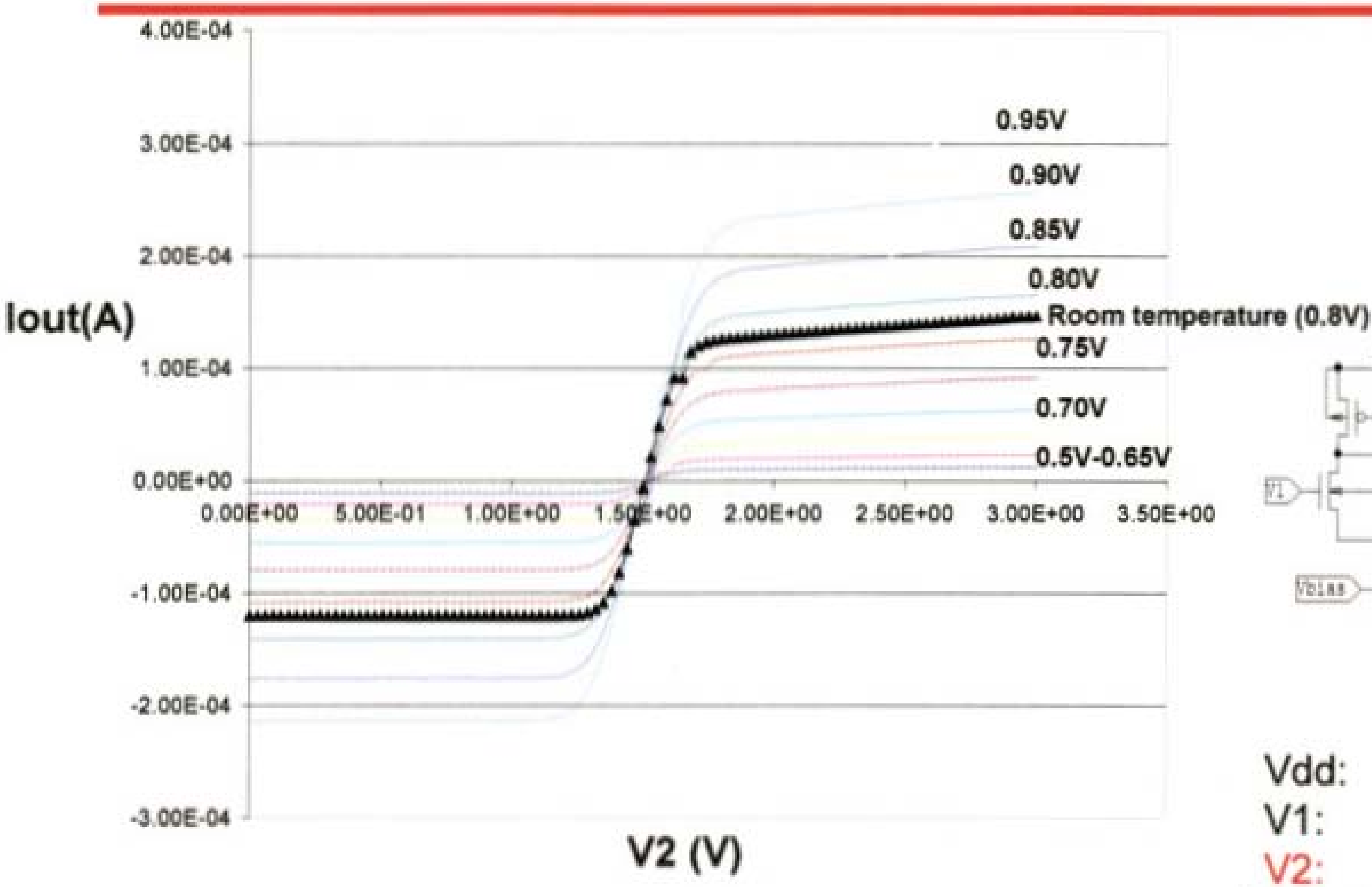


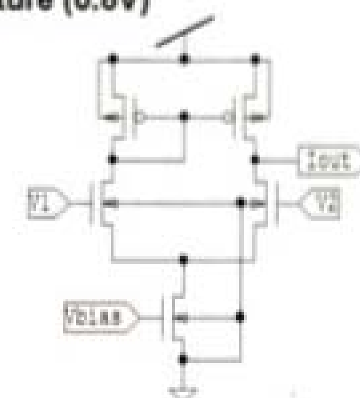
V2 (V)

Vdd:	3.1V
V1:	1.5V
V2:	0-3.0V
V(Iout):	2V

- ***Negative and positive saturation voltages increase as the temperature gets higher.***

OTA Bias Sweep at 120°C



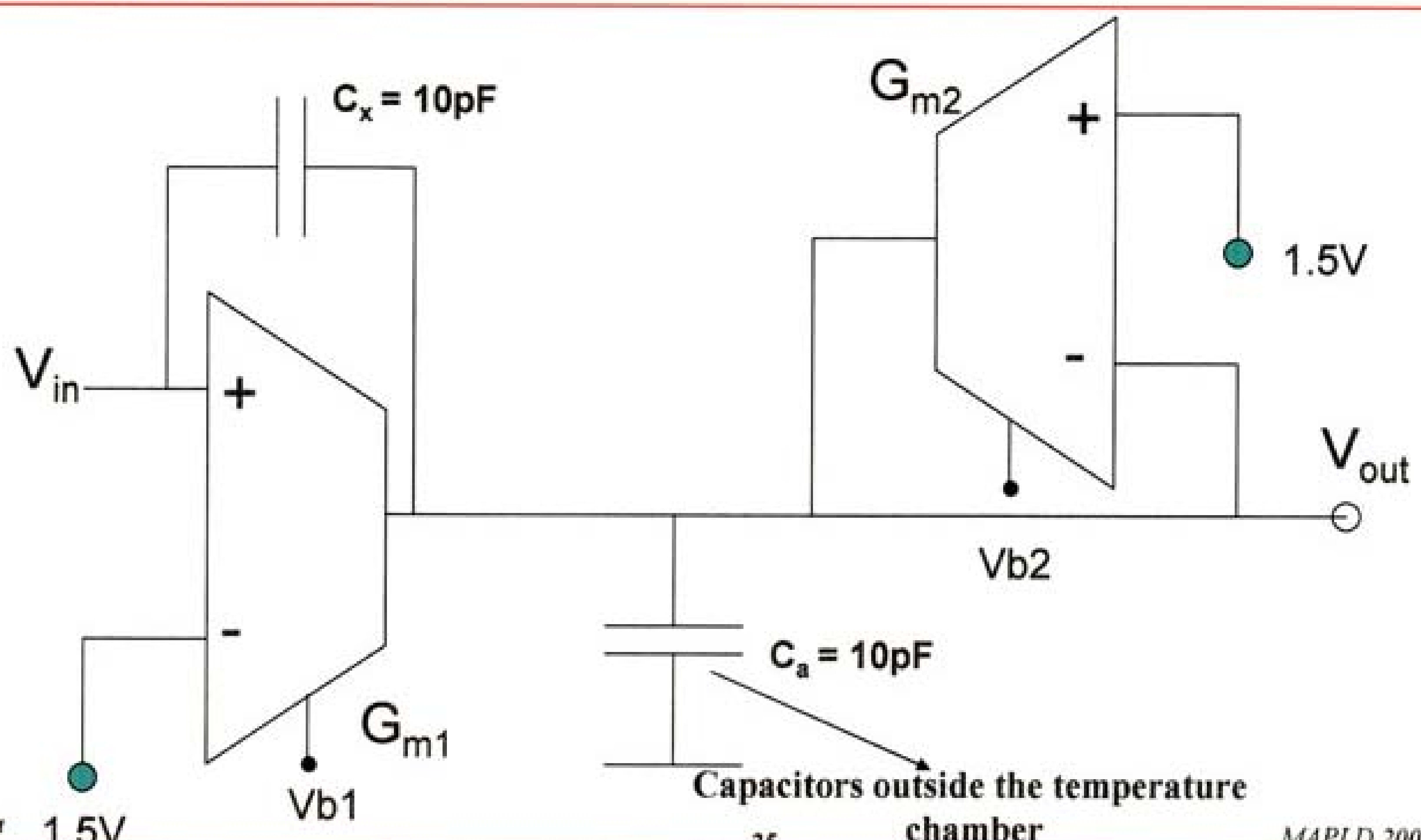


Vdd: 3.1V
V1: 1.5V
V2: 0-3.0V
V(Iout): 2V

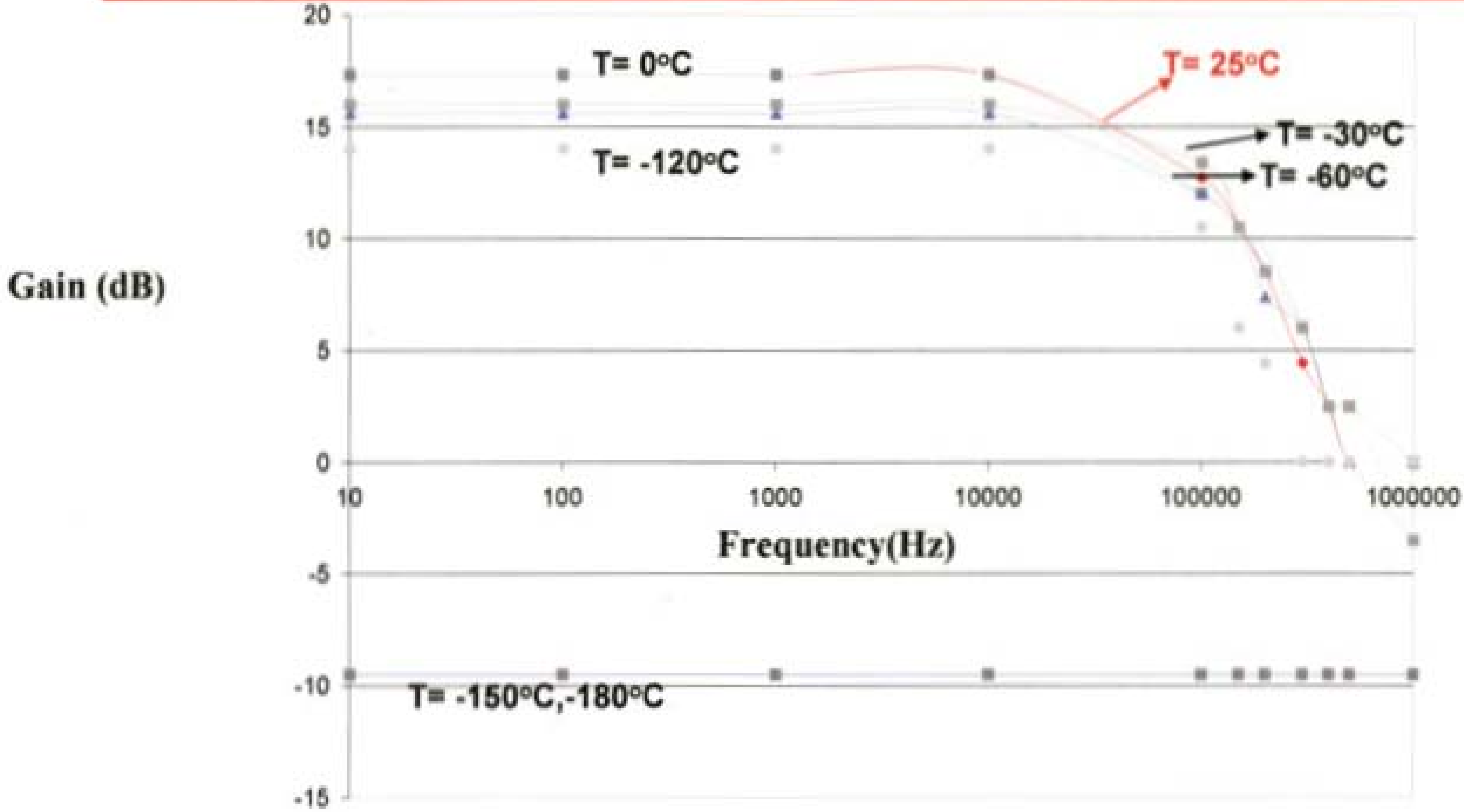
- ***Device function can be recovered by decreasing Vb from 0.8V to around 0.75V.***

Objectives: First Order GmC Low Pass Filter

- Test the recovery through V_{bias} in a filter circuit;
- Built at the board level using two chips (two OTAs);
- Characterize filter behavior at extreme temperatures and test recovery through adjustment of bias voltage;

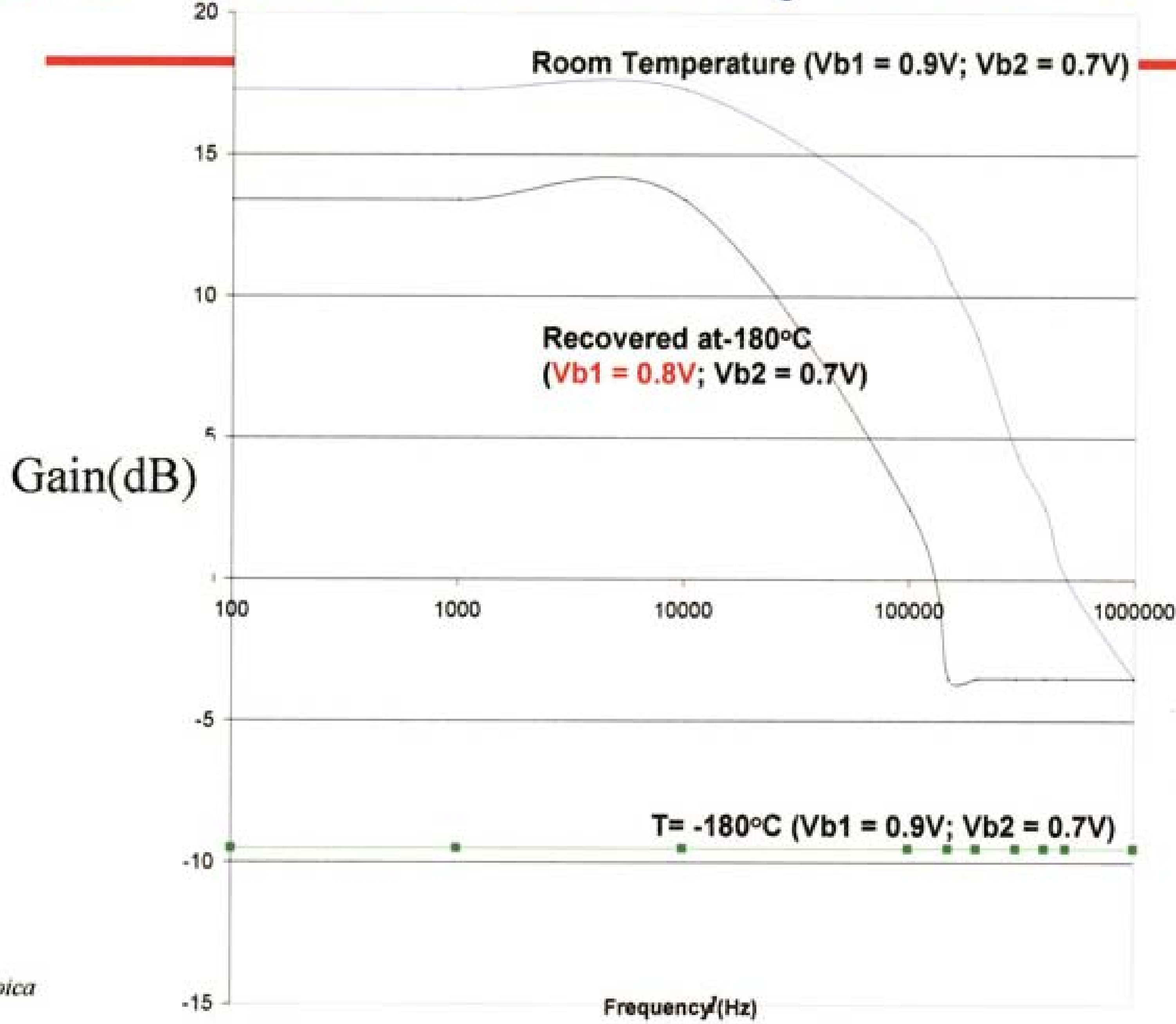


Low Temperature Tests – Frequency Response

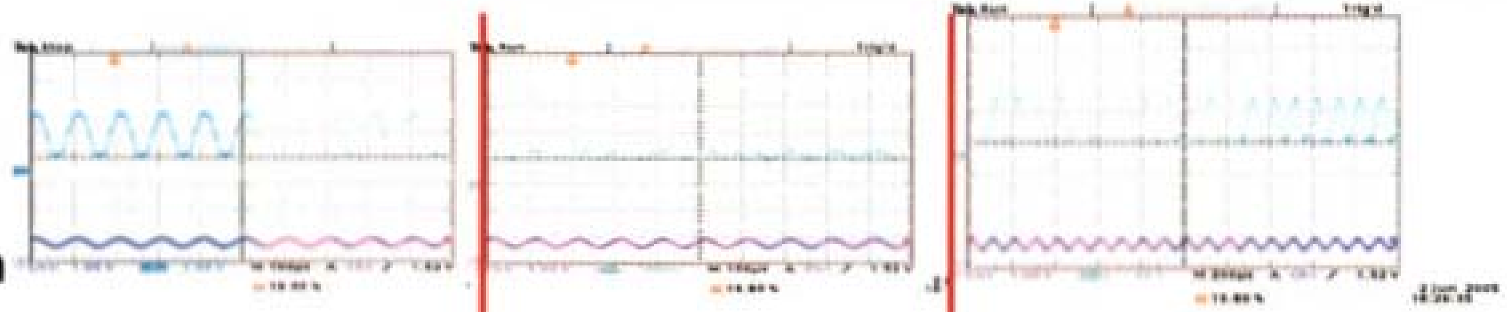


- Vb1 = 0.9V, Vb2 = 0.7V
- Filter transfer response deteriorates below -120°C.

Function Recovery at –180°C



Low Temperature – Response in the Time Domain (f = 10kHz)

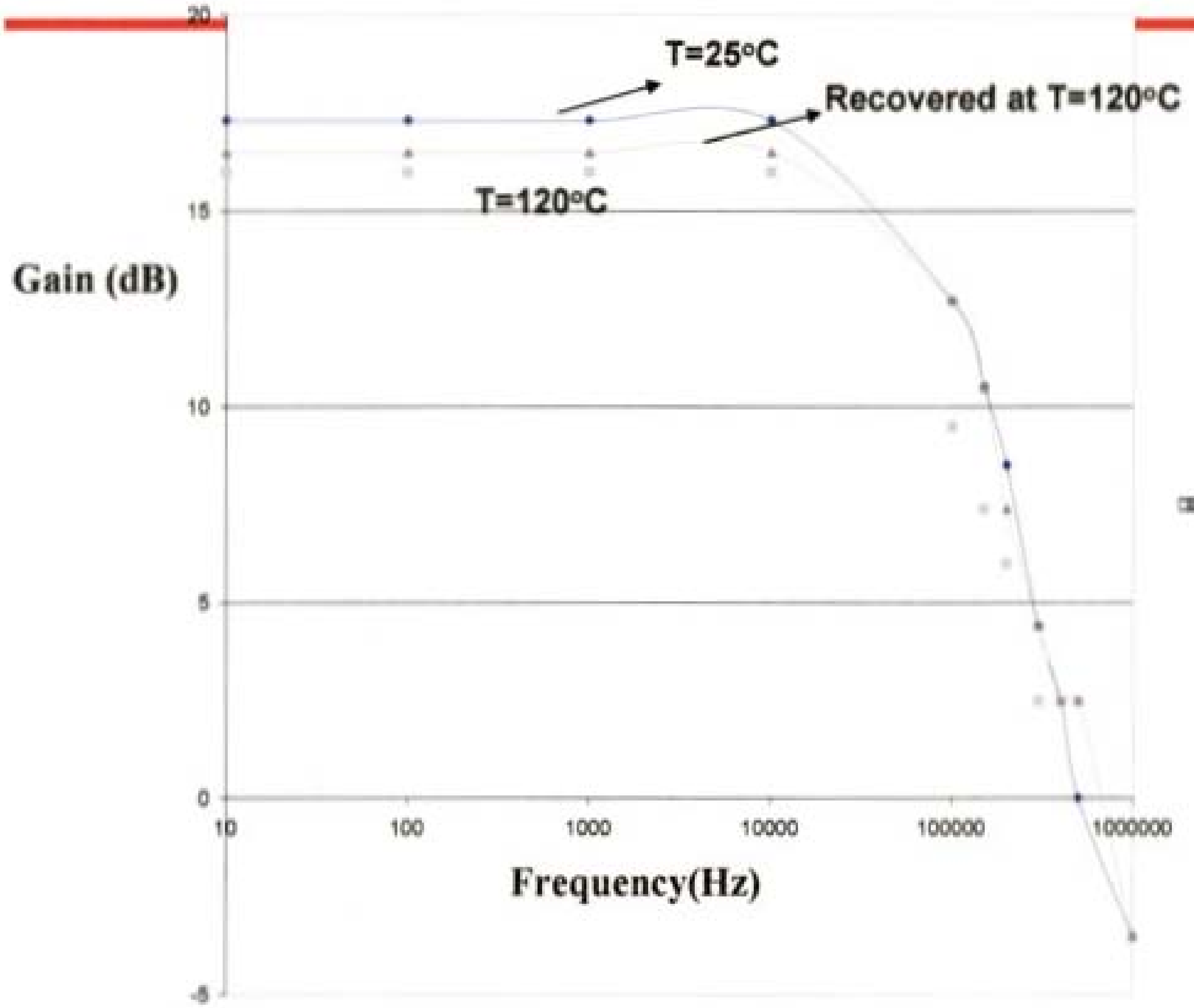


T = 25°C	T = -180°C	T = -180°C
Vb1 = 0.9V	Vb1 = 0.9V	Vb1 = 0.8V
Vb2 = 0.7V	Vb2 = 0.7V	Vb2 = 0.7V
Vout = 1.8Vp-p	Vout = 0.1Vp-p	Vout = 1.4Vp-p

Filter Recovery at –180°C

1. **Partial functionality recovery accomplished using "manual" local search over Vb1 and Vb2;**
2. **There is possibly one or more pair of values Vb1/Vb2 that produce a better recovery at –180oC ⇒ Sweep Vb1 and Vb2 using finer steps and/or implement non-local and more systematic search.**

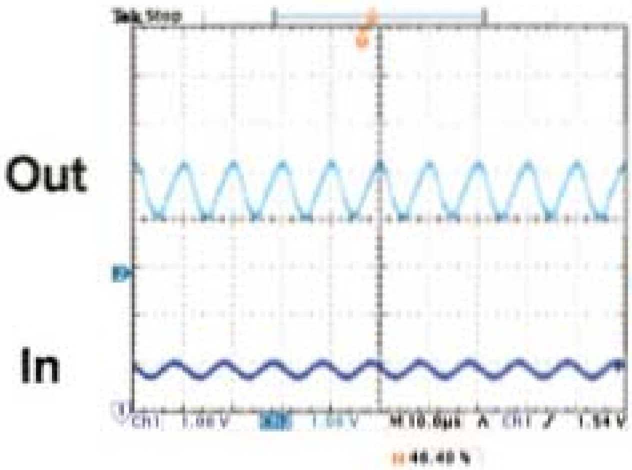
Filter Recovery at High Temperature



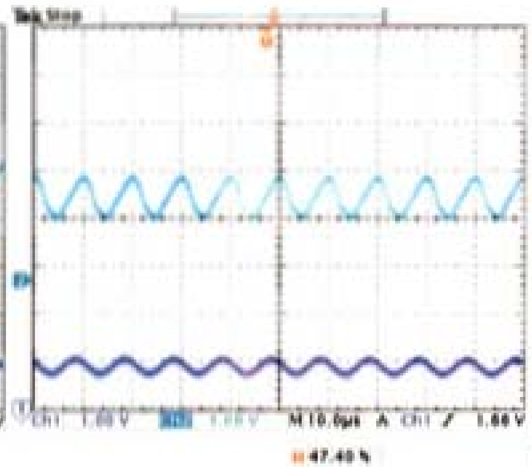
- Vb1 = 0.9V, Vb2 = 0.7V
- Filter transfer response slightly deteriorates at 120°C.

High Temperature – Response in the Time Domain (f = 100kHz)

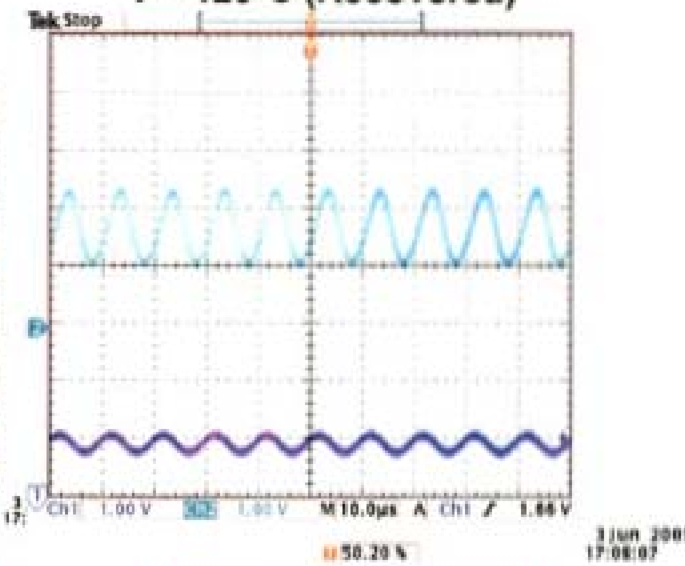
T = 25°C



T = 120°C



T = 120°C (Recovered)



T = 25°C	T = 120°C	T = 120°C
Vb1 = 0.9V	Vb1 = 0.9V	Vb1 = 1.1V
Vb2 = 0.7V	Vb2 = 0.7V	Vb2 = 0.6V
Vout = 1.3Vp-p	Vout = 0.9Vp-p	Vout = 1.3Vp-p

Conclusions

- Results indicate that bias voltage control adjustment is an efficient mechanism for circuit recovery at extreme temperatures.
  - Small changes in the bias voltage are sufficient to promote functionality recovery of the OTA and WRTA devices tested at low and high temperatures;
  - Low Pass filter recovery was also possible through changes in the bias voltages $\rightarrow$ more systematic search methods and/or algorithms needed to further improve recovered function.