Tradeoffs in Flight-Design Upset Mitigation in State-of-the-Art FPGAs

Hardened By Design vs. Design-Level Hardening

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In the beginning was Actel …

- Leveraging from a commercial product line
  - ONO anti-fuse based → one-time programmable (OTP)

- "beginning" = 1993
  - Reference:

    Katz, R.; Barto, R.; McKerracher, P.; Carkhuff, B.; Koga, R.; "SEU hardening of field programmable gate arrays (FPGAs) for space applications and device characterization," *IEEE Transactions on Nuclear Science,* Dec. 1994

Later, Xilinx

Leveraging from a commercial product line

- SRAM based → reconfigurable

"later" = 1998

- Reference: Guertin, S.M.; Swift, G.M.; Nguyen, D.; "Single-event upset test results for the Xilinx XQ1701L PROM", *Radiation Effects Data Workshop Record*, 1999
- Quote:

  (Xilinx SRAM-based FPGAs)… "do appear suited to a broad range of other (non-critical) applications, such as sensor and camera controllers."

OUTLINE

- FPGAs:
  A key enabling technology for modern spacecraft
- Background in radiation testing of FPGAs
  - Earlier, Katz/Swift collaboration
  - Recently, Xilinx Consortium
- Feature Comparison
- Triple Modular Redundancy (TMR) -
  hardware approach vs. software approach
- Concluding Remarks

FPGAs: A key "enabling technology"

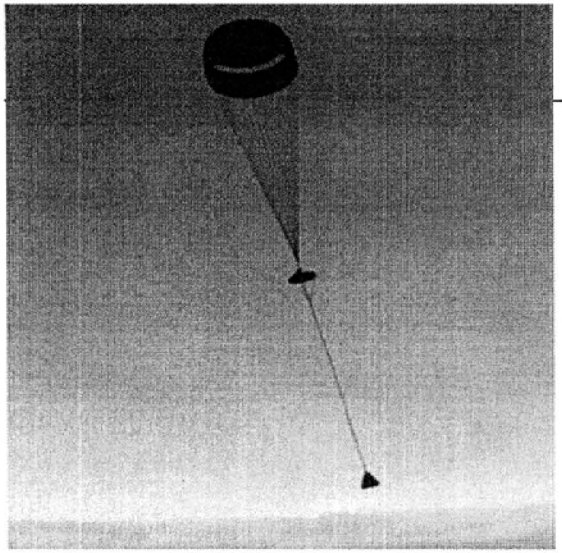
Like custom ASICs, FPGAs can replace whole boards

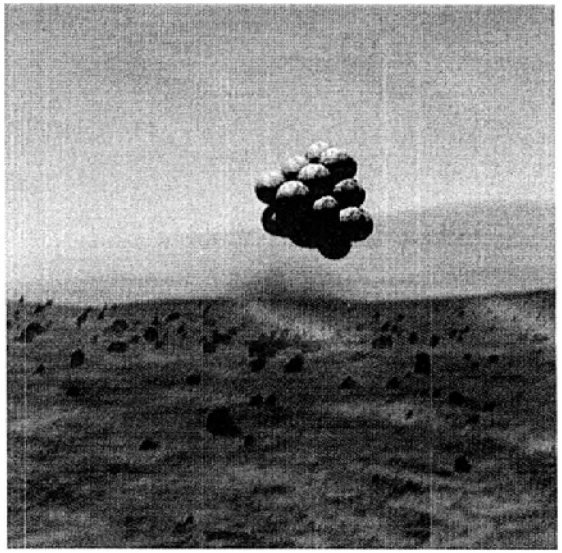
- Saving mass, volume, power
- Achieving extra functionality

FPGAs are much cheaper than ASICs

- Design efforts can be later in the schedule
- Design mistakes don't require a re-spin through the foundry

MER Pyro-Controller



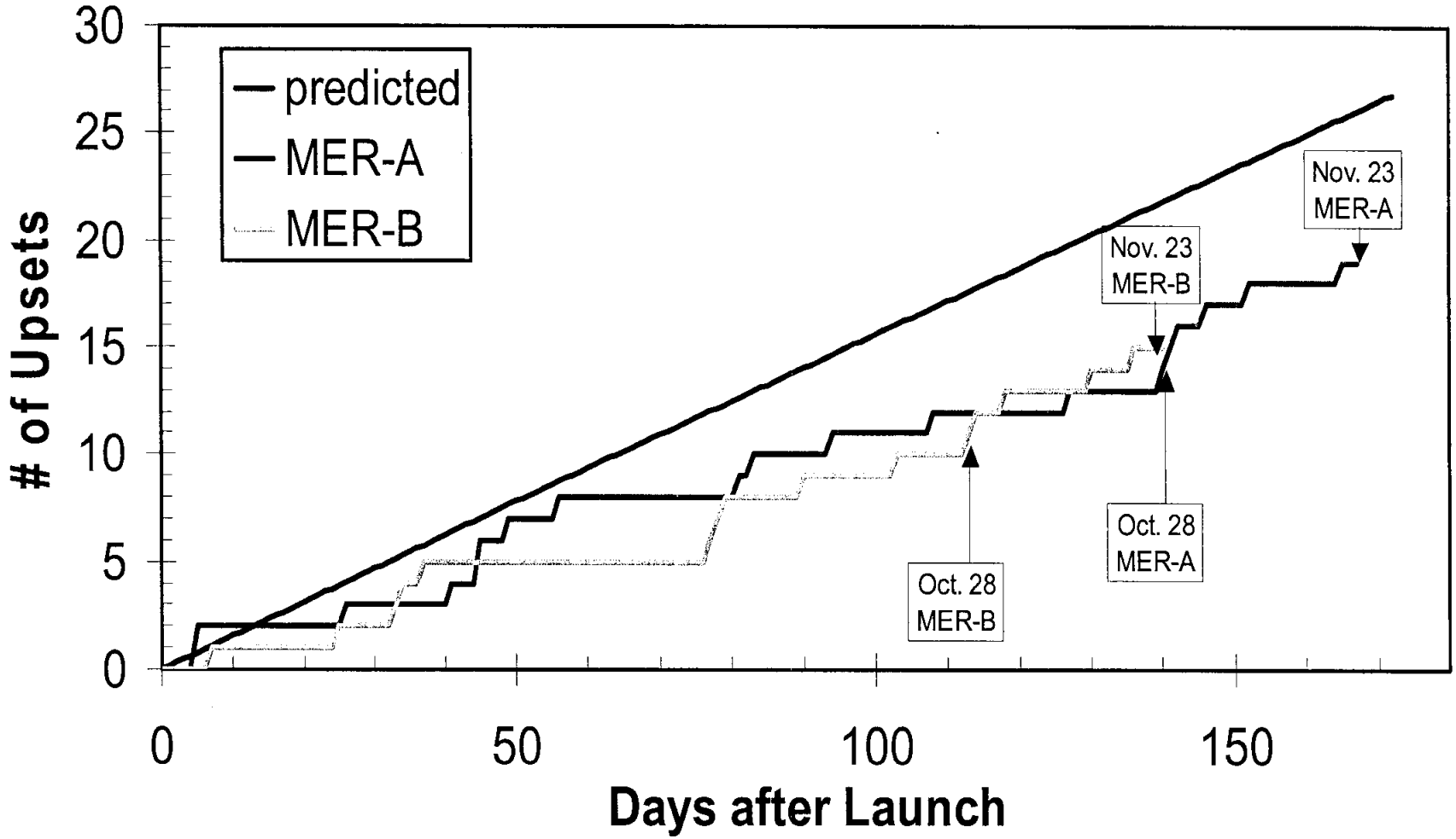


Used self-checking of configuration to initiate a re-configuration after spotting an upset

MER Pyro-Controller

Nearing Mars

Xilinx XQR4062XL



My Background

- Actel has not been directly involved in recent radiation testing
  - No direct involvement in radiation tests since the ONO anti-fuse was replaced
  - Results here are from others' work
- Xilinx experience is recent
  - Active participant in Xilinx Rad Test Consortium
  - Currently, finishing two+ year test campaign targeting the Virtex II family

Comparison of "current" devices

Actel RT54SX-S family vs. Xilinx Virtex II family

Note: both are essentially immune to single-event latchup and have good total ionizing dose tolerance,
[Actel > 135 krad(Si); Xilinx > 200 krad(Si)]

Main Feature Comparison

	Actel	Xilinx
Pins:	~550	>1000
Gates:	72,000	~6M (/~3.4)
	2012	67,584 / 3 = ~22.5k
Speed:	200 MHz	650 MHz

Extra Features Comparison

	Actel	Xilinx
BRAM:	no	2Mb
I/O Standards:	many	many
Others:	hardwired TMR	Clock Manager Multipliers

Actel: What bits can upset?

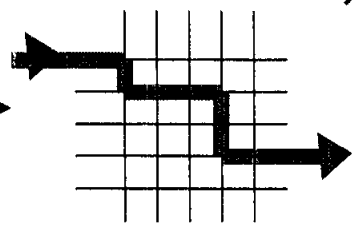
User flip-flops only

- Direct hits of same flip/flop in multiple domains
  - Very unlikely due to layout
- Clock domain hits

SEFI modes essentially eliminated

Xilinx: What bits can upset?

- Configuration Bits
  - Logical Function
  - Routing
  - User Options

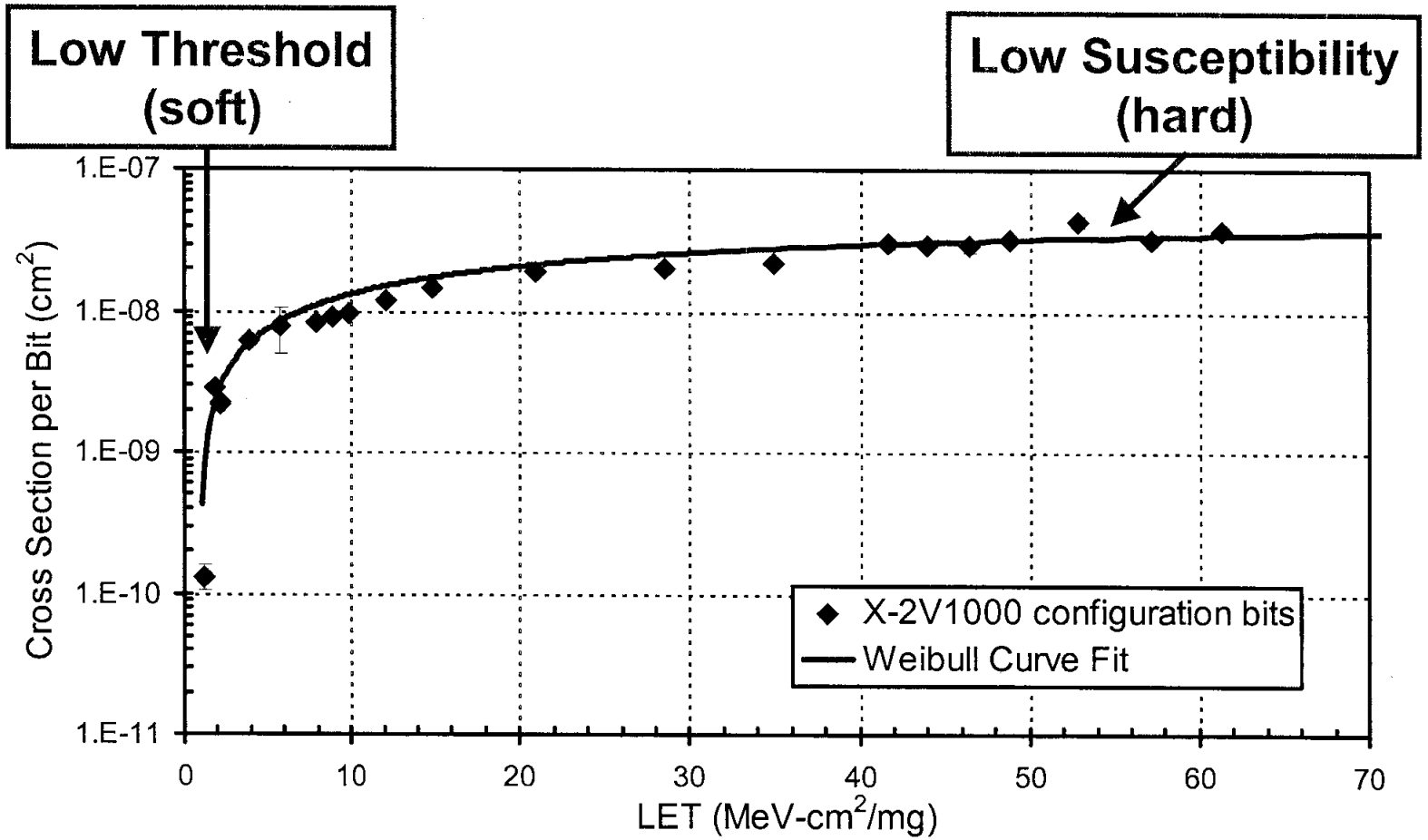


× NAND
× Ex-OR
× Flip-Flop type
× etc...

× Type of I/O
× Mode of BRAM Access
× Clock Manager
× etc...

- BRAM
- User Flip-flops
- Control Registers

Xilinx: In-beam Test Results



Resulting in fairly low in-space rates

e.g., rate for 2V1000 in GCR_{min} is 1 per day.

Actel-style TMR

Actel-style TMR is straightforward:

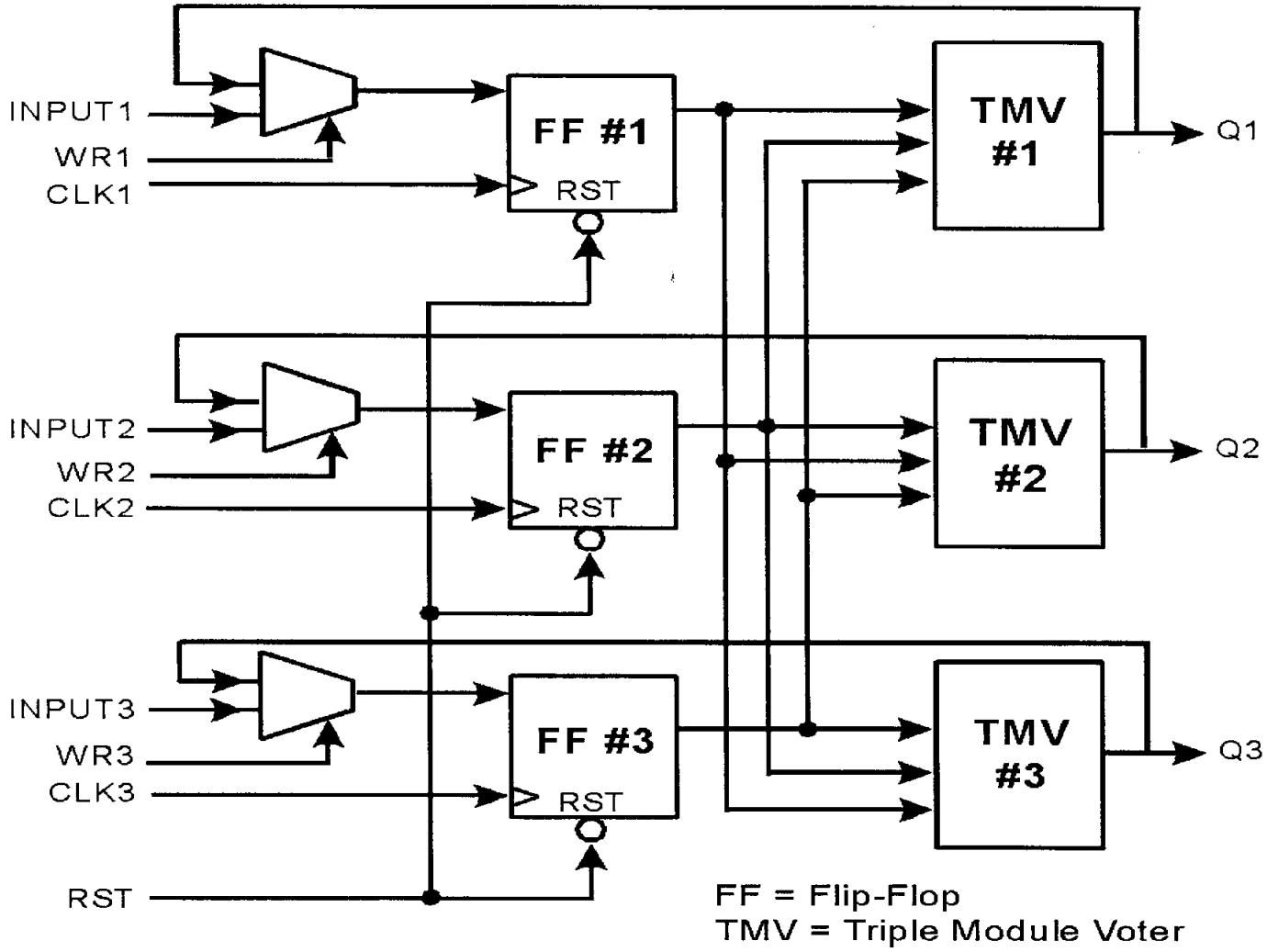
- Each flip-flop is replaced by three plus a voter
- Uses one clock domain
- No external parts

Xilinx-style TMR

Xilinx-style TMR is more complicated:

- First, it's not too useful without configuration scrubbing
- Whole functional blocks are triplicated, *not* individual flip-flops,
- Three voters are used
- Three clock domains
- Elimination of:
  - Weak keepers (aka half latches)
  - Use of configuration cells as part of the design
    - For example, SRL16
- Needs some external circuitry (at least, a watchdog timer)

Xilinx-style TMR



Xilinx TMRtool

- Xilinx-style TMR done by hand is difficult and tedious
- An automated tool which integrates into the design flow has been developed ("now" available)
- In-beam testing shows tools is very effective

Upset Comparison

- ATMR now has eliminated:
  - Upsets of static storage elements, and
  - SEFIs
- ATMR upsets from:
  - Transients that are clocked into storage
  - Clock tree hits

- Xilinx FPGAs have a small susceptibility to two types of SEFIs
  - Reset (sometimes only partial)
  - Disable scrub port
- XTMR in combination with scrubbing can lower system upset rates below the SEFI rate

Rate Comparison

- Actel
  - Dominated by transients
  - Roughly a system error per few thousand years (GCR)

- Xilinx
  - Dominated by SEFI rate
  - Expect one in 65 years in GCR

GCR = **G**alactic **C**osmic **R**ay background (interplanetary space)
almost identical to geosynchronous orbit

CONCLUSIONS

For the present –

Both can achieve very acceptable radiation tolerance

Actel wins on:

- Less burden on the designer
- No auxiliary components
- Lower SEFI susceptibility

Xilinx wins on:

- Designer control of the resources vs. hardness tradeoff
- On-chip feature set
- Re-configurability

Competition is good.

Acronyms

FPGA - Field Programmable Gate Array

ASIC - Application Specific Integrated Circuit

SEU - Single Event Upset

SEFI - Single Event Functionality Interrupt

TMR - Triple Modular Redundancy

ATMR - Actel-style TMR

XTMR - Xilinx-style TMR

A.U. - Astronomical Unit (earth-sun distance)

MER - Mars Exploration Rovers
(i.e., Spirit and Opportunity)

Additional References

[1] Katz, R.; Wang, J.; McCollum, J.; Cronquist, B.; "The impact of software and CAE tools on SEU in field programmable gate arrays," *IEEE Transactions on Nuclear Science,* Dec. 1999

[2] Jih-Jong Wang; Katz, R.B.; Dhaoui, F.; McCollum, J.L.; Wong, W.; Cronquist, B.E.; Lambertson, R.T.; Hamdy, E.; Kleyner, I.; Parker, W.; "Clock buffer circuit soft errors in antifuse-based field programmable gate arrays," *IEEE Transactions on Nuclear Science*, Dec. 2000

[3] Wang, J.J.; Wong, W.; Wolday, S.; Cronquist, B.; McCollum, J.; Katz, R.; Kleyner, I.; "Single event upset and hardening in 0.15 /spl mu/m antifuse-based field programmable gate array," *IEEE Transactions on Nuclear Science*, Dec. 2003