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Ultra-low-temperature homoepitaxial growth of Sb-doped silicon

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Abstract

An ultra-low-temperature process for homoepitaxial growth of high-quality, surface-confined, Sb-doped silicon layers is presented. Non-equilibrium growth by molecular beam epitaxy (MBE) is used to achieve dopant incorporation in excess of $2\times10^{14}\,cm^{-2}$ in a thin, surface-confined layer. Sb surface segregation larger than expected from theoretical models was observed, in agreement with other experimental works. Furthermore, this work details an entirely low-temperature process (<450 °C) that can be applied to fully processed and aluminum-metallized silicon devices. One application of this process is the formation of a back-surface electrode for back-illuminated high-purity silicon imaging arrays.
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1. Introduction

Antimony (Sb) delta doping by low-temperature molecular beam epitaxy (MBE) of silicon has received much attention for device applications where sharp and well-controlled n-type dopant distribution profiles are required, such as tunnel diodes [1] and heterojunction bipolar transistors [2,3]. However, the elevated growth temperatures thus far required for high-quality epitaxy exclude applications requiring growth on fully fabricated devices containing aluminum metallization. These devices cannot be subjected to temperatures greater than 450 °C to prevent Al spiking in silicon. One such low-temperature application that we explore in detail elsewhere is Sb doping of back-illuminated high-purity silicon imaging arrays [4].

The creation of sharp n-type dopant profiles in silicon during growth is challenging due to the high surface segregation ratio of the common n-type dopants Sb, P, and As [5,6]. Of these dopants,

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Sb is the most commonly used and has a lower surface segregation than P and As. The interaction of Sb with the silicon surface is a subject of great interest and much debate, and has been widely studied for growth of germanium and Si_xGe_{1-x} as well as silicon [7–10]. At moderate temperatures, Sb acts as a surfactant and at low temperatures, Sb can be incorporated as an n-type dopant. When evaporated from a solid source, Sb is present in the vapor phase as the precursor Sb_4. Studies on the kinetics of molecular adsorption and dissociation have revealed a complex reaction path leading to the formation of multiple Sb dimer configurations on the Si(0 0 1) surface [11]. Conversion of Sb_4 to these dimer states has been observed even at very low temperatures. Despite its wide use, controversy still exists over the structure of the surface induced by Sb adsorption on Si(0 0 1) [12–15]. The complex structure of this surface may explain the unexpected behavior of Sb on Si at low temperatures that results in larger than expected surface segregation.

The tendency of Sb to segregate to the surface during growth favors its use as a surfactant, and therefore, low-temperature growth is required to ensure incorporation of Sb in the Si lattice. Even so, it has been found that Sb surface segregation at low temperatures (250–400 °C) can be as much as two orders of magnitude larger than expected values based on extrapolation from high-temperature data [16–19]. Several explanations for this large segregation have been suggested, including surface roughening [18] and local heating [19]. To overcome the segregation problem encountered in growth of sharp Sb profiles, several approaches have been tried, including solid-phase epitaxy (SPE) [20–22], ion implantation and annealing [23], and ultra-low-temperature MBE [17]. However, the MBE growth techniques that have been implemented to date have required a high-temperature ($\geqslant 550$ °C) silicon buffer layer. This work demonstrates that sharp Sb profiles and high electrical activation of Sb can be achieved at low temperatures suitable for growth on aluminum-metallized devices by taking advantage of surface preparation techniques [24] that make it possible to grow low-temperature buffer layers (< 450 °C). To the best of our knowledge, this is the first entirely low-temperature growth process for Sb-doped silicon.

2. Experiment

2.1. Surface preparation

Surface preparation is critical to low-temperature silicon growth, requiring complete removal of the native oxide and stable surface termination. High-purity Si(0 0 1) wafers (n-type $>4000\,\Omega$ cm) are treated with (1) hot 4:1 H_2SO_4:H_2O_2 for 10 min, (2) 10:1 H_2O:HF for 1 min, (3) hot 1:6:1 HCl:H_2O:H_2O_2 for 10 min, and (4) 10:1 H_2O:HF for 1 min. A rinse with de-ionized water follows each of these cleaning steps. Oxide removal and hydrogen surface termination are accomplished by a spin etch at 2500 RPM in a nitrogen dry box with (1) ethanol, (2)1:5 HF:ethanol, and (3) a final ethanol rinse. Wafers are transferred into the MBE system through the dry box, without further exposure to air.

For growth on metallized devices, the surfaces are prepared differently in order to protect the front-side circuitry. A typical imaging device will be back-illuminated, and will have a patterned front surface containing Al metallization. Sb doping by MBE will be applied to the silicon back surface. Devices are first mounted with wax to protect the front side and are given two RCA-type cleans: 10 min each in 5:1:3 H_2O:H_2O_2:NH_4OH and 4:1:1 H_2O:HCl:H_2O_2. The wax is then removed with xylene and devices are solvent cleaned for 10 min each at 65 °C in xylene, EKC505 Cu photoresist stripper, IPA, and 3 min each at 65 °C in xylene and Transene 100. They are then transferred to a nitrogen dry box for a 10-min UV ozone exposure followed by the spin etch procedure described above to achieve hydrogen termination. They are then transferred from the dry box directly into the MBE system without exposure to atmosphere.

2.2. Growth and characterization

Epitaxial silicon growth is performed in a Riber EVA 32 Si MBE system with a base pressure of 1×10^{-10} Torr. Two-inch silicon wafers are

mounted in a molybdenum holder and backed by a sapphire diffuser plate for radiative sample heating. Devices are mounted in a similar manner, and are held in place using machined silicon fixtures, such that the device does not contact the molybdenum holder. Silicon is supplied by an e-beam source at a deposition rate of $0.4\,\text{Å}\,s^{-1}$. Sb is supplied by a Knudsen cell heated to ~320 °C corresponding to a flux of $\sim 1.5\times 10^{12}\,cm^{-2}\,s^{-1}$. The substrate is heated to 450 °C using a slow ramp with low-temperature soak steps designed to drive off hydrocarbons [24]. An undoped Si buffer layer, typically between 25 and 150 Å thick, is deposited at 450 °C. The substrate temperature is then lowered at $\sim 8\,°C\,min^{-1}$ for the Sb and Si cap layer deposition. When the target substrate temperature is reached (typically ~300 °C), the Sb shutter is opened to expose the wafer to the desired Sb dose, typically ~0.4 ML. The Sb shutter is then closed, and a silicon cap layer is deposited at a rate of $0.4\,\text{Å}\,s^{-1}$.

Surfaces were characterized by in situ reflection high-energy electron diffraction (RHEED) using a 10 keV electron gun. Quadrupole SIMS analysis was performed by Charles Evans and Associates using a 500 eV Cs+ ion beam impinging on the sample at an angle of 60°. Hall effect measurements were performed using the Van der Pauw configuration with indium contacts and a field strength of 0.2 T. X-ray photoemission spectroscopy (XPS) was performed in a UHV chamber with a base pressure of 10^{-10} Torr, using monochromatic Al Kα X-rays (1486.6 eV) at ambient temperature with photoemission 55° from the surface normal.

2.3. Temperature calibration

During MBE growth, the sample is radiatively heated. The thermocouple is not in contact with the wafer, and therefore, several other methods were used to obtain accurate growth temperatures, namely infrared pyrometer readings, observations of 2×1 surface reconstruction (~450 °C), and observations of the Al–Si eutectic transformation (577 °C). The temperature of the sample depends on the surface reflectivity, doping level, and thickness. Therefore, separate calibrations were performed for each type of wafer and device structure. RHEED observations of crystal quality during growth as well as SIMS were used to compare device growths to wafer growths. Any discrepancy in temperature would manifest itself in a difference in Sb segregation. Such differences were not observed and the calibrated temperature is considered accurate to ±10°.

3. Results and discussion

3.1. Surface preparation

XPS was used to determine surface contamination levels. Silicon wafers undergo a more rigorous cleaning process than devices and are expected to exhibit similar or better levels of surface contamination. As a worst case, XPS was used to characterize the surface of a high-resistivity silicon p–i–n diode after undergoing the cleaning process described in the previous section. The resulting spectrum is shown in Fig. 1. Only minimal amounts of C, O, and F are present, comparable to data in the literature on silicon wafer surfaces prepared for low-temperature MBE growth [25].

3.2. Growth on high-purity Si wafers

3.2.1. RHEED

RHEED was used to monitor the silicon surface during growth. At room temperature, the

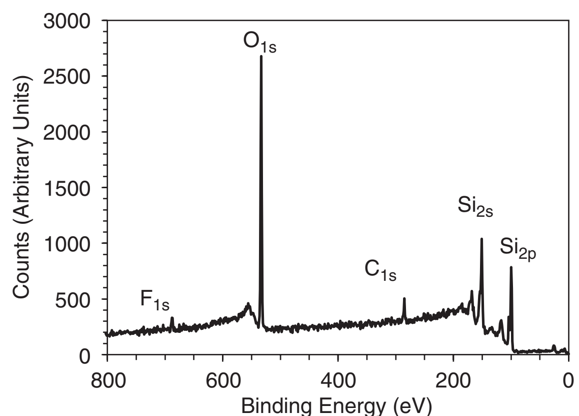

Fig. 1. XPS spectrum of a clean high-purity n-type Si(0 0 1) surface after HF:ethanol spin etch.

hydrogen-terminated surface exhibits a 1×1 surface reconstruction visible with RHEED. The substrate is heated before growth to drive off the hydrogen and form a reconstructed Si surface. As the substrate approaches 430 °C, surface silicon atoms begin to form dimers and 2×1 surface reconstruction becomes visible. The silicon buffer layer can then be grown. After Sb exposure, the second-order spots become faint. A 1 ML surface coverage of Sb would exhibit a reconstruction that appears to be 1×1 even though Sb forms dimers; this can be explained by the 'disordered dimer' surface suggested by Pulci et al. [13] which is actually a mixture of 2×1 and 2×2 dimer geometries. At less than 1 ML, Sb surface coverage we would expect to see a mixture of apparent 1×1 (from Sb) and 2×1 (from Si) patterns which correlates well with the weakening of the second-order spots observed in the RHEED patterns after Sb exposure. After deposition of the low-temperature silicon cap layer, the 2×1 reconstruction of the silicon surface will return as evidenced in the RHEED patterns shown in Fig. 2. The 2×1 reconstruction is strongest for cap layers grown at higher temperatures where the Sb diffuses into the silicon cap to a large extent, indicating that the cap layer is of higher crystalline quality when grown at higher temperatures as expected. At very low temperature, 265 °C, the crystalline quality starts to break down and the RHEED pattern indicates 3D growth with some twinning visible. It was also found that Sb surface segregation was persistent at 265 °C as expected and nothing was gained by lowering the temperature by this amount (SIMS results showed similar profiles for 300 and 265 °C, as discussed in the following section). At even lower growth temperatures, the silicon cap is amorphous and Sb is no longer electrically active. The growth temperature chosen therefore represents a compromise between dopant activation which is poor at low temperatures and dopant segregation which is enhanced at high temperatures.

3.3. SIMS

SIMS was used to determine the total Sb dose as well as the extent of Sb segregation into the silicon cap layer. Fig. 3 shows that surface segregation is prevalent at higher temperatures (380 °C). A temperature of ~300 °C was chosen for the majority of the growths since no significant advantage was gained by going to even lower temperatures. The Sb concentration FWHM for the 300 °C growth is ~35 Å. Because the peak concentration is high ($\sim7\times10^{20}\,\text{cm}^{-3}$), the Sb could potentially be placed <35 Å from the surface while maintaining sufficient conductivity, even though some Sb is lost to surface segregation. The limit will occur when too much Sb is lost to the surface. In a device, this would manifest itself in a poor conductivity and high surface dark current. A study of this limit will be a subject of future work.

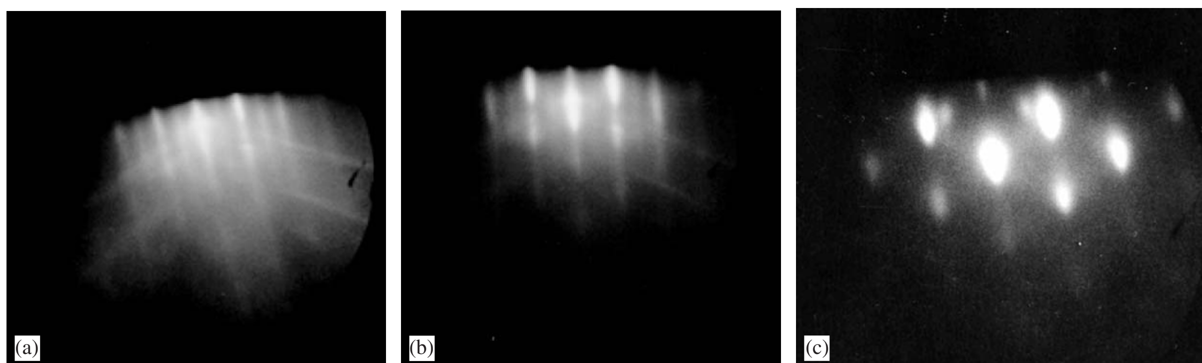

Fig. 2. RHEED patterns after (a) 0.8 ML Sb and 200 Å Si cap at 380 °C, (b) 0.4 ML Sb and 150 Å Si cap at 300 °C, and (c) 0.4ML Sb and 150 Å Si cap at 265 °C.

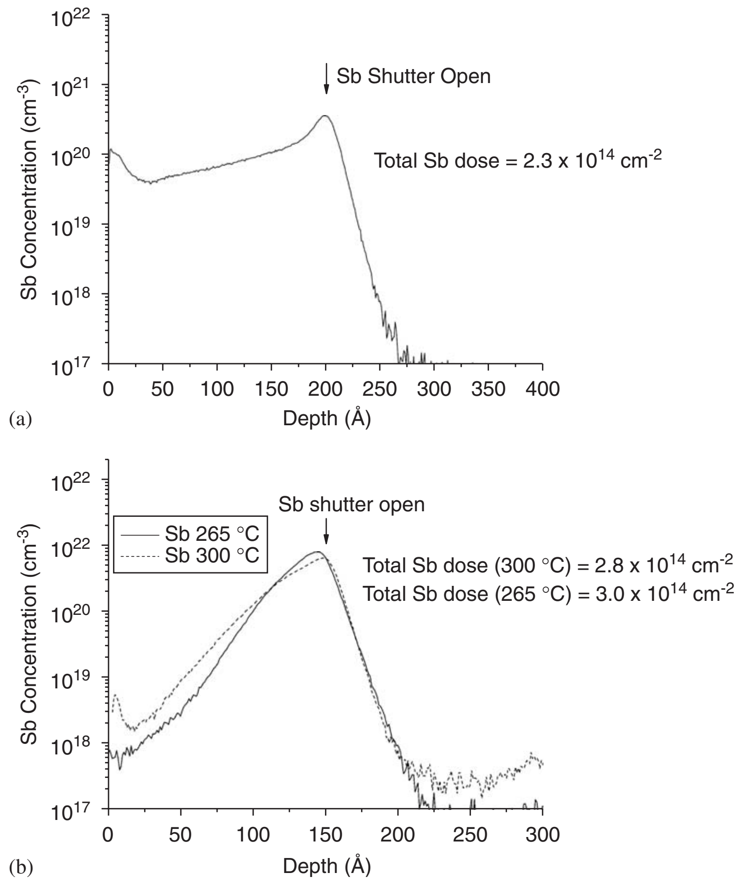

Fig. 3. SIMS of Sb-doped layer grown at (a) 380 °C with 0.8 ML Sb and 200 Å cap and (b) 265 °C and 300 °C with 0.4 ML Sb and 150 Å cap (note: *x*-axis is shifted to line up peaks).

The surface segregation ratio of Sb can be calculated using the SIMS results as described by Hobart et al. [16]. The surface segregation ratio is defined by

$$r_{\mathrm{Sb}} = \frac{\theta_{\mathrm{Sb}}}{\gamma_{\mathrm{Sb}}}, \quad (1)$$

where θ_{Sb} is the Sb surface coverage relative to the Si(0 0 1) surface and γ_{Sb} is the bulk Sb fraction at a given depth, both found from SIMS.

Fig. 4 shows our results plotted along with results from the literature. The kinetic two-state exchange model from Jorke [26] (theoretical curve) is shown alongside the data. The discrepancy between measurements and theory in the low-temperature regime has been known for some time, indicating that a simple two-state exchange kinetically limited model is not accurate in describing low-temperature segregation. It has been suggested by Jiang et al. [18] that surface roughening could enhance the surface exchange process leading to increased segregation at low temperatures. Our data is in agreement with that of Hobart and Jiang, all showing significantly higher surface segregation at low temperatures.

3.4. Hall effect

Hall effect measurements shown in Fig. 5 were used to determine the electrical properties of the

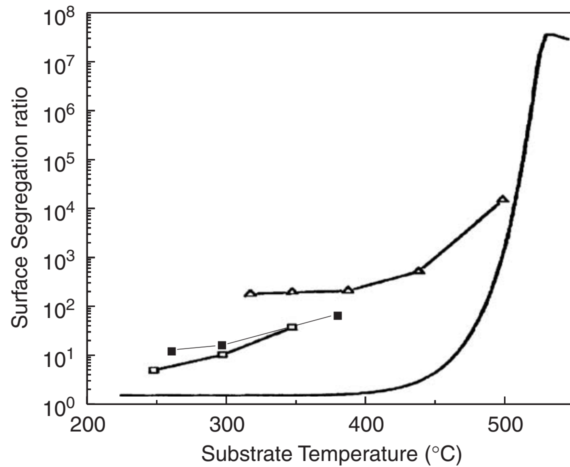

Fig. 4. Surface segregation ratio of Sb as a function of substrate temperature during growth. Our data (■), data from Jiang et al. (□), data from Hobart et al. (△), and theoretical curve from Jorke et al. (solid curve).

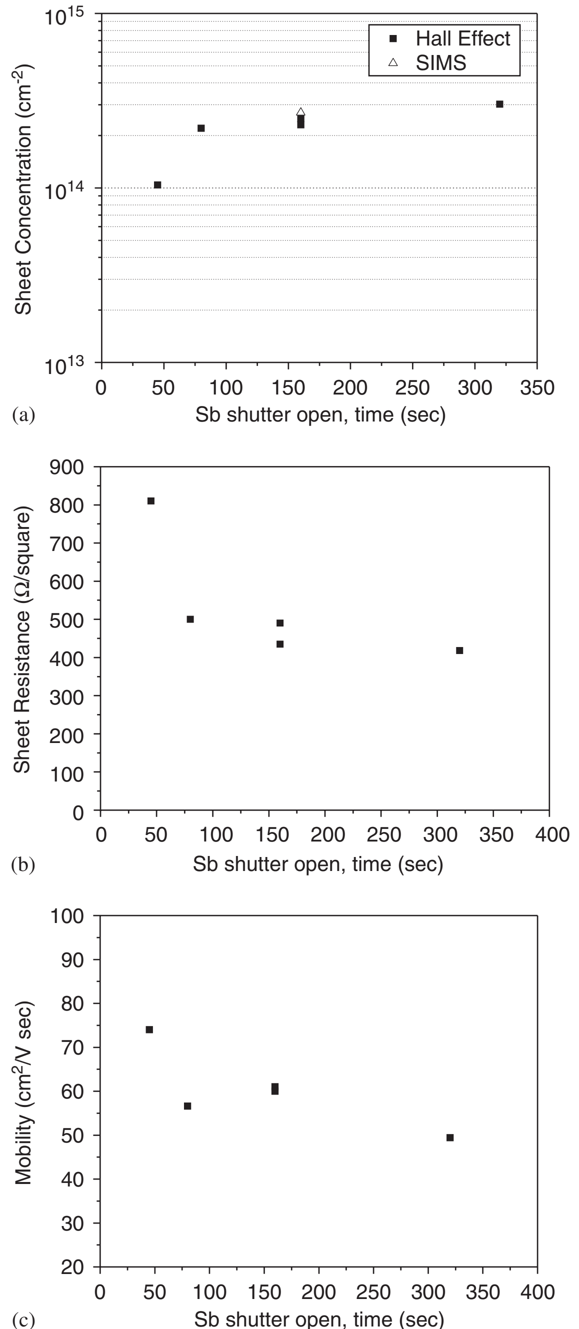

Fig. 5. Hall effect measurements of Sb-doped layers with 150 Å Si cap layers on high-purity n-type silicon wafers showing (a) sheet concentration (with concentration obtained from SIMS also shown), (b) sheet resistance, and (c) mobility with increasing Sb exposure time at an Sb flux of $1.5 \times 10^{12}\,cm^{-2}\,s^{-1}$.

Sb layers. While MBE growth allows for much higher Sb incorporation than equilibrium growth, it is expected that electrical activation of the donors will decrease for high Sb exposure. With increasing Sb exposure, the activated dose, sheet resistance, and mobility saturate. At 160 s exposure time, the Sb is ~85% activated as determined by comparing Hall effect and SIMS results with an activated dose $\sim 2 \times 10^{14}\,cm^{-2}$.

3.5. Growth on devices

The Sb doping process was applied to both photodiode test structures and 1k × 1k CCDs fabricated at Lawrence Berkeley National Laboratory (LBNL) and DALSA semiconductor. Details of these devices are described elsewhere [27,28]. Testing of photodiodes and CCDs with MBE-grown Sb layers indicates that a thin low-temperature back surface contact with low leakage current can be successfully formed. A characteristic test pattern image from an Sb-doped CCD is shown in Fig. 6. The CCDs with Sb-doped MBE layers have exhibited low dark current and high response. Details of the detector characterization are described elsewhere [4].

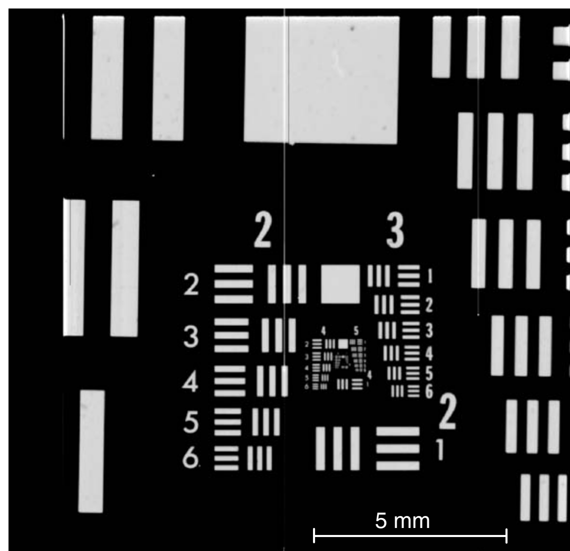

Fig. 6. (a) –140 °C test pattern image taken with a 250-μm-thick, back-illuminated, 1230 × 1170, 12 μm pixel LBNL CCD, with backside Sb doping by MBE. Substrate bias = 45 V. A vertical short unrelated to the MBE process is visible down the center of the image.

4. Conclusions

Using low-temperature MBE, a new process has been developed for creating sharp Sb dopant profiles entirely at low temperature. The growth consists of a silicon buffer layer deposited at ~450 °C, ~0.4 ML Sb exposure, and a silicon cap grown at ~300 °C. Using this temperature profile, an Sb layer with high electrical activation can be confined to 35 Å. This process can be applied to Al-metallized devices, for example, high-resistivity n-type silicon detector arrays.

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