

National Aeronautics and Space Administration



# **Guideline for Ground Radiation Testing of Microprocessors in the Space Radiation Environment**

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JPL Publication 08-13 4/08





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NASA Electronic Parts and Packaging (NEPP) Program  
Office of Safety and Mission Assurance

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NASA WBS: 939904.01.11.30  
JPL Project Number: 102197  
Task Number: 3.34.7

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This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

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<b>I.</b>	<b>Introduction .....</b>	<b>1</b>
<b>II.</b>	<b>Microprocessors .....</b>	<b>2</b>
	<i>II.A Overview .....</i>	<i>2</i>
	<i>II.B Microprocessor Types Addressed in this Guide.....</i>	<i>2</i>
	<i>II.C Performance and Processing Evolution.....</i>	<i>3</i>
	<i>II.D Configuration Requirements .....</i>	<i>4</i>
	<i>II.E Packaging .....</i>	<i>5</i>
	<i>II.F Thermal Issues .....</i>	<i>6</i>
<b>III.</b>	<b>Radiation Induced Effects in Microprocessors.....</b>	<b>7</b>
	<i>III.A Introduction to Basic Radiation Effects.....</i>	<i>7</i>
	<i>III.B Early Test Approaches for Microprocessors.....</i>	<i>9</i>
	<i>III.C Test Approaches for High-Performance Microprocessors.....</i>	<i>11</i>
	III.C.1 Operating Systems .....	11
	III.C.2 Test Methods.....	13
	III.C.2.1 Register-Level Tests .....	13
	III.C.2.1.A Semi-Static .....	14
	III.C.2.1.B Semi-Dynamic .....	15
	III.C.2.2 Tests of Internal Cache .....	15
	III.C.2.3 Operational Software Tests.....	16
	III.C.2.4 Program Hangs .....	17
<b>IV.</b>	<b>Beam Requirements .....</b>	<b>19</b>
	<i>IV.A Heavy Ions Beams .....</i>	<i>19</i>
	IV.A.1 Heavy Ion Beams Available at Various Accelerators .....	19
	<i>IV.B Proton Beam.....</i>	<i>24</i>
<b>V.</b>	<b>Steps Required for Microprocessor Radiation Testing.....</b>	<b>25</b>
	<i>V.A Device Properties and Physical Preparation .....</i>	<i>25</i>
	<i>V.B Hardware Requirements .....</i>	<i>25</i>
	<i>V.C Operating System and Software.....</i>	<i>25</i>
	<i>V.D Testing.....</i>	<i>25</i>
<b>VI.</b>	<b>Reporting and Interpretation of Results .....</b>	<b>27</b>
	<i>VI.A General Issues .....</i>	<i>27</i>
	<i>VI.B Register and Cache Tests .....</i>	<i>27</i>
	<i>VI.C Functional Errors, Hangs, and Crashes.....</i>	<i>27</i>
<b>VII.</b>	<b>Test Results for Highly Scaled Microprocessors .....</b>	<b>29</b>
	<i>VII.A Registers and Cache.....</i>	<i>29</i>

VII.A.1	PowerPC Microprocessors.....	29
VII.A.2	Intel Processors.....	30
VII.B	<i>Frequency Dependence of Registers and Cache</i> .....	33
<b>VIII.</b>	<b>Conclusion</b> .....	<b>37</b>
<b>IX.</b>	<b>Acknowledgments</b> .....	<b>41</b>
<b>X.</b>	<b>References</b> .....	<b>42</b>

# **Guideline for Ground Radiation Testing of Microprocessors in the Space Radiation Environment**

## **I. Introduction**

Single-event effects can be a significant problem for devices operating in space, particularly for microprocessors because of their complexity. Radiation tests are often required in order to allow estimates of upset rates caused by space radiation. The test results help to determine what kinds of effects are produced and how they can be detected and overcome. Complex failure modes are of particular interest because they potentially limit ways in which errors and malfunctions can be detected and corrected by hardware or software techniques.

In recent years there has been increased interest in the possible use of unhardened commercial microprocessors in space because they operate at higher speed and have superior electrical performance compared to hardened processors. However, unhardened devices are susceptible to upset and degradation from radiation and more information is needed on how they respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, and the majority of them have been older device types which are designed with much larger feature sizes and higher operating voltages than modern devices [1-22].

The goal of this work is to develop a guideline that is applicable to processors that are potentially useful in space. Thus, the guideline does not consider very high performance processors that are intended for server or high-performance applications where very large amounts of power are tolerated to gain performance because it would be impractical to use such high-power devices in typical space applications.

This guide is intended to support insertion of these microprocessors into spaceflight applications and to recommend ground test protocols. The first guideline principle that should be followed is a serious concurrent engineering approach for down selecting space-qualified microprocessors. This requires that the design engineer seek the support of a radiation effects expert who understands total ionizing dose (TID) and single-event effects (SEEs) issues for microprocessors as applied to the system in question.

This guide assumes that the radiation effects expert has a working knowledge of the practices outlined in the three documents listed below. It uses terms and builds on procedures defined in these documents.

1. ASTM Guide F1192-00—Standard guide for the measurement of single event phenomena (SEP) induced by heavy ion irradiating of semiconductor devices [F1192M]
2. JEDEC heavy ion testing guideline [JEDEC HI]
3. ASTM Standard 883: Test Method 1019.5 [1019.5]

## **II. Microprocessors**

### **II.A Overview**

This document is intended to be a guideline for radiation tests of microprocessors, in particular advanced commercial microprocessors, which have been the subject of several studies during the last 20 years [1-22]. The main emphasis is on single-event upset testing, first because microprocessors are highly sensitive to single-event upset effects and, second, because there are many technical challenges in performing such tests on modern microprocessors. Total dose testing is addressed only briefly, noting that most microprocessors are relatively immune to total dose damage because of the inherent effects of scaling on device design and radiation response.

Although the results are applicable to hardened microprocessors, the main focus is on high-performance commercial microprocessors. These devices are evolving very rapidly because of performance pressure in the high-volume commercial marketplace. Feature sizes of commercial microprocessors are now at the 90 nm node with 65 nm soon to come, and processors are available that operate at clock frequencies of several GHz, providing much higher performance compared to hardened processors.

There is considerable interest in evaluating single-event upset effects at high frequency. Some of the initial work on frequency effects and radiation testing will be discussed. However, the document will not make specific recommendations on testing devices at very high frequency because of the difficulties associated with board design and dealing with the very high power dissipation at high frequency (CMOS power dissipation is essentially proportional to frequency). Test fixture difficulties and power dissipation both act as interferences when tests are done at very high frequencies.

The first part of the document discusses the main technical issues that need to be considered for planning, executing and interpreting microprocessor radiation tests. A relatively sophisticated understanding of those points is essential before the details that are relevant for the guideline can be discussed. Specific recommendations and approaches for radiation tests are included at the end of the document, along with a discussion of unresolved issues.

### **II.B Microprocessor Types Addressed in this Guide**

In recent years there has been increased interest in the possible use of unhardened commercial microprocessors in space because they operate at higher speeds and have superior electrical performance compared to hardened processors. Henceforth, the main focus of this guideline is on high-performance commercial microprocessors. Those devices are evolving very rapidly because of performance pressure in the high-volume commercial marketplace.

A basic method for improving the SEE immunity without degrading the performance is to reduce the SEE-sensitive volume. This can be accomplished through the use of silicon-on-insulator (SOI) substrates. For SOI processes the charge collection depth for normally incident ions is reduced by more than an order of magnitude compared to similar processes fabricated on epitaxial substrates. Because of the much smaller charge collection depth, the single-event upset (SEU) sensitivity of SOI devices is expected to be much reduced. However, other factors, such as lower operating voltages, reduced junction capacitance and amplification by parasitic bipolar transistors [23] may limit the degree of improvement in SEE sensitivity that can be obtained with commercial SOI processors. Commercial microprocessors with the PowerPC architecture are now available that use partially depleted silicon-on-insulator processes to improve performance. Partially depleted silicon-on-insulator processes use a tub depth between 0.09 and 0.18  $\mu\text{m}$  [24], reducing the charge collection depth for

normally incident ions by more than an order of magnitude compared to similar processes with conventional isolation (on thin epitaxial substrates).

The trend for commercial SOI microprocessors is to reduce feature size and internal core voltage and increase the clock frequency. Commercial microprocessors with the PowerPC architecture are now available that use partially depleted SOI processes with a feature size of 90 nm and an internal core voltage as low as 1.0 V and a clock frequency in the GHz range.

A recent study of first-generation SOI microprocessors from two different manufacturers showed that, although the cross section was lower than for processors with bulk/epitaxial substrates, the linear energy transfer ( $LET_{th}$ ) threshold was very nearly the same [12,14].

Also, we extend focus of this guideline to highly scaled high speed advanced CMOS processors such as Intel Pentium and AMD K7. The Intel Pentium and AMDK7 have been tested extensively for total ionizing dose and single-event effects [11]. These processors have been found to be extremely tolerant to total ionizing dose and no radiation induced latchups have been observed with protons or heavy ions to an LET of approximately 15 MeV-cm<sup>2</sup>/mg. However, for Intel Pentium III, if running with the caches disabled is an option and with mitigation in place, these events may be controllable to allow for operation in the space environment.

## **II.C Performance and Processing Evolution**

Microprocessors have changed radically during the last 20 years. The earliest devices used 4-bits, with very primitive capability, but quickly evolved to 8 bits. Table 1 summarizes the properties of several types of microprocessors starting with the early 8-bit devices [3-9, 12, 14-15, 17-21]. The key points are the drastic reduction in feature size and the development of SOI processors during the last five years. Although not shown in the table, the number of register bits is still relatively small. However, new microprocessors contain large amounts of internal cache memory, increasing the total cross section for upsets if the cache is used.

Until recently most processor development concentrated on increasing clock frequency and adding architectural improvements such as advanced pipelining, out-of-order instruction sequencing, and increasing the size of on-board cache to increase throughput. At the present time there are several distinct branches in processor development because of the extremely high power dissipation that occurs in microprocessors that are intended for maximum clock frequency and throughput. That branch, driven heavily by performance, is intended for server applications where the high power dissipation can be accounted for in overall system design, such devices are nearly impossible to use in space because of the extreme difficulty of cooling. A second branch of microprocessor design is intended for mainstream desktop computer applications. Those devices can also dissipate relatively large amounts of power, as much as 100 W. Although it is conceivable that such devices could be used in space, the high power dissipation is a major drawback. The third branch of microprocessor design decreases power dissipation to develop intermediate performance levels with power dissipation below 20 W.

These distinctions are important because (1) high-performance processors use complex packages with massive heat sinks that make it very difficult to perform radiation tests; and (2) the predictions of the Semiconductor Industry Roadmap are very different for high-performance, desktop, and reduced power microprocessors, which can lead to erroneous conclusions about the performance and features of microprocessors.

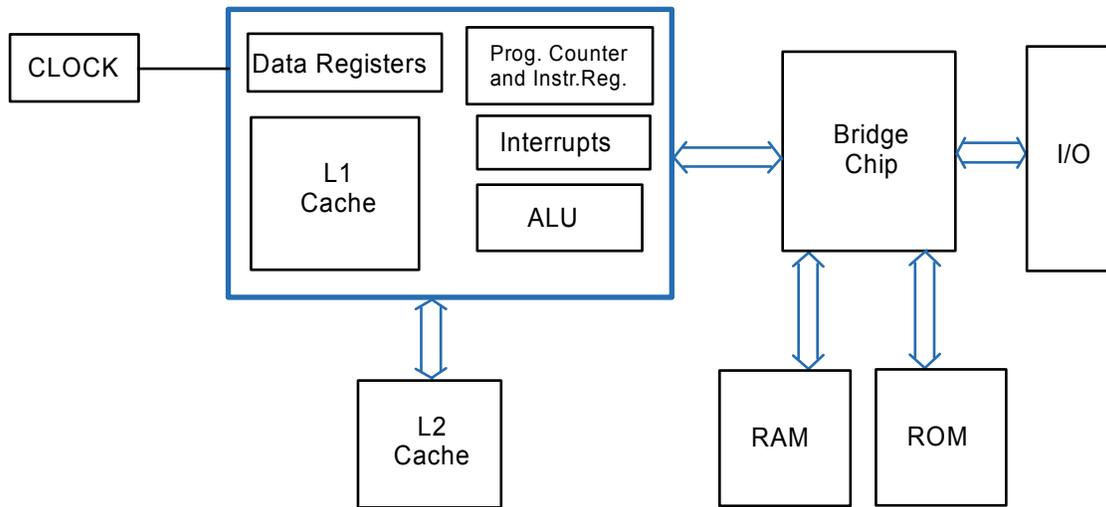
**Table 1. Comparison of several types of microprocessors.**

<b>Device</b>	<b>Manuf.</b>	<b>Year</b>	<b>Feature Size (<math>\mu\text{m}</math>)</b>	<b>Core Voltage (V)</b>	<b>Comments</b>
Z-80	Zilog	1986	3.0	5.0	8-bit NMOS
8086	Intel	1986	1.5	5.0	16-bit
80386	Intel	1991	0.8		16-bit
68020	MOT	1992	1.2		
LS64811	LSI	1993	1.2		
80386	Intel	1996	0.6		
80387	Intel	1996	0.6		
H30466A-21	SEI	1996	0.6		
PC603E	MOT	1997	0.5		
Pentium	Intel	1997	0.35		
PC750	MOT/IBM	2000	0.29	2.4	
Pentium	Intel	2002			
PC7455	MOT	2002	0.18	1.6	SOI process
IBM750FX	IBM	2002	0.13	1.3	SOI process
PC7457	MOT	2003	0.13	1.3	SOI process
PC7448	MOT	2006	0.09	1.1	SOI process

## **II.D Configuration Requirements**

Microprocessors are not stand-alone devices. An extensive amount of supporting electronics is required in order to place a microprocessor in a working configuration. Fig. 1 shows a typical block diagram of a contemporary microprocessor. In this example the L1 cache is contained on-chip, with a direct chip interface to external cache (L2). (In the most recent SOI, PowerPCs L2 cache is on chip.) Such processors typically contain 350 to 450 pins. The processor is designed to interface with a special bridge chip. Random access and non-volatile memory interfaces are done through the bridge chip, along with various input/output functions. A 32- or 64-bit interface is needed between the bridge chip and processor.

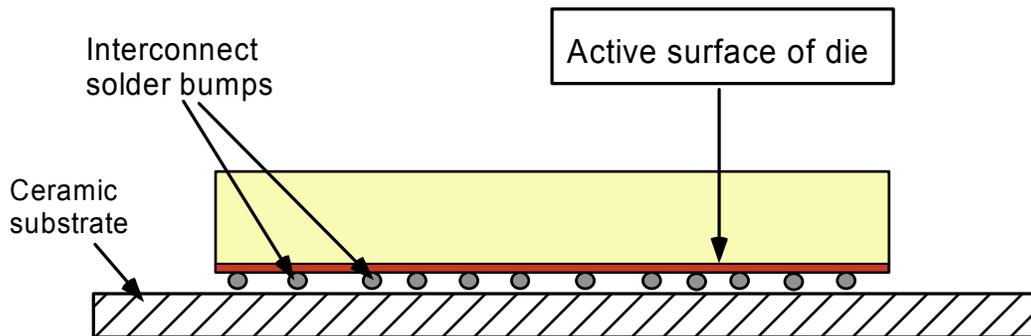
Designing a board to allow the processor to operate is difficult, particularly for processors with clock frequencies above 100 MHz. The interface logic levels have been reduced from 5 V for older processors to 1.1 V for more advanced processors. Terminated connections or differential line driver/line receiver pairs must be used at all interfaces. Errors or oversights in board design can lead to sporadic operation that will interfere with radiation tests. In most cases the development boards that are available from mainstream microprocessor manufacturers have been carefully designed and checked out for operation under worst-case conditions.



**Fig. 1. Block diagram of the operational blocks required for a modern microprocessor.**

## **II.E Packaging**

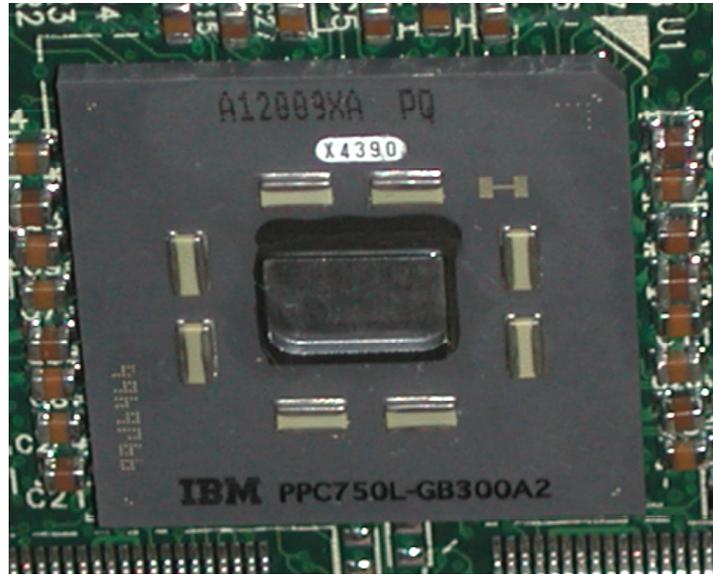
Although packaging is usually considered to be of secondary importance for radiation testing, the specific package type used for microprocessors has a large impact on radiation testing because of the difficulty of transporting heavy ions through the package. Modern microprocessors typically use “inverted” packaging with a ball-grid array. A diagram of such an inverted package is shown in Fig. 2. Contacts on the active surface of the die are made with a ceramic substrate. Pins (or direct connection to a circuit board) are attached to the ceramic substrate; they are not shown on the diagram. Because of this inverted structure and the large number of pins, it is not practical to remove the die from this inverted configuration and repackage it so that the active surface is at the top. Consequently, for radiation testing with heavy ions, it is necessary to maintain the inverted configuration, irradiating the device through the back of the package. The ion used for testing must have sufficient range to pass through the surface of the die, or the die thickness must be reduced. Typical die thicknesses are approximately 750-900  $\mu\text{m}$ . Relatively few ions are available with a range of this magnitude, severely limiting heavy-ion tests. Ion range will be discussed in more detail in a later section.



**Fig. 2. Diagram of the inverted package structure typically used for high-performance microprocessors.**

Various mechanical methods can be used to reduce the thickness of the back of a microprocessor die, allowing particles with less range to be used for testing. One method uses a high-speed diamond abrasive tool. Fig. 3 shows an example where this was done to reduce the die thickness to approximately 200  $\mu\text{m}$ .

It should be noted that, as a consequence of back thinning, the thermal issue becomes more severe, particularly during radiation testing. Heat removal techniques should be applied. There might be some concerns that if the die is too thin, it might affect the charge collection and consequently influence the outcome of the radiation testing.



**Fig. 3. An example of an advanced microprocessor with an inverted package where the back of the die has been mechanically thinned, leaving approximately 25% of the original die thickness.**

## **II.F Thermal Issues**

The processors and the other components on the test board dissipate considerable amounts of heat. These devices can dissipate relatively large amounts of power, as much as 100 W. Although it is conceivable that such devices could be used in space, the high power dissipation is a major drawback. Commercial processors usually are packaged with an external heat sink on the top for heat removal. High-performance processors use complex packages with massive heat sinks that make it very difficult to perform radiation tests. Particularly, heat is a major problem when the testing is done in a vacuum and processors tend to overheat. During the radiation testing, it is necessary to modify the original heat sink to allow for beam access or replace it with a custom made heat sink. The radiation data should be collected by allowing time for the processor to cool between successive irradiations when needed. Also, to prevent over heating, the radiation runs should be kept short. A thermocouple can be used to measure the temperature. For the newer processors, a routine can be developed to read out the processor's junction temperature.

### III. Radiation Induced Effects in Microprocessors

#### III.A Introduction to Basic Radiation Effects

Photons, electrons, protons, and heavy ions are all able to produce ionization when they travel through matter. The total energy loss of an ionizing particle as it travels through matter is called the linear energy transfer (LET). The LET is the total energy loss per unit distance of travel and is usually normalized by dividing by the density of the medium so that the units are MeV-cm<sup>2</sup>/mg. The reason for this normalization is that it makes LET for a given particle and energy more nearly the same in different materials (still not exactly the same, but more nearly the same).

A single-event effect (SEE) occurs when a single energetic particle is capable of creating an observable effect in a device. One category of SEE involves charge collection following the liberation of mobile electron-hole pairs by an energetic particle in a semiconductor. This category can be further divided into direct ionization, indirect ionization, or a combination of both. Direct ionization (always the dominant process for heavy ions) occurs when the incident particle creates electron-hole pairs. Indirect ionization occurs when the incident particle (usually a proton or neutron) produces an energetic recoil particle, a fragment of (or the entire) the nucleus from a target atom and the latter particle creates electron-hole pairs.

Device immunity is determined by its linear energy transfer threshold (LET<sub>th</sub>). The LET<sub>th</sub> is defined as the minimum LET to cause a single-event effect at a particle fluence of 10<sup>7</sup> ions/cm<sup>2</sup> per ASTM. Low LET<sub>th</sub> implies proton sensitivity. The LET<sub>th</sub> usually reduces as a device accumulates large TID.

Device SEE susceptibility from a specified type of particle is usually described in terms of a cross section. The device cross section for the specified particle type is defined by quotient of the errors observed and the fluence required to induce these errors. This definition is solely empirical; it is not the geometrical or physical cross section of the device. For heavy-ion induced SEE, the particle type is specified by LET, and the cross section is a function of LET.

The most familiar example in this category is single-event upset (SEU). SEU is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." SEUs are transient soft errors, and are non-destructive. A reset or rewriting of the device results in normal device behavior thereafter. An SEU may occur in analog, digital, or optical components or may have effects in surrounding interface circuitry. SEUs typically appear as transient pulses in logic or support circuitry or as bit flips in memory cells or registers. Also possible is a multiple-bit SEU in which a single ion induces SEUs in two or more bits simultaneously. Multiple-bit SEU is a problem for single-bit error detection and correction (EDAC) where it is impossible to assign bits within a word to different chips (e.g., a problem for DRAMs and certain SRAMs). A severe SEU is the single-event functional interrupt (SEFI) in which an SEU in the device's control circuitry places the device into a test mode, halt, or undefined state. The SEFI halts normal operations and requires a power reset to recover. A SEFI may also be due to a SEU in the shift register that controls the address of the control logic, and the result is a misread of all information in the device.

The present trends (e.g., scaling device size and power reduction, line resolution increase, increased memory and speed) will only heighten the SEU susceptibility. This is easily seen when one considers the device as a simple capacitor (C) in which the ionized particle deposits sufficient charge (Q) to result in a voltage (i.e., logic state) change. SEU occurs when LET is sufficient to deposit  $Q > Q_{crit}$

Since the  $LET_{th}$  is equivalent to the LET required to produce a voltage change ( $\Delta V$ ) sufficient for an SEU, then mathematically:

$$LET_{th} \propto \Delta V = Q/C$$

As the size of these active devices decreases, the capacitance will decrease and so, correspondingly, the charge necessary to induce the SEU. The depth of the devices has been generally unchanged; it is the length and width of these devices that have been reduced. If we consider a square device of feature size,  $L \times L$ , the critical charge for state change is proportional to the feature size squared ( $Q_{crit} \propto L^2$ ). Robinson et al. [25] present the measured critical charge for a number of IC technologies (including NMOS, CMOS/bulk CMOS/SOS, i2L, GaAs, ECL, CMOS/SOI, and VHSIC bipolar) as being:

$$Q_{crit} = (0.023 \text{ pC}/\mu\text{m}^2) L^2$$

This critical charge is that charge necessary to flip a binary "1" to a "0" or vice versa but is less than the total stored charge. Specifically,  $Q_{crit}$  is then the difference between the storage node charge and the minimum charge required for the sensing amplifier to read correctly. In SRAM circuits,  $Q_{crit}$  depends not just on the charge collected but also the temporal shape of the current pulse.

Single-event latchup (SEL) is a condition that causes loss of device functionality due to a single-event induced current state. Kolasinski et al. [26] first observed SEL in 1979 during ground testing. SELs are hard errors, and are potentially destructive (i.e., may cause permanent damage). The SEL results in a high current, which may or may not exceed device specifications but, regardless, can damage the device due to local joule heating. The latched condition can destroy the device, drag down the bus voltage, or damage the power supply. Originally, the concern was latchup caused by heavy ions; however, latchup can be caused by protons in very sensitive devices. An SEL is cleared by a power off-on reset or power strobing of the device. If power is not removed quickly, catastrophic failure may occur due to excessive heating or metallization or bond wire failure. SEL is strongly temperature dependent: the threshold for latchup decreases at high temperature, and the cross section increases as well.

Single-event burnout (SEB) is a condition that can cause device destruction due to a high current state in a power transistor. SEB causes the device to fail permanently. SEBs include burnout of power MOSFETs, and frozen bits. SEB of power MOSFETs was first reported by Waskiewicz et al. in 1986 [27]. Only SEB of n-channel power MOSFETs has been reported. An SEB can be triggered in a power MOSFET biased in the OFF state (i.e., blocking a high drain-source voltage) when a heavy ion passing through deposits enough charge to turn the device on. SEB susceptibility has been shown to decrease with increasing temperature. SEB can also occur in bipolar junction transistors (BJTs) as was first reported by Titus et al. in 1991 [29].

Single-event gate rupture (SEGR). A power MOSFET may undergo SEGR, which is the formation of a conducting path (i.e., localized dielectric breakdown) in the gate oxide resulting in a destructive burnout. Fischer was the first to report on SEGR of power MOSFETs in 1987 [28]. Swift et al. [30] and Irom et al., [31] have described a new hard error, that of single-event dielectric ruptures (SEDR). SEDR (also referred to as micro-damage) occurs in CMOS and is similar to SEGR observed in power MOSFETs. SEGR phenomena have been seen in gate oxides in ICs.

## III.B Early Test Approaches for Microprocessors

Microprocessor radiation testing was first done more than 20 years ago. The 8-bit devices that were available at that time were very elementary compared to the complex devices that are now available, with very simplified instructions and interface requirements. Because of the simplicity of older processors, it was possible to develop machine language instructions for radiation testing using fully custom hardware. Early microprocessors had 48 to 64 pins, compared to more than 400 for modern microprocessors, and did not contain on-board cache. Five basic approaches were used in the earlier studies [19]:

- 1) **Self Testing, Single Computer Method**  
A microprocessor can be tested in a simple computer configuration, e.g., single board computer. The processor “self-tests” and the result of the self-test can be visually recognized either by a CRT displayed output pattern or even by a simple LED output.
- 2) **Controller Assisted, Single Computer Method**  
An external controller interrogates the operation of the microprocessor under test by comparing its outputs with the “true” values stored in an external memory table.
- 3) **Controller Assisted, Golden Chip Method**  
An external controller compares the outputs of the microprocessor under test with the outputs of a “standard” microprocessor (golden chip) operating under the same program. In the above three methods the microprocessor under test automatically fetches the instructions stored in memory (RAM or ROM) whenever it requires them.
- 4) **Controller Dominated, Single Computer Method**  
It is possible for the controller to “take over” the function of simple computer memory by introducing instructions whenever the microprocessor under test requires them. Here the instructions are “force-fed,” and the microprocessor under test effectively single-steps through the given program sequentially. The same controller interrogates the outputs of each step.
- 5) **Controller Dominated, Golden Chip Method**  
This is another single-step method. The interrogation of upsets consists of comparing the outputs of the microprocessor under test and those of a “standard” microprocessor (golden chip) operating under the same program. The controller stores the error data.

In all methods, except for the first one, the speed of the operation is limited by that of the controller during the handshake. The controller is usually a micro- or mini-computer, which requires tens of microseconds to collect and store data. Therefore, the clock frequency of the microprocessor under test must be interrupted while the controller collects upset data. A concept of “average clock frequency” is introduced to specify the average clock rate during the test period. A comparison (pros and cons) of the five test methods is made in Table 2.

**Table 2. Comparison of five approaches used in older radiation tests of microprocessors.**

<b>Test Methods</b>	<b>Self Testing Single Computer</b>	<b>Controller Assisted</b>		<b>Controller Dominated</b>	
<b>Trade Off Criteria</b>		<b>Single Computer</b>	<b>“Golden Chip”</b>	<b>Single Computer</b>	<b>“Golden Chip”</b>
Effective Clock Frequency	High	Medium	Medium	Low (< 10 KHz)	Low (< 10 KHz)
Individual Element Test Ability	Low	High	High	High	High
Error Table Structure/Data Display	Simple	Complex	Complex	Complex	Complex
Test Preparation Lead Time	Short	Medium	Medium	Medium	Long
Devices Tested	1802 SA3000	1802, 6800 80C86 8X300 M02815 8X305 SA3000	9900 9999 F9445	2901	Z80 NSC800

In principle these approaches could also be used for modern processors. However, the extremely complex interface requirements and the difficulty of designing an operational system exact a very high price for custom hardware development, making the first approach impractical. Although the Golden Chip approach can still be used, it is difficult to operate high-frequency processors in lockstep. Thus, most tests of complex microprocessors use the development board approach.

## III.C Test Approaches for High-Performance Microprocessors

### III.C.1 Operating Systems

The response of a microprocessor to radiation depends on software as well as hardware. Although it is possible to operate a processor with dedicated machine-language instructions and avoid the need for an operating system, this is generally impractical for the complex processors that are used today, partly because of the need for a bridge chip (or emulated equivalent) to perform most of the I/O and memory interface functions.

Minimizing processor activity during irradiation essentially reduces the number of internal operations, thereby making the operation susceptible to errors in only a few internal locations. For example in radiation testing of PowerPC microprocessors performed by the Jet Propulsion Laboratory (JPL) group, the processor was programmed to perform a one-word instruction in a small infinite loop and wrote a register snapshot to a strip chart in the physical memory every half second. After the irradiation ended, an external interrupt triggers a program to count state changes in internal registers or the data cache. This method is referred to as “do nothing with strip chart.”

Nearly all microprocessor testing is done with some form of operating system. Development boards typically contain very basic operating systems. In some of their early testing, A. K. Moran and K. A. LaBel [2, 9] performed SEE tests on the 80386, 80486, 80387, and 82380 using a single-board computer. The device was exercised using a software routine which performs addressing, memory reads and writes, and other operations. External clock speed was 16 MHz. Failure of the device to write to a test address, incorrect data, or device lock-up was counted as an SEU. If lockup occurred, the test run was halted, and a reset was issued to the device. The SEE data for 80386 is presented in Fig. 4. It is also possible to use more sophisticated operating systems. For example, Hiemstra and Baril conducted proton tests of Pentium processors using a board with the Windows NT operating system [10]. That choice was made because Windows NT was to be used in the manned missions that incorporated the processor. During those tests, malfunctions in the operating system frequently occurred and actually interfered with attempts to examine register upsets, resulting in the “blue screen” that indicates an operating system crash. The hang rate was so high that it was not possible to determine the error rate for registers in those tests. Fig. 5 shows the cross section observed for “hangs” during the tests by Hiemstra and Baril (“hangs” disrupt operation, typically requiring a cold re-boot to restore operation). The “hang” rate for proton tests done with a more primitive operating system for the PowerPC processor are 3-4 orders of magnitude lower than for the tests done with Windows NT. These results provide dramatic evidence of the importance of the operating system on single-event upset testing [10]. If a complex operating system is used, it will heavily influence the results and may interfere with attempts to characterize the basic response of the processor. Thus, very primitive operating systems are preferred for microprocessor testing; however, note that tests with complex operating systems may be the preferred approach if they are actually used in the application.

The significance of hangs and crashes will be discussed in more detail later. Note that while some of these events may be caused by failures in the operating system, others may occur because a critical part of the processor (such as the instruction register) was affected.

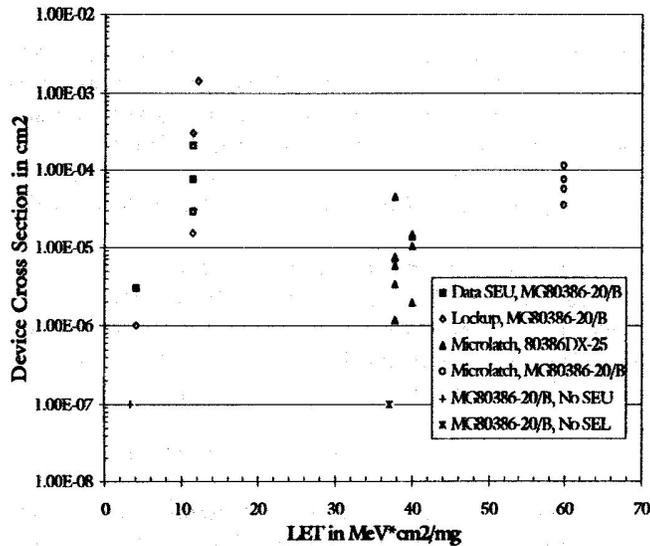


Fig. 4. Cross-section for SEE during heavy ion testing of Intel MQ80386 microprocessor. The SEU threshold LET for count, reset mode is 4-5 MeV-cm<sup>2</sup>/mg. The SEU threshold LET for lockup mode is 6-11.4 MeV-cm<sup>2</sup>/mg. The latchup LET threshold is 30-32 MeV-cm<sup>2</sup>/mg [9].

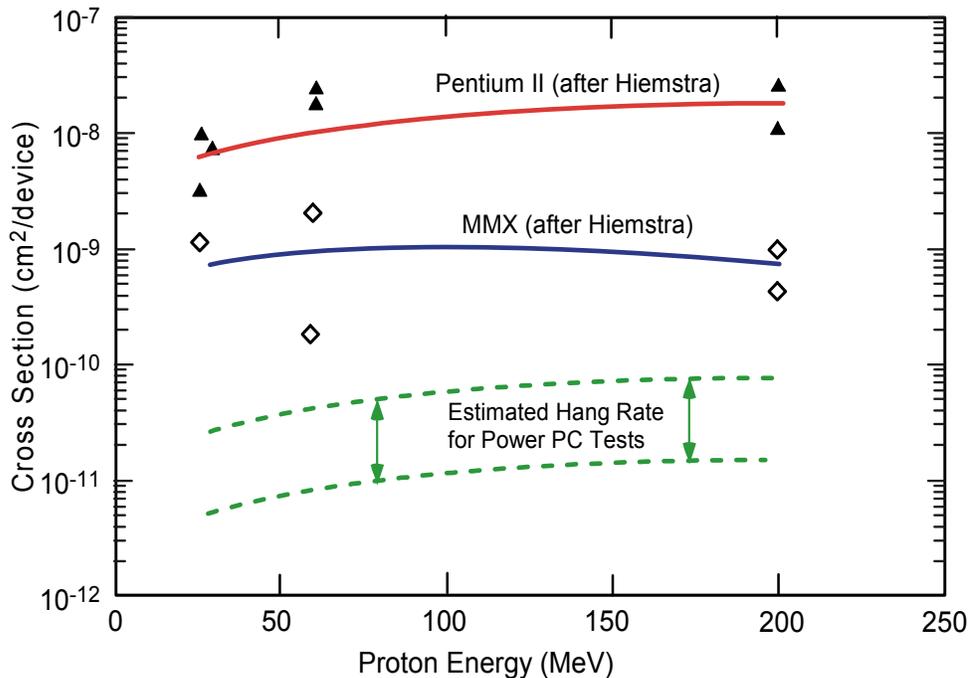


Fig. 5. Cross-section for “hangs” during proton tests of two different types of processors. The large difference in the cross section is almost certainly due to the complex Window NT operating system used for tests of the Intel processors [10]. The PowerPC tests used a very primitive operating system provided with a development board which was far less sensitive to processor errors.

Other methods have been implemented to test high performance microprocessors. For example, the NASA GSFC group used two computer systems in their test setup to perform SEE testing on Intel Pentium III (P3) and the AMD K7 microprocessors. The first computer system contained the Device Under Test (DUT). The second computer system was a Peripheral Component Interconnect (PCI)

Extension for Instrumentation (PXI)-based computer that was used to control the testing. The DUT computer operating the DUT microprocessor was entirely COTS-based. The DUT, a commercial microprocessor (Intel Pentium III or AMD K7) modified for beam access and heat removal, resides on a motherboard designed for a desktop system. The PXI-based Test Controller consisted of a PXI chassis. Within the PXI chassis resides an embedded Pentium III based controller (running Win98, Labview™ application). The DUT software was executed using the Pharlap Real-Time operating system (RTOS), with preemptive task switching turned off [11].

The Innovative Concepts, Inc., used a motherboard provided by Gespac, Inc., to test Motorola PowerPC PC603E. The Gespac board operated the target devices using the VXWorks operating system. During all exposures, a compact script was run at speed in the PC603, which performed a series of block memory transfers, and comparisons as well as I/O to the system bus. The on-chip data and instruction caches were enabled for all exposures.

The French collaboration CNES/PATRIA [7] used “Test sous Ions Lourds de MICROprocesseurs” TILMICRO test equipment to test PowerPC PC603 (A, E, P, and R) series from Motorola and ATMEL. This test system has already been used for other microprocessors such as PIC16C76 from MICROCHIP, 80c31 from ATMEL, DX4 from Intel, and ADSP21020 from Analog Devices. The test system has a basic operating system and allowed the test program to run at 25 MHz under the radiation testing while controlling whole components.

The NASA JPL group used commercial evaluation boards to test the commercial PowerPCs. They used Motorola’s PowerPC evaluation boards known as “Yellowknife” and “Sandpoint.” These commercial boards were chosen because they eliminate the large engineering effort required to design a custom test board for the microprocessor and also provide a very basic internal operating system that eliminates the many layers of code in more advanced operating systems. This provides far better timing, diagnostic information, and control of processor information flow. These boards came with a simple monitor/debugger that Motorola has dubbed “DINK.” DINK communicates over a bidirectional serial port to a computer terminal. The other external communication provided on these boards is a JTAG port (JTAG is an industry standard, boundary scan interface) [12, 14].

## **III.C.2 Test Methods**

A number of assembly language software programs need to be written to detect errors in various sections of the processor. It is possible to design software that primarily exercises specific registers, cache, or regions and, thus, allows the number of errors to be determined for various registers, cache, or specific operating modes.

### **III.C.2.1 Register-Level Tests**

As discussed earlier, tests of first- and second-generation microprocessors showed that nearly all of the responses to heavy ions were directly related to state changes in registers. Nearly the same results occurred for tests that used a broad range of instructions compared to those with more restricted instruction sets, when the results were examined in the context of errors in internal registers. The transparent operation of 8-bit microprocessors provided direct visibility of the program counter as well as interrupts, facilitating the interpretation of test results. This led to the development of register-level test software [9, 19].

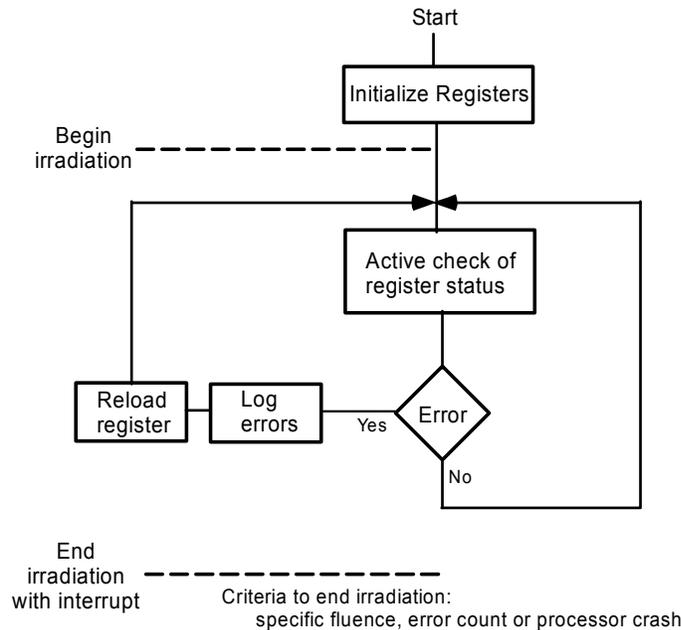
Newer processors use more internal registers than older processors. The cross section of some types of registers may be different because of differences in the device geometry. Consequently, it is necessary to refine the register-level test approach to evaluate the response of different types of internal registers (i.e., general-purpose registers, tags, and flags). An added complication for newer

processors is asymmetry in the sensitivity, resulting in a much larger cross section for upsets in a specific direction (i.e., 1 to 0) [12,16], compared to upsets that cause the opposite transition to occur. In order to deal with the asymmetry problem, the register test must be repeated with different internal register patterns that deliberately test upset symmetry.

There are two methods of testing the registers: semi-static and semi-dynamic. In the following, we explain both methods.

### III.C.2.1.A Semi-Static

In this test method, the program counter and instruction register are continuously exercised while the registers are static. Hence, this test method is called “semi-static.” This typically consists of a compact program that initially loads specific values into a large number of registers and continually examines the status of the registers during the time that the device is irradiated. The register status test usually takes very little time to execute, and is run periodically at intervals from 1–200 milliseconds, providing a nearly continuous evaluation of register status. A flow chart showing this approach is shown in Fig. 6. If an error is detected during the sequence, the contents of the register and the register status are logged, along with the elapsed time during the irradiation when the error occurred. The error is corrected, and the active register test loop continues until the test is stopped. Reasons for stopping the test include (a) reaching a set (pre-planned) fluence; (b) detecting an appropriate number of error counts; and (c) abnormal results, including a “crash” or “hang” that stops the dedicated register test program sequence. Note that this test method assumes that the processor works properly nearly all of the time during the test. It will not work effectively unless the error rate is relatively low and dominated by register errors. The results of this type of test can be reported either in upsets-per-bit (the preferred approach), or upsets-per-chip.



**Fig. 6. Flow chart showing register-level test software. The test program runs continually during the irradiation, providing nearly continuous visibility of the status of internal registers.**

### **III.C.2.1.B      *Semi-Dynamic***

Another program sequence to test the microprocessor registers involves writing a pattern on the x-register and transferring the contents of the x-register to the Special Register (SP), then back to the x-register, etc., for a given time, in order to observe the bit error. The microprocessor is programmed to perform the transfer task only during exposure to beam. Also, the Arithmetic Logical Unit (ALU) can be placed in the program loop to test the vulnerability of the ALU section.

The following method was adapted by the NASA JPL group to test the registers in the Motorola PowerPC microprocessors [17]. In this method the loop performed the following steps for testing of General Purpose Registers (GPRs) in the Motorola PowerPC:

1. Load a GPR with the operand 0x55555555 (multiplicand).
2. Load the next GPR with operand 0x2 (multiplier).
3. Multiply the registers together and write the result into the first register.
4. Increment the register pointer (now the second becomes the multiplicand and a third GPR is the multiplier) and repeat steps 1 to 3 until all the GPRs hold multiplication results.
5. Read the entire GPR and check that the result agrees with expected value of 0xaaaaaaaa.
6. If not, then log the result to external memory as a strip chart (to be utilized in off-line analysis).

This test has three possible outcomes:

1. The test passes and no upset is recorded.
2. The results do not match the expected value, but only one or two bits are wrong so this is counted as a register upset.
3. The result does not match the expected value, but many bits are erroneous, which is counted as a processing unit upset because it occurred, for example, in the Arithmetic Logical Unit (ALU) or in the register addressing logic.

In this method, the registers are continuously being read and written, and the ALUs are kept busy.

The NASA GSFC group adapted the following test method to test the Pentium III registers:

Fill sets five CPU registers (ebx, ecx, edx, ebp, and edi) to an initial value of 0xAAAAAAAA then continuously check to see if any of the register values change. If any values change, an error is reported and an attempt is made to reset the register to its baseline value. The register is read again to form a new baseline value. The error report includes the register that changed, the value it changed to, the baseline before the error and the baseline after the error. The test then continues. At each keep alive the baselines are reset to 0xAAAAAAAA.

### **III.C.2.2      **Tests of Internal Cache****

Modern processors dedicate a significant part of the chip area to on-board cache memory. Cache memory cells are designed somewhat differently than register cells, typically using more compact geometry. Nearly all processors use 6-T memory cells for cache, although some papers have discussed the possibility of using other technologies, including DRAMs because of the much smaller cell size.

Cache memory needs to be evaluated separately using dedicated software that is specifically designed to evaluate cache. Some processors are designed to allow internal error correction of the cache memory. This provides an additional degree of freedom for radiation testing. In principle, cache tests can be done in the same way as register tests. Typically the number of bits in the cache is much larger than the total number of register bits, providing better counting statistics during an SEU test run because the number of errors is larger. The cross section of the cache bits is typically smaller than that of the registers. Cache bits may also exhibit asymmetric sensitivity to stored 1's and 0's.

In newer processors a more complex method is required to examine errors in the cache. Upsets in the cache are counted with special post beam software. The cache is initialized under specified conditions prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from the contents of the cache, is placed in the external memory space covered by the cache. Comparing the cache contents after irradiation provides verification of the cache contents. Tag upsets, as well as upsets of the data valid flag, can be detected by monitoring the distinctly different pattern. The tag and data valid upsets are thus distinguished and counted separately from upsets of the data bits themselves.

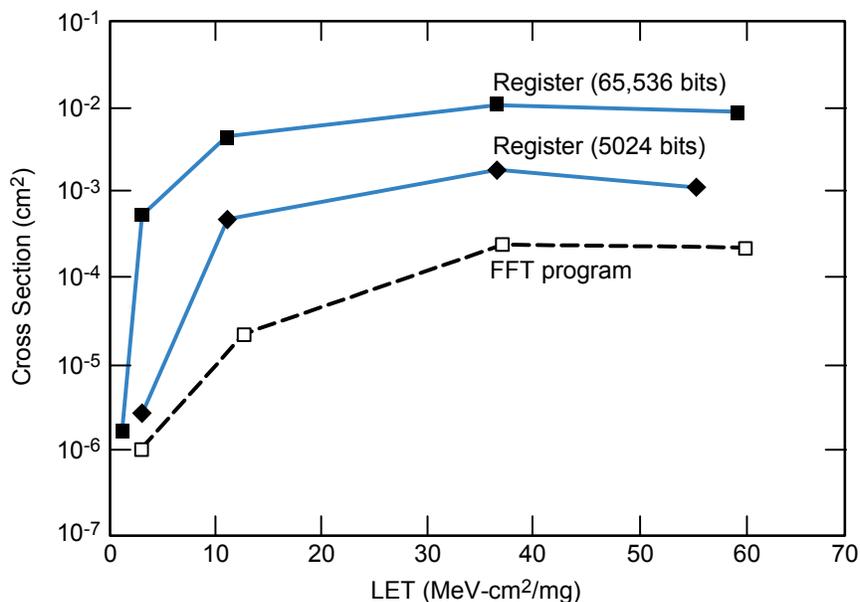
For example, in radiation testing of PowerPC microprocessors, the adopted method for measuring of cache SEUs utilized the upper fourth (8 K byte) of the cache. The cache is filled with a known pattern prior to irradiation. In a small loop, the processor continuously writes a snapshot of the cache to a strip chart in the physical memory. After irradiation, an external interrupt triggers a program to compare the cache contents with the pattern initially loaded and counts state changes in the cache [12, 16-17, 20-22]. In this method, one heavily exercises the data cache, which is likely to make the largest contribution to upset rates for most real applications.

### **III.C.2.3 Operational Software Tests**

Tests of specific software applications can also be done, although the interpretation of such results is less straightforward compared to register tests. Results of operational software can often only be measured using a "go/no-go" criterion, stopping the test whenever the output of the program differs from the expected result. In such cases a series of runs are made, stopping the beam after an error is detected. The processor program is reloaded after each test, restarting the test until another error occurs. The results can only be reported as a total cross section, not a per-bit cross section as for register or cache tests, and require a sequence of test runs.

Fig. 7 compares tests of the PowerPC 603E for registers, cache (the larger number of bits), and a fast-Fourier transform program [7]. The results are all reported as total chip cross section. The cross section for cache and registers scales with the number of bits. The cross section for the FFT program is much lower, which is the typical result when tests are done with operational software. The reasons for this are related to register usage and visibility. First, even a complex program may use only some of the internal registers and, second, many of the errors that occur in registers will only affect the results if they appear between the time that the register is loaded with information used for the calculation and the time that the step using that information is completed. The latter factor reduces the "visibility" of register errors by factors that are typically between 10 and 100.

The results in Fig. 7 show some key points that affect not only microprocessor testing, but also the way that test results are interpreted in the context of upsets or malfunctions in real applications. In principle it is possible to calculate the upset rate of a specific application program from the more fundamental results from register and related tests, but such calculations require a thorough knowledge of the processor design and architecture.



**Fig.7. Comparison of the total chip cross section for cache (64Kbits), general purpose registers (5024 bits), and a fast-Fourier transform program The processor was the Motorola PC603E [7].**

### III.C.2.4 Program Hangs

During certain SEE tests, the processor can become non-functional—program “hangs” or Single Event Functional Interrupts (SEFIs)—and these types of errors are of extreme concern in applications because they may require complex procedures to restore normal operation. In most cases it is not possible to determine the underlying cause of these malfunctions because there are many possible ways in which processor operation can be disrupted. However, the relative occurrence of “hangs” should be measured and compared to the upset rate obtained for internal registers or other functions of the processor in the space environment.

Although “hangs” occurred relatively infrequently in older processors, they occur far more frequently in modern processors that have complex internal architectures. In nearly all cases, recovery from a “hang” condition cannot be done by applying a reset pulse, but instead requires removal of power and cold restart. Consequently, “hangs” are extremely important for modern microprocessors in the space environment.

The “hang” cross section for Intel and PowerPC processors was shown earlier in Fig. 5 for proton tests. In that example the much higher cross section for Intel processors was attributed to crashes in the operating system (Windows NT in that example). Fig. 8 shows specific “hang” cross section results that were obtained with a far more primitive operating system [22] for highly scaled SOI PowerPC microprocessors from Motorola with feature sizes ranging from 180-90 nm. Radiation testing of the Motorola SOI processor was done using a development board from Motorola known as “Sandpoint.” This board was chosen because it eliminated the large engineering effort that would be required to design a custom test board for the processor. It also provided a basic PROM-based system monitor instead of a complex operating system. This provides far better diagnostic information and control of processor information during SEU testing compared to more advanced operating systems. This board has a daughter card for the processor with no active components underneath, which is important for proton tests, where high energy protons could strike other components on the test board. This allowed us to shield other components on the board during proton tests, assuring that the measured response was entirely due to effects within the processor. The only external communication channels provided on these boards are a simple serial connection for a “dump” terminal and a JTAG port. An Agilent

Technology 5900B JTAG probe was used for these tests. This probe made it possible to interrogate the processor even after unexpected events occurred (such as operational errors during irradiation). Auxiliary tests (including JTAG) support the conclusion that the “hangs” are due to conditions in the processor, not failure of the operating system.

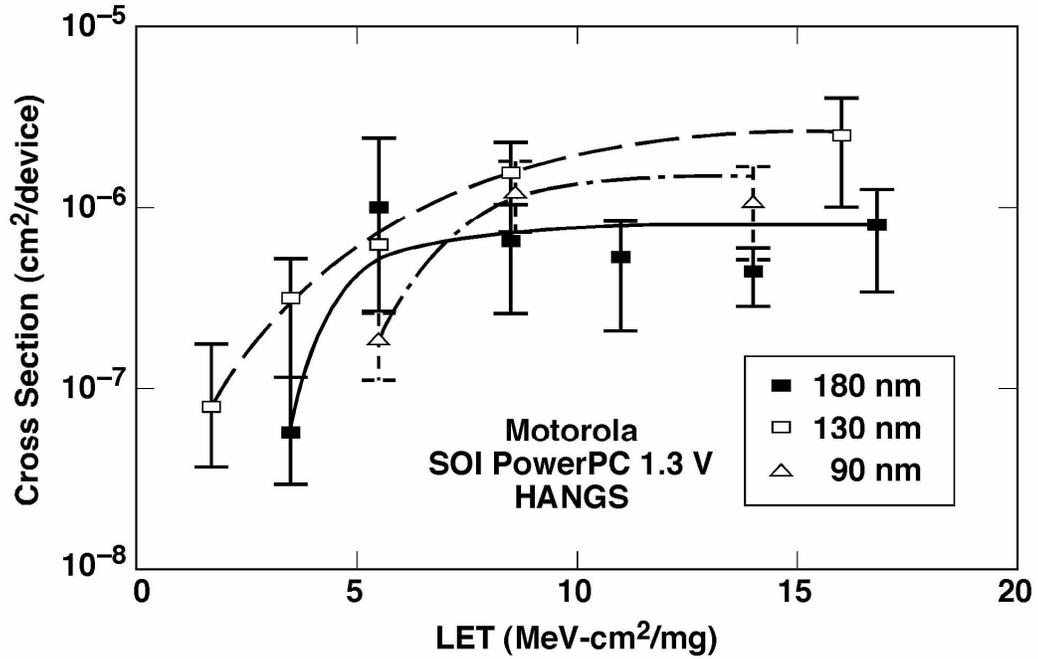


Fig. 8. “Hang” cross section for advanced versions of the PowerPC processor. [20].

## IV. Beam Requirements

### IV.A Heavy Ions Beams

The active region of high-performance processors is very thin, typically about 2–3  $\mu\text{m}$  or less. However, as discussed in Section 2, the inverted package used for microprocessors requires irradiation from the back of the package. The thickness of a typical microprocessor die is 700–900  $\mu\text{m}$ . In order to test such a device, the range of the ion beam must exceed the die thickness. Note that there is significant energy loss by such beams as they travel through such thick regions, requiring correction for energy loss. The LET varies rapidly with distance near the end of the range and, thus, it is necessary to know the die thickness to within about 2%. Ar, Ne, and Kr ions can be used on devices where the back of the substrate has been reduced by mechanical thinning.

#### IV.A.1 Heavy Ion Beams Available at Various Accelerators

The beams that are available for five commonly used accelerators are shown in Tables 3–9. Tables 3 and 4 show the range of high LET ions at Brookhaven National Laboratory (BNL) and UC Berkeley, respectively. Although ions with lower LET have somewhat greater range, the ions that are available from those facilities have such a limited range that it is nearly impossible to test processors using irradiation from the back of the die because the die would have to be reduced so much in thickness that it would affect the packaging and lead integrity of the “flip-chip” bonding.

**Table 3. Range of ions with LET < 30 MeV-cm<sup>2</sup>/mg at BNL.**

Ion	Energy (MeV)	LET at Normal Incidence (MeV-cm <sup>2</sup> /mg)	Range at Normal Incidence ( $\mu\text{m}$ )
Ne	800	1.2	1655
Ar	1598	3.8	1079
Kr	3117	14.2	622

**Table 4. Range of ions with LET > 30 MeV-cm<sup>2</sup>/mg at UC Berkeley.**

Ion	Energy (MeV)	LET at Normal Incidence (MeV-cm <sup>2</sup> /mg)	Range at Normal Incidence ( $\mu\text{m}$ )
Br	305	36.9	38.7
Ag	345	52.9	34.5
I	370	60.1	34.3
Au	390	84.1	29.1

The Texas A&M cyclotron produces ions with far greater range. Tables 5 and 6 show the energy and range of ions with energies of 25 MeV and 40 MeV per nucleon. The LET values are the LET at the surface. LET increases as the ion loses energy during its transition through the silicon. The LET must be corrected to account for that energy loss. Figs. 9 and 10 show how the LET changes with distance for the different ions with energies of 25 and 40-MeV per nucleon.

**Table 5. Range of 25 MeV per nucleon ions at Texas A&M.**

<b>Ion</b>	<b>Energy (MeV)</b>	<b>LET at Normal Incidence (MeV-cm<sup>2</sup>/mg)</b>	<b>Range at Normal Incidence (μm)</b>
Ne	545	1.7	790
Ar	991	5.4	485
Kr	2081	19.3	332
Xe	3197	37.9	286

**Table 6. Range of 40 MeV per nucleon ions at Texas A&M.**

<b>Ion</b>	<b>Energy (MeV)</b>	<b>LET at Normal Incidence (MeV-cm<sup>2</sup>/mg)</b>	<b>Range at Normal Incidence (μm)</b>
Ne	800	1.2	1655
Ar	1598	3.8	1079
Kr	3117	14.2	622

### 25 A MeV Beams

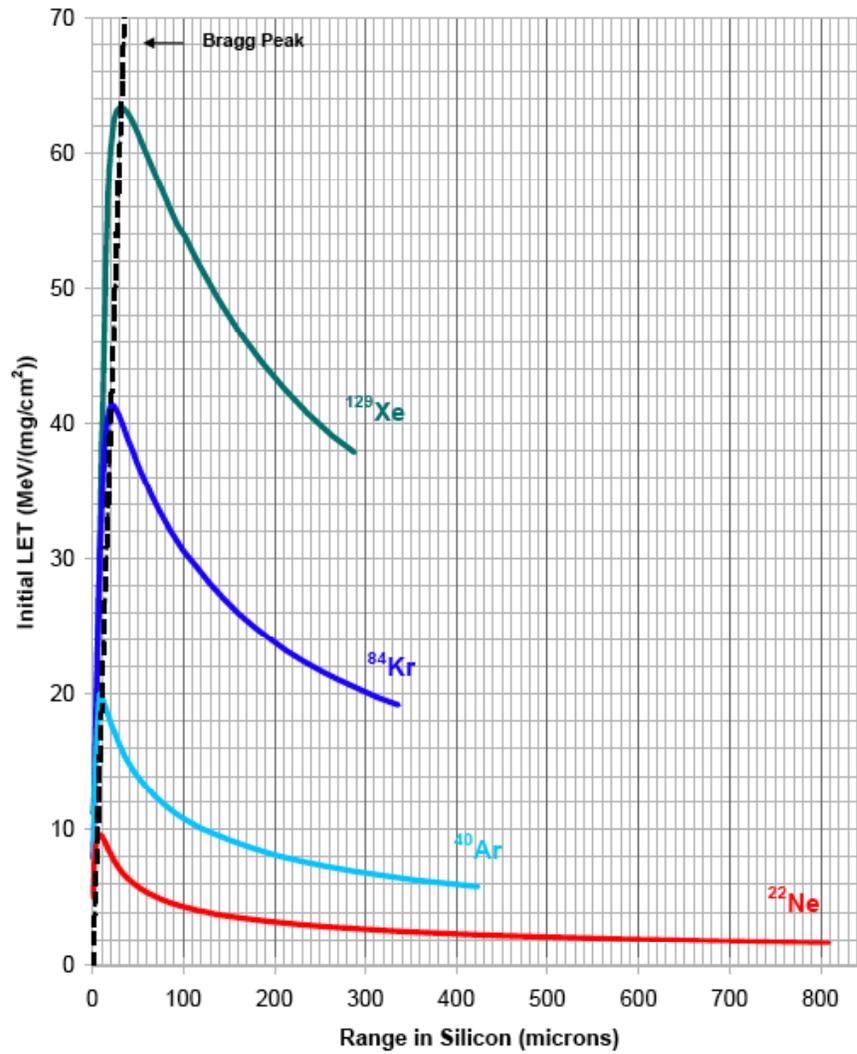


Fig. 9. Variation of 25 MeV per nucleon ions with distance in silicon.

### Initial LET vs. Range in Silicon for 40 A MeV Beams

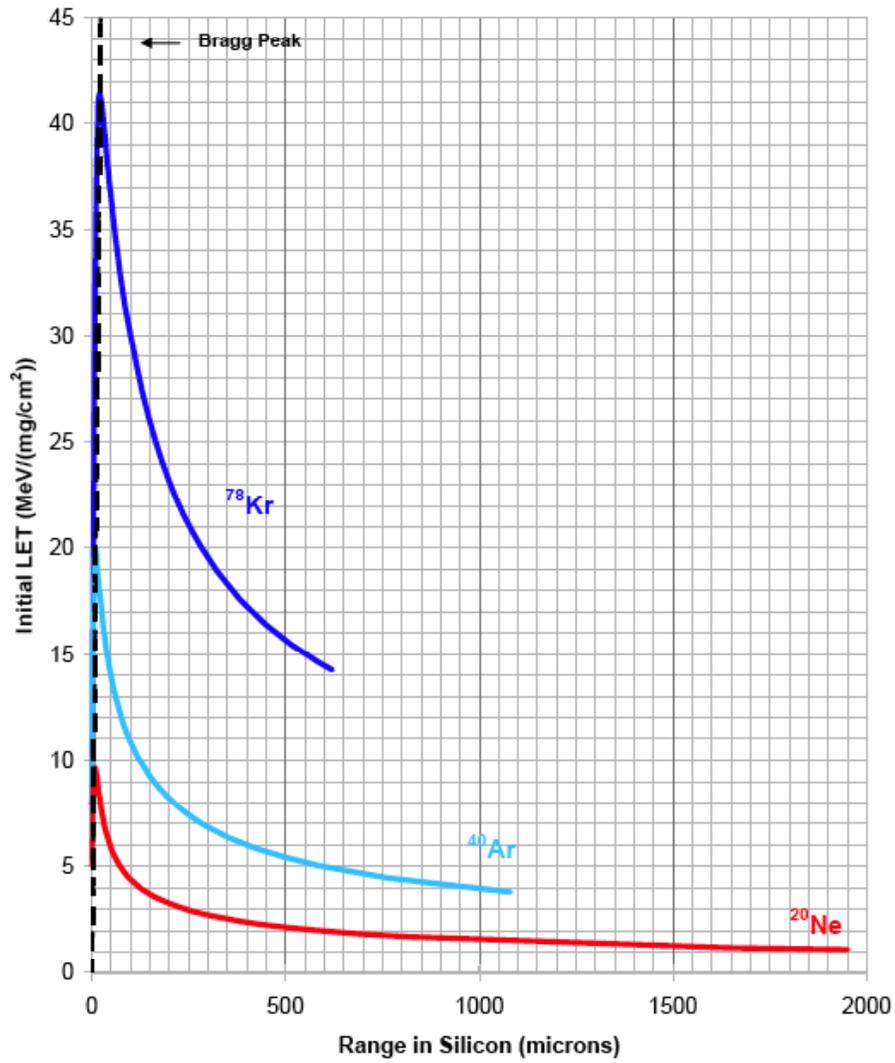


Fig.10. Variation of 40 MeV per nucleon ions with distance in silicon.

The European facilities are located at the Universite Catholique de Louvain la Neuve (UCL) Belgium and RADiation Effects Facility (RADEF) at University of Jyvaskyla, Finland. Table 7 and 8 show the energy and range of ions with energy range between 0.6 MeV and 27.5 MeV per nucleon for UCL facility. The LET values are the LET at the surface. Table 9 shows the energy and range of ions for RADEF in Finland.

**Table 7. High LET cocktail at UCL Belgium.**

<b>Ion</b>	<b>Energy (MeV)</b>	<b>LET at Normal Incidence (MeV-cm<sup>2</sup>/mg)</b>	<b>Range at Normal Incidence (µm)</b>
B	41	1.7	80
N	62	2.97	64
Ne	78	5.85	45
Ar	150	14.1	42
Kr	316	34	43
Xe	459	55.9	43

**Table 8. High penetration cocktail at UCL Belgium.**

<b>Ion</b>	<b>Energy (MeV)</b>	<b>LET at Normal Incidence (MeV-cm<sup>2</sup>/mg)</b>	<b>Range at Normal Incidence (µm)</b>
C	131	1.2	266
Ne	235	3.3	199
Si	236	6.8	106
Ar	372	10.1	119
Ni	500	21.9	85
Kr	756	32.4	92

**Table 9. Range of Ions at RADEF Finland**

<b>Ion</b>	<b>Energy (MeV)</b>	<b>LET at Normal Incidence (MeV-cm<sup>2</sup>/mg)</b>	<b>Range at Normal Incidence (µm)</b>
N	139	1.8	202
Ne	186	3.6	146
Si	278	6.4	130
Ar	372	10.1	118
Fe	523	18.5	97
Kr	768	32.1	94

## IV.B Proton Beam

Protons with energies above 65 MeV have sufficient range to pass through the thick substrate used in processors with inverted packages, although it may be necessary to correct for energy loss. The range of protons with energies between 15 and 100 MeV is shown in Table 10. Unless the substrate is thinned, it will be nearly impossible to determine the threshold proton energy for upset because of straggling and uncertainty in device thickness. Thus, although the proton cross section can be determined at high energies without modifying the device, it is necessary to use thinned devices in order to determine the energy threshold, typically less than 30 MeV.

**Table 10. Range of high-energy protons in silicon.**

Energy (MeV)	Range in Silicon ( $\mu\text{m}$ )	Range in Silicon (mils)
15	1,585	62.4
20	2,580	101.6
30	5,820	229.1
50	17,700	696.8
65	24,400	960.6
100	46,600	1,834

Proton testing can be done “in air,” with supporting equipment located close to the device. This makes proton testing inherently more straightforward compared to tests with heavy ions. However, relatively high fluences are required, which may induce TID damage in the device during a series of test runs. Proton cross sections for highly scaled devices are on the order of  $10^{-13}$  to  $10^{-14}$   $\text{cm}^2$  per bit. As an example, if 5,000 registers are used by the software in a specific test, a fluence of  $5 \times 10^{11}$   $\text{p}/\text{cm}^2$  is required to measure (on average) ten upsets if the cross section is  $10^{-14}$   $\text{cm}^2$  per bit.

## **V. Steps Required for Microprocessor Radiation Testing**

### **V.A Device Properties and Physical Preparation**

The first step is to determine the basic properties of the device that is to be tested. One of the most critical features is the package type. If flip-chip bonding is used, then the thickness of the chip must be measured to determine if mechanical thinning is required in order to do the tests. Some processors incorporate heat sinks at the back of the die (top of package). The heat sinks may have to be removed or modified in order for the ions to reach the active part of the device.

The next step is to do the required modifications and electrically test the device afterwards to ensure that it still functions correctly.

### **V.B Hardware Requirements**

Test boards must be fabricated (or, if commercial boards are used, adapted) that allow the device to be placed in front of the accelerator beam, with direct access to the device. Unless tests are done with an emulation system, other devices, such as memory, bridge chips, and power control, are placed on the test board. The test board must be thoroughly checked out to ensure that the processor works satisfactorily at the frequency that will be used for the tests.

Special diagnostic methods, such as JTAG, require additional connections to the test board.

The hardware must include a temperature sensor to measure the operating temperature of the device during operation. For the newer processors a routine can be developed to read out the processor's junction temperature.

### **V.C Operating System and Software**

An operating system must be selected. Primitive operating systems are recommended, as discussed earlier, but it is also possible to use more complex operating systems (i.e., Windows NT). However, it is far more difficult to distinguish functional errors in the processor from crashes in the operating system when a complex operating system is used.

Special software is usually developed for microprocessor testing unless the tests are intended to evaluate a specific software application. The general types of software that are required include:

1. Register tests, which load a predetermined pattern into several of the registers and continually evaluate the state of the registers, using a minimum of internal instructions in order to isolate register upsets.
2. Cache tests, which are analogous to register tests, but specifically test the internal cache memory.
3. Tests of specific instruction types or sequences.

### **V.D Testing**

The first step is to select the facility that will be used and the properties of the ions that are required.

Once at the facility, the test hardware is placed in front of the beam, evaluating the performance of the hardware and software to ensure that it functions properly with the beam off. This is an essential step because the cable length, noise, and general interface issues may be somewhat different at the facility compared to conditions in a more conventional laboratory.

After the hardware and software are checked out, the device is temporarily removed from the beam. The accelerator is tuned for the specific ion energies required, using appropriate diagnostics to measure the particle flux (and energy, if required).

The next step is to place the device in the beam, turn on the accelerator and use the software and hardware to evaluate the microprocessor operation. Generally this is done at several levels, starting with tests of basic registers and progressing to tests involving more complex operations of the device. During the irradiation, the processor temperature should be monitored and it is a good practice to keep the irradiation runs very short to prevent overheating the processor. Also, it is recommended to allow the time for the processor to cool between the successive irradiations when needed.

That step is repeated for other types of ions or for “degraded” ions where the energy has been reduced by inserting shields to lower the energy. When degraded beam is used, caution should be applied to make sure the ion has enough range to penetrate the sensitive region of the die.

Test data are recorded during the tests, including measurements of the particle fluence for each test run. If functional errors occur, then the fluence at which the functional error occurred must be estimated using the diagnostic methods that were developed for the test.

## **VI. Reporting and Interpretation of Results**

### **VI.A General Issues**

Test results must include a basic description of the approach used to test the devices, including the hardware and software that is used to evaluate the device, the operating frequency, and the operating system. Because of the complexity of microprocessors and their associated test methods, a far more thorough description of testing details is required than for more conventional devices.

Commercial microprocessors tend to evolve rapidly, with a confusing array of part numbers and specifications. Thus, including the full part number in the report will not provide enough information for data interpretation. The details listed below must be included, in addition to the part number and date code:

- a. Package type
- b. Special treatment of the device, such as thinning or repackaging
- c. Maximum rated operating frequency of the device
- d. Core voltage
- e. Feature size

The properties of the ion beams used for testing must also be included in the report, including corrections for energy loss.

There may be specific features of a processor that affect the results. For example, some types of processors allow cache error correction to be turned on. Alternatively, some microprocessor tests are done with specific application programs, not with more basic tests that allow upsets in registers, cache and other regions of the processor to be determined. Although application-specific software results are often the end goal of processor testing, the results tend to be of limited use unless the software is documented in a way that allows more general interpretation.

Finally, processors generate a great deal of heat, particularly when they are operated near maximum frequency. Device temperature should be monitored and reported.

### **VI.B Register and Cache Tests**

Register and cache tests can be treated in an analogous way to tests of static random-access memories. Just as for memories, it is essential to include error bars for counting statistics in the results. The type of pattern loaded into registers and cache should be included as well. The usual practice is to report such data as upsets per bit.

### **VI.C Functional Errors, Hangs, and Crashes**

Functional operation is the most critical problem for microprocessor tests, and it is also the most difficult feature to evaluate during testing. As discussed earlier, functional operation is somewhat dependent on the operating system that is used during testing. Unlike tests of registers or cache, functional errors are reported on an error-per-device basis. The basic features related to functional errors, hangs, and crashes that need to be reported include:

- a. Diagnostic results that partially isolate the operating system from the results, including JTAG.
- b. Fraction of the test runs that result in functional errors and an estimate of the cross section for functional errors compared to the cross section for registers and cache.

- c. Categorization of functional errors by the type of malfunction that occurs.
- d. Steps required for restoring operation, e.g., application of a RESET pulse or power removal and completing restart.

## VII. Test Results for Highly Scaled Microprocessors

### VII.A Registers and Cache

#### VII.A.1 PowerPC Microprocessors

Test results for several different PowerPC processors are shown in Fig.11, along with test results provided by the manufacturer of a radiation-hardened processor with the PowerPC architecture, the RAD6000. The feature size of the commercial processors is shown in parentheses. Tests of the commercial PowerPC devices were done with a development board, using an elementary operating system. Irradiations were done from the back of the die, using the long-range ions available at Texas A&M. Cache test results for the PowerPC processors are similar, with a slightly lower saturation cross section. The lower cross section is due to the smaller size of the transistors that are used in the cache memory. Cache test results for SOI processors with three different feature sizes are shown in Fig. 12 [22]. Despite the decrease in feature size, the threshold LET is essentially the same. The saturation cross section of the device with smaller feature size is slightly lower than the other devices.

Fig. 12 compares results of the SEU measurements for D-Cache of the Motorola PowerPC 7448 (90 nm feature size) to the results of the Motorola PowerPC 7457 (130-nm feature size). Also, for comparison the results for the Motorola PowerPC 7455 (180 nm feature size) are shown. The core voltage for the three measurements was 1.3 V. Even though the Motorola PowerPC 7448 processor has a much smaller feature size than the PowerPC 7455 and 7457, the LET threshold ( $LET_{th}$  is defined as the maximum LET value at which no effect was observed at an effective fluence of  $1 \times 10^7$  ions/cm<sup>2</sup>) is likely not very different. The LET threshold of the SOI PowerPC processors is about 1 MeV cm<sup>2</sup>/mg. The saturation cross section of the Motorola PowerPC 7448 is more than a factor of five lower than that of the other PowerPC processors with feature sizes of 130 and 180 nm. It is interesting to note that there is little difference between the saturated cross section for SOI PowerPCs with feature size of 130- and 180-nm, given the difference in feature size. These results suggest that scaling between 180- and 130-nm feature size has little effect on SEU sensitivity for these types of processors. However, this trend did not continue as device feature size was changed to 90 nm.

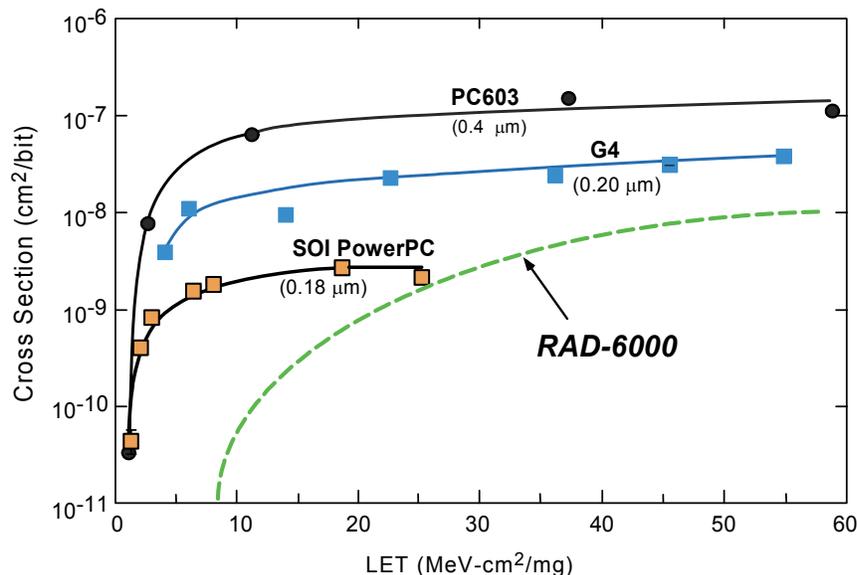


Fig. 11. Register test results for three different commercial PowerPC processors.

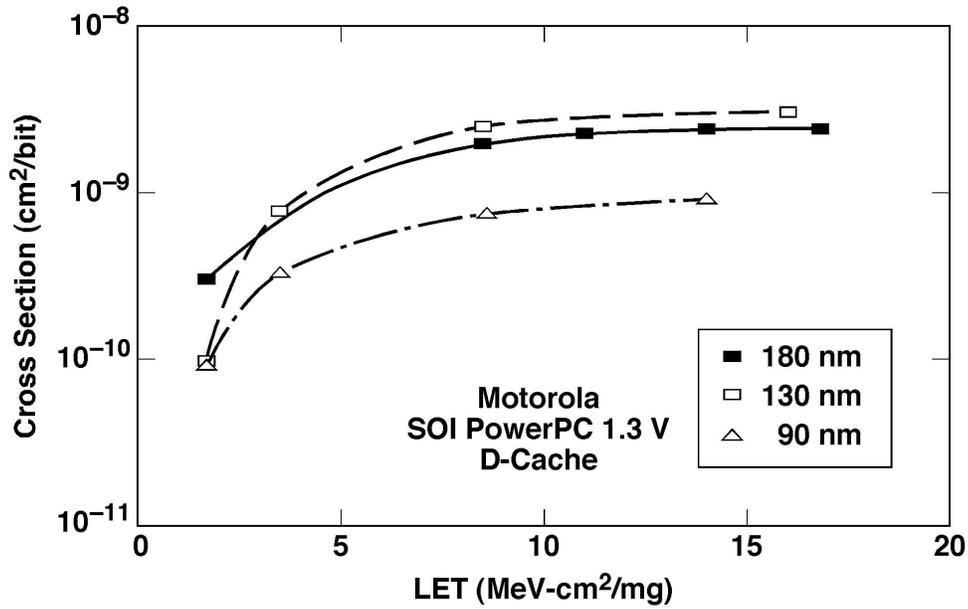


Fig. 12. Cache test results for three SOI PowerPC processors with different feature size [22].

Proton tests of registers are shown in Fig. 13. The proton cross section is about five orders of magnitude lower than the heavy ion cross section (Fig. 11), which is consistent with the lower interaction probability for protons because of the small nuclear cross section. The proton energy threshold is below 10 MeV.

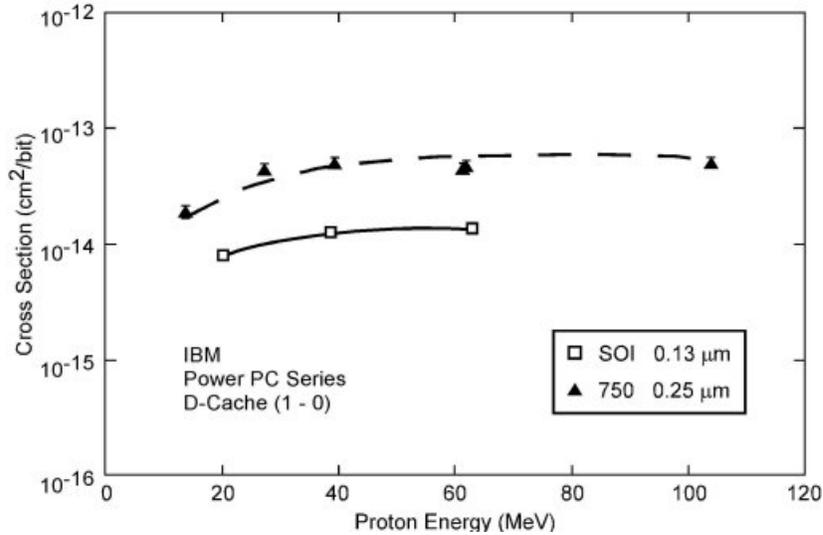


Fig. 13. Proton cross section for cache memory in two different PowerPC processors [14].

## VII.A.2 Intel Processors

Earlier work by Hiemstra [10] on proton tests of Intel processors was shown in Fig. 5. Heavy-ion tests of Intel processors were done by NASA GSFC group [11]. They tested the following:

1. CPU registers (ebx, ecx, ebp, and sdi)
2. Coprocessor registers
3. Data cache (L1 and L2) and memory (cache off)
4. Instruction cache
5. Coprocessor logic
6. MMX unit registers (pxor, por, pmul, pmulh, pads, addps, divps, and mulps)

Figs 14–16 show examples of their results. They are reported on the basis of total upsets at the device level rather than “per bit”. The Intel processors are more difficult to test because of higher power dissipation.

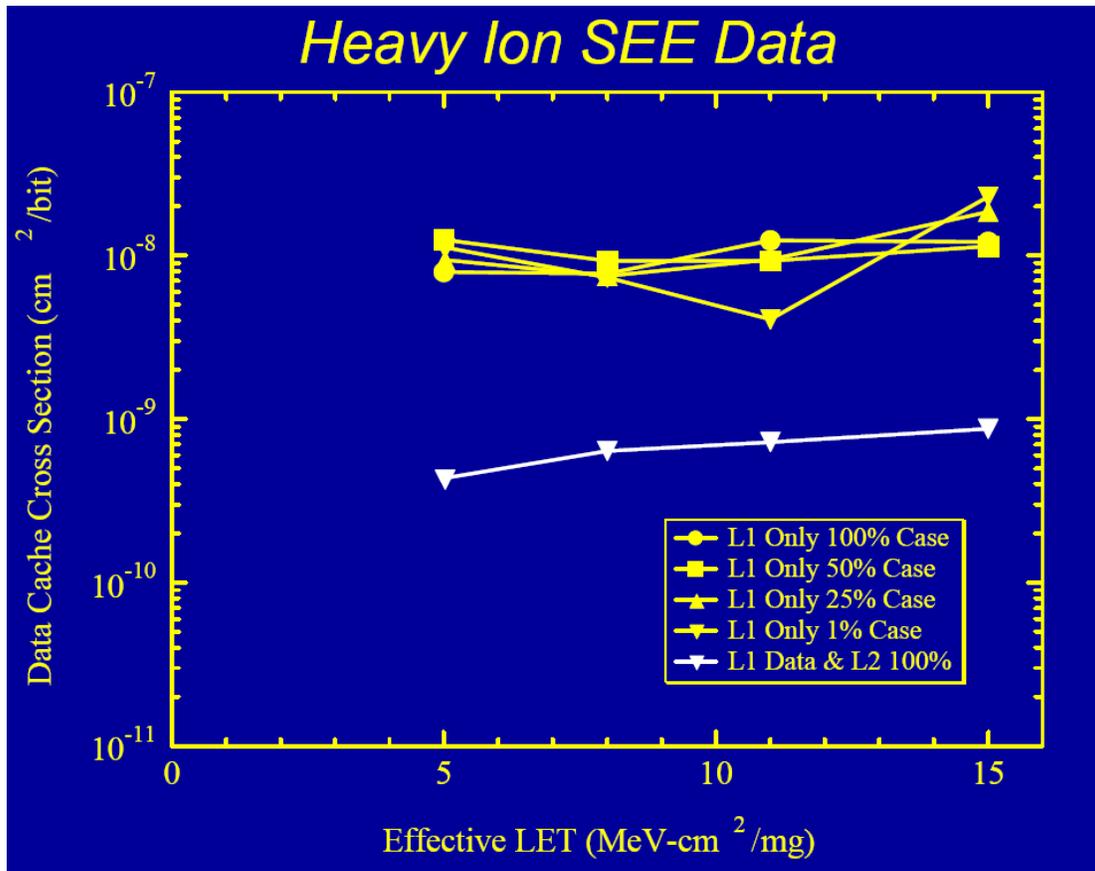


Fig. 14. Pentium III L1 cache upset cross section as a function of the Effective LET, for various test cases [11].

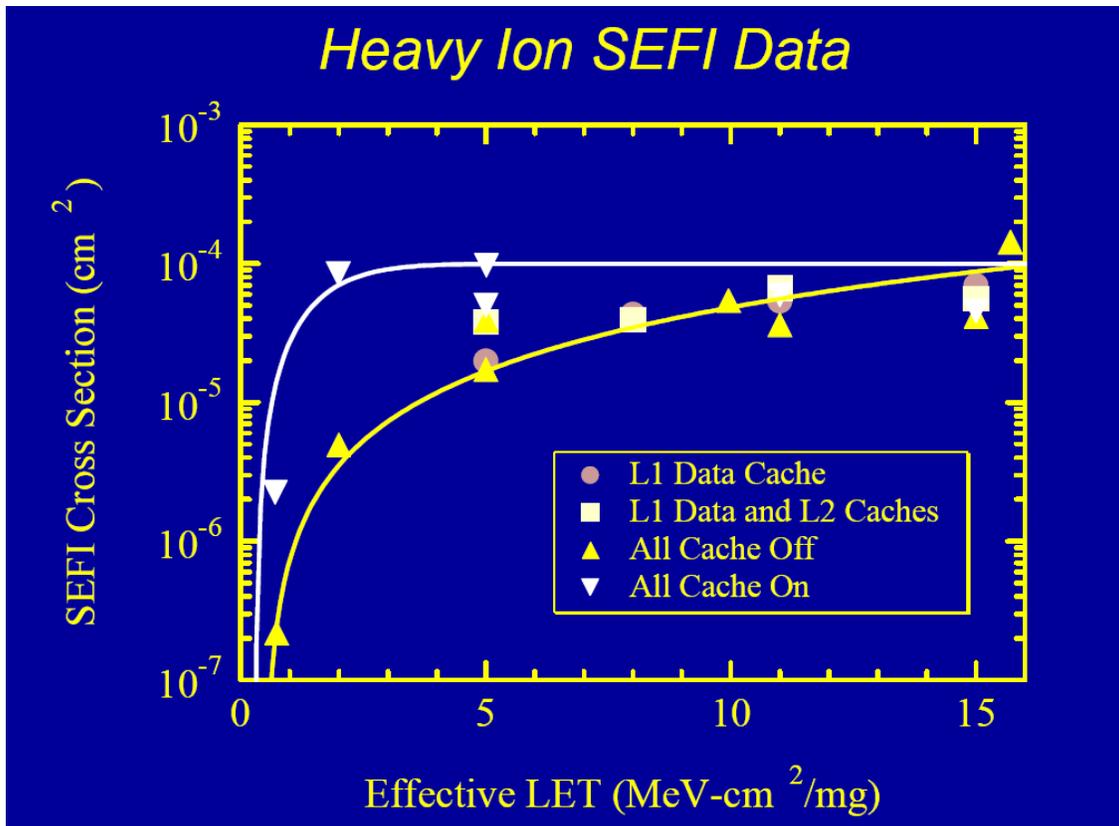


Fig. 15 Pentium III SEFI cross section as a function of the Effective LET, for various test cases [11].

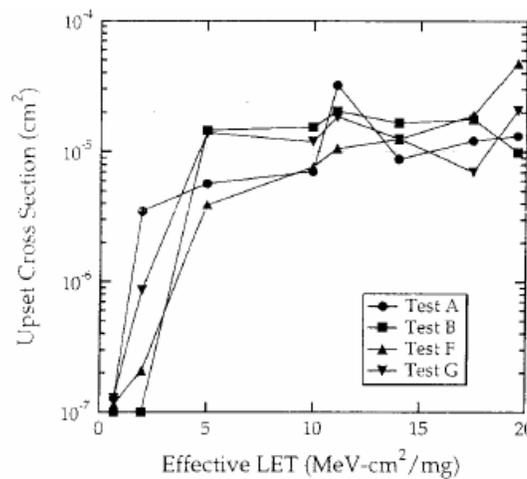


Fig. 16. Pentium III cross section as a function of the Effective LET, for tests A, B, F, and G (registers, coprocessor register, coprocessor logic, and MMX units) [11].

The Goddard group also measured proton single-event upset for registers, cache, floating point, and MMX units for Pentium III (P3) and AMD K7 processors [11]. They reported cross sections of about 10-11 cm<sup>2</sup>. In their measurements very few single-event upsets were actually observed. There were problems in data collection, as the SEFI rate was sufficiently high as to impact the duration of runs. The data had to be collected with the Cache Off or the SEFI would have been too high to collect any significant data.

## VII.B Frequency Dependence of Registers and Cache

One of the key questions regarding processor testing is the effect of clock frequency on test results. In principle, one would expect a higher upset rate when the clock frequency is near the maximum rated value. Such tests are difficult to do for several reasons. First, the noise margin and signal integrity of a test board that is modified for radiation testing may be sufficiently different from the conditions in a dedicated application which can prevent the determination of the frequency dependence. Note that modern microprocessors operate at clock frequencies  $> 1$  GHz. Second, a processor generates a great deal of heat when operated at maximum speed. It is difficult to extract heat from a processor that has been modified to provide direct access to the chip (or the back of the chip) by an ion beam, and the increase in temperature that occurs at high frequency may further interfere with attempts to measure frequency dependence.

Fig. 18 shows recent measurements of frequency dependence for register upsets in an SOI version of the PowerPC [17]. There is a slight increase in the cross section when the tests are done with a clock frequency of 1 GHz compared to tests at 350 MHz, but the effect is much smaller than implied by modeling studies for single-event transients. One reason for this is that although microprocessors operate at high switching speeds, the internal design has to be somewhat conservative in order to avoid yield problems.

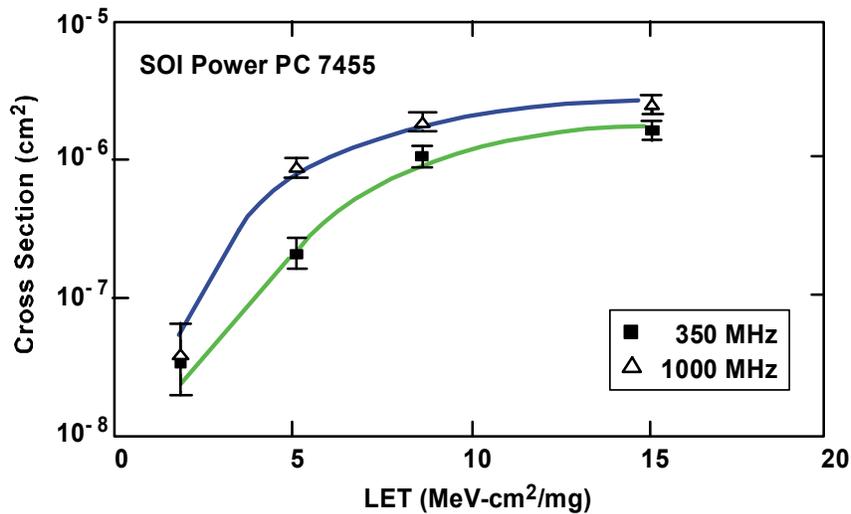


Fig.18. Frequency dependence of register tests of SOI PowerPC processors [17].

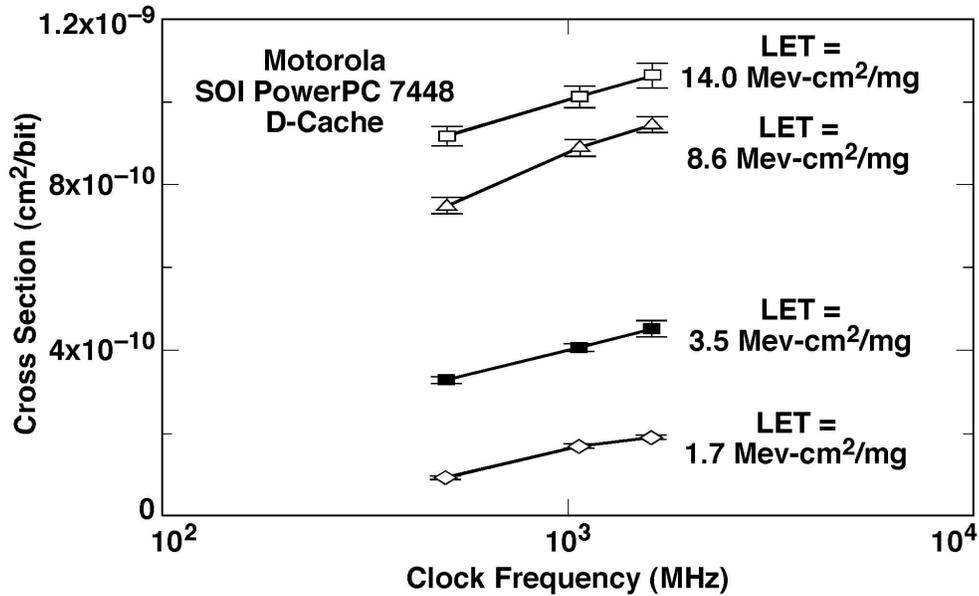


Fig. 19. Comparison of SEU cross-sections for D-Cache at clock speeds of 500, 1066, and 1600 MHz [21].

Fig. 19 compares the SEU measurements for the D-Cache of the Motorola PowerPC 7448 at three clock frequencies: 500, 1066, and 1600 MHz [21]. The cross section is plotted on a linear scale while the clock frequency is plotted on a logarithmic scale. The large number of storage locations within the D-Cache allows more statistically significant numbers of errors to be measured, decreasing the error bars due to counting statistics. The error bars are one sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols.

Fig. 19 clearly shows that the measured SEU rate increases with clock frequency. The difference in the SEU measurements is caused by the contribution from single-event transients (SETs). A SET in a digital circuit can manifest itself as a SEU in combinational logic cells, and it has been demonstrated that the SETs in logic circuits increase with increasing circuit clock frequency [32–35].

Fig. 20 compares the SEU measurements for Motorola PowerPC 7448 FPR at three clock frequencies: 500, 1066, and 1600 MHz [21]. The error bars are one sigma and result from Poisson statistics. Fig. 20 clearly shows that the measured SEU for FPR increases with clock frequency and there is a clock frequency dependence in the data. The cross section results with 1600 and 1066 MHz clock speeds are systematically larger compared with the results for a clock speed of 500 MHz. Similar to the D-Cache data, this is caused by the contribution from SETs.

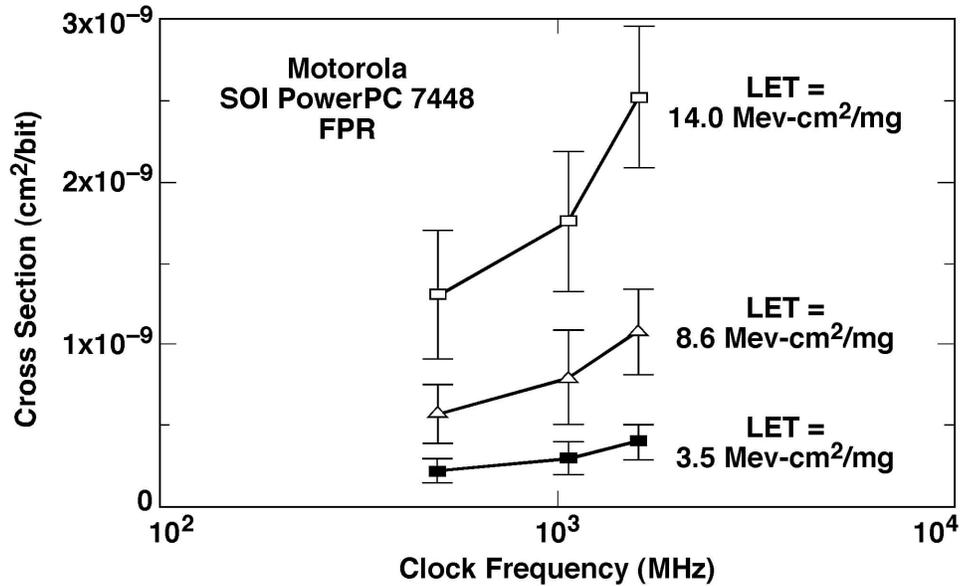


Fig. 20. Comparison of SEU cross-sections for FPR at clock speeds of 500, 1066, and 1600 MHz [21].

The frequency dependence of Intel Pentium III and AMD K7 processors has also been examined. Figs. 21 and 22 show the Pentium III and AMD K7 SEFI cross sections, respectively, as a function of the processor speed with various cache states [11]. It is quite obvious from these figures that the cache represents the most sensitive region of the processor and its operation causes the SEFI rate to increase by approximately a factor of 3 to 10. There is approximately a factor of three difference between Pentium III and K7 SEFI cross sections, with K7 being higher.

For the Pentium III, different rated processor speeds are shown with different symbols in Fig. 21. The K7 processors were not clocked down, so the data points shown in Fig. 22 are for the rated processor speed.

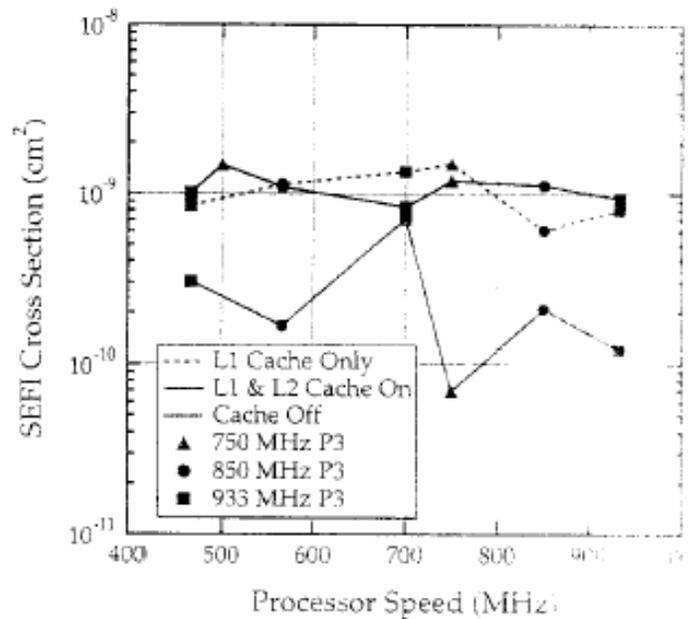


Fig. 21. Pentium III SEFI cross section as a function of the processor speed with various cache states. Note that the symbol shape represents the three different rated processor speeds used in the testing [11].

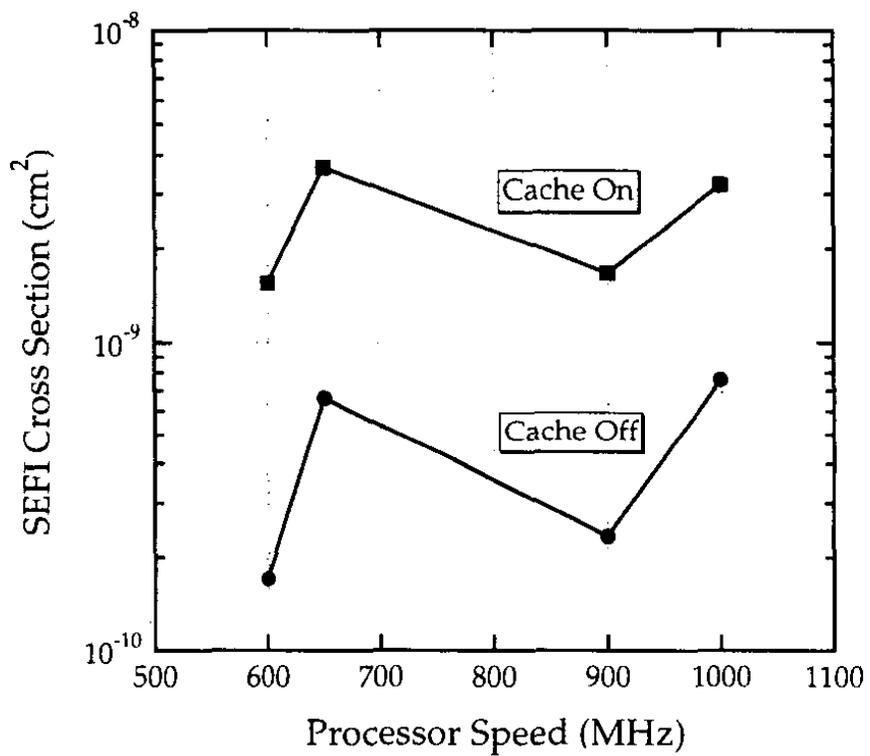


Fig. 22. AMD K7 SEFI cross section as a function of the processor speed with on/off cache states [11].

## VIII. Conclusion

The goal of this work is to develop a guideline that is applicable to microprocessors that are potentially useful in the space environment. This document is intended to be a guideline for radiation tests of microprocessors, in particular advanced commercial microprocessors, which have been the subject of several studies during the last 20 years. The main emphasis is on single-event upset testing, first because microprocessors are highly sensitive to single-event upset effects and, second, because there are many technical challenges in performing such tests on modern microprocessors. This guide is intended to support insertion of these microprocessors into spaceflight applications and to recommend ground test protocols. The first guideline principle that should be followed is a serious concurrent engineering approach for down selecting space-qualified microprocessors. This requires that the design engineer seek the support of a radiation effects expert who understands radiation issues for microprocessors as applied to the system in question. Radiation effects, particularly single-event effects, can be a significant problem for devices operating in space, particularly for microprocessors because of their complexity. Radiation tests are often required in order to allow estimates of upset rates caused by space radiation. The test results help to determine what kinds of effects are produced and how they can be detected and overcome. Complex failure modes are of particular interest because they potentially limit ways in which errors and malfunctions can be detected and corrected by hardware or software techniques.

In recent years there has been increased interest in the possible use of unhardened commercial microprocessors in space because they operate at higher speed and have superior electrical performance compared to hardened processors. Therefore, the main focus of this guideline is on high-performance commercial microprocessors. Those devices are evolving very rapidly because of performance pressure in the high-volume commercial marketplace. Feature sizes of commercial microprocessors are now at the 90 nm node with 65 nm soon to come, and processors are available that operate at clock frequencies of several GHz, providing much higher performance compared to hardened processors. However, unhardened devices are susceptible to upset and degradation from radiation, and more information is needed on how they respond to radiation before they can be used in space.

There is considerable interest in evaluating single-event upset effects at high frequency. Some of the initial work on frequency effects and radiation testing was discussed. However, the document does not make specific recommendations on testing devices at very high frequency because of the difficulties associated with board design and dealing with the very high power dissipation at high frequency (CMOS power dissipation is essentially proportional to frequency). Test fixture difficulties and power dissipation both act as interferences when tests are done at very high frequencies.

A basic method for improving the single-event effect immunity without degrading the performance is to reduce the single-event effect sensitive volume. This can be accomplished through the use of SOI substrates. For SOI processes, the charge collection depth for normally incident ions is reduced by more than an order of magnitude compared to similar processes fabricated on epitaxial substrates. Because of the much smaller charge collection depth, the SEU sensitivity of SOI devices is expected to be much reduced. However, other factors, such as lower operating voltages, reduced junction capacitance, and amplification by parasitic bipolar transistors, may limit the degree of improvement in single-event effect immunity that can be obtained with commercial SOI processors. We discussed in detail the radiation sensitivity, in particular single-event effect in commercial microprocessors with the PowerPC architecture. These devices used partially depleted SOI processes to improve performance, which use a tub depth between 0.09 and 0.18  $\mu\text{m}$ , reducing the charge collection depth for normally incident ions by more than an order of magnitude compared to similar processes with conventional isolation (on thin epitaxial substrates). The trend for commercial SOI microprocessors is to reduce feature size and internal core voltage and increase the clock frequency. Commercial microprocessors

with the PowerPC architecture are now available that use partially depleted SOI processes with feature size of 90 nm and internal core voltage as low as 1.0 V and clock frequency in the GHz range. The upset rates of commercial SOI microprocessors with the PowerPC architecture are low enough to allow their use in space applications where occasional upsets can be tolerated. Although a small number of “hangs” were observed during radiation tests, the cross section for this type of functional error is low enough so that “hangs” are expected only occasionally, with an estimated rate of one in 25 years from galactic cosmic rays in deep space. Also, we extend focus of this guideline to highly scaled, high speed advanced CMOS processors such as Intel Pentium and AMD K7. The Intel Pentium and AMDK7 have been tested extensively for total ionizing dose and single-event effects. These processors have been found to be extremely tolerant to total ionizing dose and no radiation induced latchups have been observed with protons or heavy ions to an LET of approximately 15 MeV-cm<sup>2</sup>/mg. In addition, for Intel Pentium III, if running with the caches disabled is an option and with mitigation in place, these events may be controllable to allow for operation in the space environment.

Microprocessors have changed radically during the last 20 years. The earliest devices used 4 bits, with very primitive capability, but quickly evolved to 8 bits. The key points are the drastic reduction in feature size, and the development of SOI processors during the last five years. The new microprocessors contain large amounts of internal cache memory, increasing the total cross section for upsets if the cache is used. Until recently most processor development concentrated on increasing clock frequency and adding architectural improvements such as advanced pipelining, out-of-order instruction sequencing, and increasing the size of on-board cache to increase throughput. At the present time there are several distinct branches in processor development because of the extremely high power dissipation that occurs in microprocessors that are intended for maximum clock frequency and throughput. That branch, driven heavily by performance, is intended for server applications where the high power dissipation can be accounted for in overall system design; such devices are nearly impossible to use in space because of the extreme difficulty of cooling. A second branch of microprocessor design is intended for mainstream desktop computer applications. Those devices can also dissipate relatively large amounts of power—as much as 100 W. Although it is conceivable that such devices could be used in space, the high power dissipation is a major drawback. The third branch of microprocessor design decreases power dissipation to develop intermediate performance levels with power dissipation below 20 W. These distinctions are important because (1) high-performance processors use complex packages with massive heat sinks that make it very difficult to perform radiation tests; and (2) the predictions of the Semiconductor Industry Roadmap are very different for high-performance, desktop, and reduced power microprocessors, which can lead to erroneous conclusions about the performance and features of microprocessors.

Designing a board to allow the processor to operate is difficult, particularly for processors with clock frequencies above 100 MHz. The interface logic levels have been reduced from 5 V for older processors to 1.1 V for more advanced processors. Terminated connections or differential line driver/line receiver pairs must be used at all interfaces. Errors or oversights in board design can lead to sporadic operation that will interfere with radiation tests. In most cases the development boards that are available from mainstream microprocessor manufacturers have been carefully designed and checked out for operation under worst-case conditions.

Although packaging is usually considered to be of secondary importance for radiation testing, the specific package type used for microprocessors has a large impact on radiation testing because of the difficulty of transporting heavy ions through the package. Modern microprocessors typically use “inverted” packaging with a ball-grid array. Contacts on the active surface of the die are made with a ceramic substrate. Pins (or direct connection to a circuit board) are attached to the ceramic substrate. Because of this inverted structure and the large number of pins, it is not practical to remove the die from this inverted configuration and to repackage it so that the active surface is at the top. Consequently, for radiation testing with heavy ions, it is necessary to maintain the inverted configuration, irradiating the device through the back of the package. The ion used for testing must have sufficient range to pass through the surface of the die, or the die thickness must be reduced.

Typical die thicknesses are approximately 750-900  $\mu\text{m}$ . Relatively few ions are available with a range of this magnitude, severely limiting heavy-ion tests. Ion range was discussed in more detail.

Various mechanical methods can be used to reduce the thickness of the back of a microprocessor die, allowing particles with less range to be used for testing. One method uses a high-speed diamond abrasive tool. It should be noted that, as a consequence of back thinning, the thermal issue becomes more severe, particularly during radiation testing, and heat removal techniques should be applied. There might be some concerns that if the die is too thin, it might affect the charge collection and consequently influence the outcome of the radiation testing.

The processors and the other components on the test board dissipate considerable amounts of heat. These devices can dissipate relatively large amounts of power—as much as 100 W. Although it is conceivable that such devices could be used in space, the high power dissipation is a major drawback. Commercial processors usually are packaged with an external heat sink on the top for heat removal. High-performance processors use complex packages with massive heat sinks that make it very difficult to perform radiation tests. Particularly, heat is a major problem when the testing is done in a vacuum and processors tend to overheat. During the radiation testing it is necessary to modify the original heat sink to allow for beam access or replace it with a custom made heat sink. The radiation data should be collected by allowing time for the processor to cool between successive irradiations when needed. Also, to prevent over heating, the radiation runs should be kept short. A thermocouple can be used to measure the temperature. For the newer processors a routine can be developed to read out the processor's junction temperature.

The response of a microprocessor to radiation depends on software as well as hardware. Although it is possible to operate a processor with dedicated machine-language instructions and avoid the need for an operating system, this is generally impractical for the complex processors that are used today, partly because of the need for a bridge chip (or emulated equivalent) to perform most of the I/O and memory interface functions. Minimizing processor activity during irradiation essentially reduces the number of internal operations, thereby making the operation susceptible to errors in only a few internal locations. Nearly all microprocessor testing is done with some form of operating system. Development boards typically contain very basic operating systems. If a complex operating system is used, it will heavily influence the results and may interfere with attempts to characterize the basic response of the processor. Thus, very primitive operating systems are preferred for microprocessor testing. Note however that tests with complex operating systems may be the preferred approach if they are actually used in the application.

A number of assembly language software programs need to be written to detect errors in various sections of the processor. It is possible to design software that primarily exercises specific registers, cache, or regions and thus allows the number of errors to be determined for various registers, cache, or specific operating modes. There are two methods of testing the registers, semi-static and semi-dynamic, which were explained in detail in the previous sections.

The active region of high-performance processors is very thin, typically about 2-3  $\mu\text{m}$  or less. However, as discussed in Section II, the inverted package used for microprocessors requires irradiation from the back of the package. The thickness of a typical microprocessor die is 700-900  $\mu\text{m}$ . In order to test such a device, the range of the ion beam must exceed the die thickness. Note that there is significant energy loss by such beams as they travel through such thick regions, requiring correction for energy loss. The beams that are available for five commonly used accelerators were discussed in a previous section. The LET varies rapidly with distance near the end of the range and, thus, it is necessary to know the die thickness to within about 2%. Ar, Ne, and Kr ions can be used on devices where the back of the substrate has been reduced by mechanical thinning. Protons with energies above 65 MeV have sufficient range to get through the thick substrate used in processors with inverted packages, although it may be necessary to correct for energy loss. Unless the substrate is thinned, it will be nearly impossible to determine the threshold proton energy for upset because of straggling and uncertainty in device thickness. Thus, although the proton cross section can be determined at high

energies without modifying the device, it is necessary to use thinned devices in order to determine the energy threshold, typically less than 30 MeV.

Finally, the way the test results should be presented was discussed. Test results must include a basic description of the approach used to test the devices, including the hardware and software that is used to evaluate the device, the operating frequency, and the operating system. Because of the complexity of microprocessors and their associated test methods, a far more thorough description of testing details is required than for more conventional devices. Commercial microprocessors tend to evolve rapidly, with a confusing array of part numbers and specifications. Thus, including the full part number in the report will not provide enough information for data interpretation. In addition to the part number and date code, package type, special treatment of the device (such as thinning or repackaging), maximum rated operating frequency of the device, core voltage, and feature size should be included in the test report. Also, the properties of the ion beams used for testing must also be included in the report, including corrections for energy loss. Finally, processors generate a great deal of heat, particularly when they are operated near maximum frequency. Device temperature should be monitored and reported.

## **IX. Acknowledgments**

The author gratefully acknowledges A. H. Johnston and G. M. Swift for helpful discussions and for their contribution to the guideline. Also, the author would like to thank C. E. Barnes for reviewing the guideline.

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