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Accumulate Repeat Accumulate Coded Modulation

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Abstract— In this paper we propose an innovative coded modulation scheme called "Accumulate Repeat Accumulate Coded Modulation" (ARA coded modulation). This class of codes can be viewed as serial turbo-like codes, or as a subclass of Low Density Parity Check (LDPC) codes that are combined with high level modulation. Thus at the decoder belief propagation can be used for iterative decoding of ARA coded modulation on a graph, provided a demapper transforms the received inphase and quadrature samples to reliability of the bits. The structure of encoder for this class can be viewed as precoded Repeat Accumulate (RA) code or as precoded Irregular Repeat Accumulate (IRA) code when combined with high order modulation, where simply an accumulator is chosen as a precoder to improve the performance. The ARA coded modulation has a simple, and a very fast encoder structure when representing LDPC coded modulation. Based on density evolution through some examples for ARA code with BPSK modulation, we show that for maximum variable node degree 5 a minimum bit SNR as low as 0.2 dB from channel capacity for code rates $1/2$, $2/3$, and $3/4$ can be achieved as the block size goes to infinity. Thus based on fixed low maximum variable node degree, its threshold outperforms not only the RA and IRA codes but also the best known unstructured irregular LDPC codes reported in the literature. Iterative decoding simulation results are provided for BPSK, QPSK, 8PSK, and 16QAM modulations over additive white Gaussian noise. The ARA code also has projected graph or protograph representation, that allows for high speed decoder implementation.

Topics: LDPC coded modulation, Turbo-like coded modulation, MPSK, 16QAM, iterative decoding on graphs, density evolution, protographs

I. INTRODUCTION

Low Density Parity Check (LDPC) codes were proposed by Gallager [1] in 1962. After introduction of turbo codes by Berrou et al [2] in 1993, researchers revisited the LDPC codes, and extended the work of Gallager. After 1993 over 500 contributions have been made to LDPC codes see for example [10], [12], [13], [14], [15] and references there.

Recently RA [4] and IRA [5] codes, as simple subclasses of LDPC codes with fast encoder structure, were proposed. As

turbo-like codes this class can also be considered as a serial concatenated code class [16]. Classical RA codes, in addition to simplicity, have reasonably good performance with iterative decoding threshold within 1 dB of capacity for rates less than or equal to $1/3$. RA codes use fixed repetition for input bits. On the other hand, IRA codes inspired by RA and irregular LDPC [3] codes have irregular repetition for input bits. For IRA codes, node degree distribution can be optimized to achieve low thresholds. To achieve very low threshold for IRA, as for LDPC codes, maximum repetition for some portion of input bits can be very high. These recent results on RA and IRA codes, which have fast encoders, motivated us to find a way to enhance the performance of these class of codes and RA codes in particular. Researchers in [7], tried to improve the input-output extrinsic SNR behavior of the outer convolutional codes in serial concatenation in low extrinsic SNR region to lower SNR threshold of serial concatenation by using repetition of certain bits of the outer code. On the other hand if a repetition code is used as an outer code such as in RA codes, one should try to improve the input-output extrinsic SNR behavior at the high extrinsic SNR region, since the input-output extrinsic SNR behavior of repetition codes are excellent in the low extrinsic SNR region. We discovered that an accumulator as a rate-1 precoder applied before the repetition code will improve the performance. Before elaborating on the role of accumulator as a precoder for RA codes and graph representation of ARA codes, we use the definition of projected graph introduced in [8], [9], [11] for implementation of the decoder for LDPC codes which shows that if an LDPC code can be represented by a smallest base-graph (projected graph) then high speed implementation of the decoder will be more feasible. Similar definition also is provided in [6] for base-graph which was called protograph. This definition also facilitates the minimal graph representation for overall graph description of LDPC codes. In fact we will show that ARA codes have such projected graph or protograph representation which is another added value.

A protograph [6] is a Tanner graph with a relatively small number of nodes. A protograph $G = (V, C, E)$ consists of a set of variable nodes V , a set of check nodes C , and a set of edges E . Each edge $e \in E$ connects a variable node $v_e \in V$ to a check node $c_e \in C$. Parallel edges are permitted, so the mapping $e \rightarrow (v_e, c_e) \in V \times C$ is not necessarily 1:1. As a simple example, we consider the protograph shown in Fig. 1 (b). This graph consists of $|V| = 4$ variable nodes and $|C| = 3$ check nodes, connected by $|E| = 9$ edges. The four variable nodes in the protograph are denoted by types 0, 1, 2, 3, and the three check nodes by types 0, 1, 2. By itself, this graph may be recognized as the Tanner graph of a rate 1/3 LDPC code (in this case, a Repeat and Accumulate code Fig. 1 (a)). In Fig. 1 (b), the variable nodes connected to the channel are shown with dark filled circles. Blank circles are those variable nodes not connected to the channel (i.e. punctured). Check nodes are circles with inside plus sign. We can obtain a larger graph by a copy-and-permute operation. For the details on protographs see [6]. The resulting larger graph is called the derived graph, and the corresponding LDPC code is a protograph code. In general, we can apply the copy-and-permute operation to any protograph to obtain derived graphs of different sizes. This operation consists of first making T copies of the protograph, and then permuting the endpoints of each edge among the T variable and T check nodes connected to the set of T edges copied from the same edge in the protograph. In Fig. 1 (b), the minimum E_b/N_o threshold of RA code with iterative decoding is also shown.

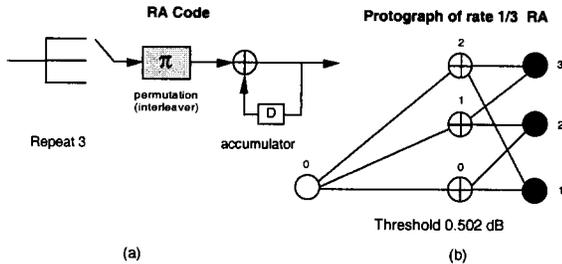


Fig. 1. (a) RA code, (b) Protograph of rate 1/3 RA code with repetition 3

Hui Jin et al [5] proposed Irregular RA (IRA) code which is a serial concatenation of a simple LDPC code with different degree variable nodes (irregular repetition) as an outer code and an accumulator as an inner code to generalize the RA code. The encoder can be implemented by repetition codes, Exclusive OR's, and an accumulator as shown in Fig. 2.

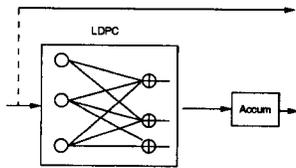


Fig. 2. IRA code

II. PUNCTURED RA AND ALTERNATIVE ENCODING OF IRA CODES

Rate 1/2 classical RA code has high threshold of 3.01 dB. Lower threshold for rate 1/2 RA can be obtained if we puncture the accumulator, provided that the repetition is greater than or equal to 3, and the systematic bits are transmitted through the channel i.e. systematic punctured RA. Based on an equivalent graph of a punctured accumulator, we obtain the protograph of systematic punctured RA with threshold 1.116 dB. This is an improvement close to 2 dB. The systematic punctured RA and its protograph is shown in Fig. 3.

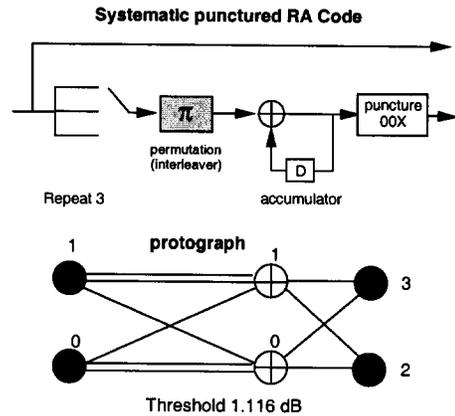


Fig. 3. Systematic punctured RA code

The immediate consequence of this observation suggests an alternative encoding structure for systematic IRA codes by just using irregular repetition, permutation, and punctured accumulator. An example of rate 1/2 systematic IRA, the encoder and the corresponding protograph is shown in Fig. 4. The threshold for this example is 0.946 dB.

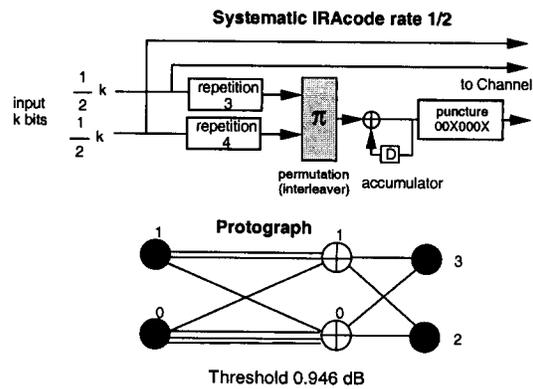


Fig. 4. Systematic IRA

III. ACCUMULATE-REPEAT-ACCUMULATE CODES

Let us consider a rate 1/3 serial concatenated code where the outer code is a repetition 3 code. Assume the systematic bits

are transmitted to the channel. Alternatively consider the same outer code but the repetition 3 is precoded by an accumulator. Let us compare the extrinsic SNR behavior of these two outer codes using Gaussian density evolution as shown in Fig. 5. As the Gaussian density evolution analysis shows, the use of a rate-1 accumulator dramatically improves the extrinsic SNR behavior of repetition 3 at high extrinsic SNR region. However it slightly deteriorates the behavior of repetition code at very low extrinsic SNR region.

Now let us use a punctured accumulator as an inner code. The periodic puncturing pattern in this example is X0X where 0's indicate the puncturing positions. Since the serial concatenation consists of outer accumulator, middle repetition, and inner accumulator, we call it Accumulate-Repeat-Accumulate (ARA) code. The rate 1/3 ARA, and the extrinsic input-output SNR curves using Gaussian density evolution are shown in Fig. 5.

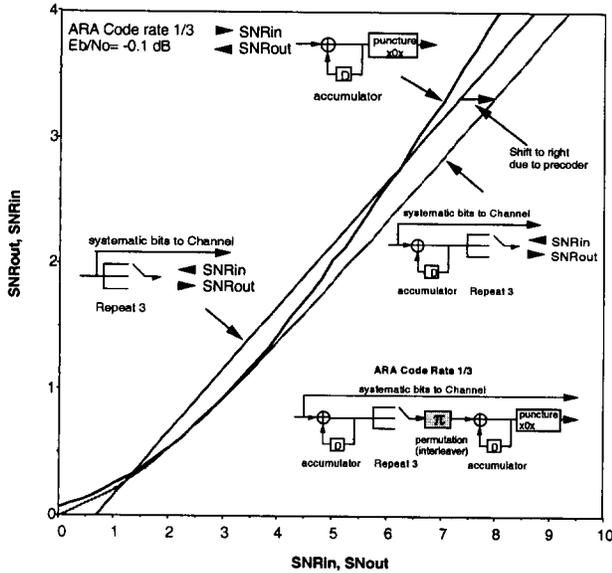


Fig. 5. Gaussian density evolution for rate 1/3 ARA

Gaussian density evolution provide an approximate threshold. Next we present the protograph for this rate 1/3 ARA code, and compute its threshold using density evolution. The protograph and computed threshold of -0.048 dB are shown in Fig. 6. This threshold shows 0.55 dB improvement over classical RA code. If we remove the precoder the threshold will be 0.73 dB. These comparisons will be fair if we fix the maximum variable node degree. Shortly we will show such comparisons with rate 1/2 LDPC codes.

In a similar way we can construct rate 1/2 ARA code. However, due to more puncturing of the inner accumulator, some portion of input before repetition should not be passed through the precoder to allow the iterative decoding to start. An example of a simple rate 1/2 ARA, its protograph, and the corresponding threshold are shown in Fig. 7. In fact this is the precoded version of the punctured RA example with

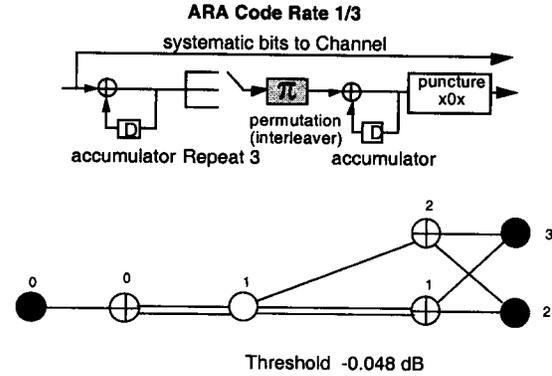


Fig. 6. Rate 1/3 ARA, and the corresponding protograph representation

repetition 3 that was discussed previously. The threshold for that punctured RA example was 1.116 dB. The precoded version now has threshold of 0.516 dB that shows 0.6 dB gain due to use of precoder. Higher code rate family is obtained by just puncturing this ARA code example, and it is shown in Fig. 8.

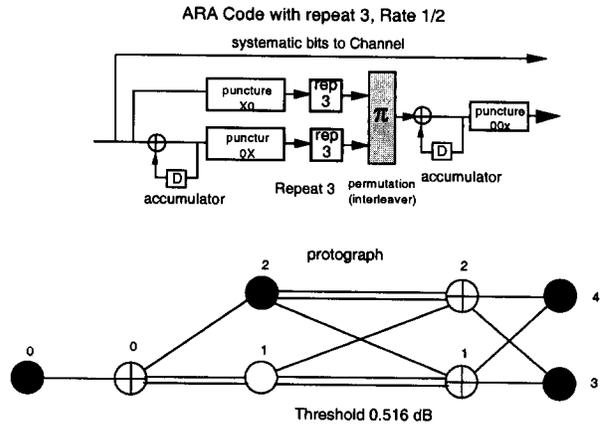
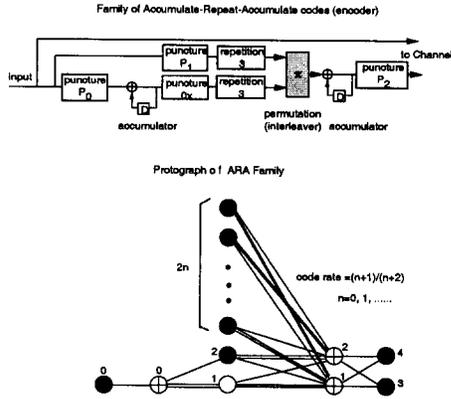


Fig. 7. Rate 1/2 ARA, and the corresponding protograph representation

Instead of using regular repetition in ARA, if we use irregular repetition then we refer to it as Irregular ARA or simply IARA code. Slightly better threshold can be obtained with IARA. In this paper we consider only regular ARA for construction of coded modulation schemes. However we provide a simple example of rate 1/2 IARA that has low threshold of 0.264 dB (0.08 dB from capacity limit for rate 1/2), and its protograph is shown in Fig. 9.

The protograph has maximum degree 5. The best rate 1/2 unstructured irregular LDPC with maximum degree 5 in [3] has threshold 0.72 dB i.e. 0.45 dB improvement. There are few reasons for such difference. In [3], the degree of variable nodes are greater or equal to 2, and punctured variable nodes were not allowed. If we look at protographs of ARA, it contains degree 1 variable nodes and punctured variable nodes. But this is not the main reason. In fact, later Richardson and



Code Rate	Protograph Threshold	Capacity	Difference	Puncturing Patterns		
				P ₀	P ₁	P ₂
1/2	0.516	0.187	0.329	XX	X0	00X
2/3	1.288	1.059	0.229	00XX	X0X0	00000X
3/4	1.848	1.626	0.222	0000XX	X000X0	0000000X
4/5	2.277	2.040	0.237	000000XX	X00000X0	000000000X
5/6	2.620	2.362	0.258	00000000XX	X0000000X0	00000000000X
6/7	2.897	2.625	0.272	0000000000XX	X000000000X0	0000000000000X
7/8	3.129	2.845	0.284	000000000000XX	X00000000000X0	000000000000000X

Fig. 8. ARA code family for rates 1/2 to 7/8, encoder, protographs, and table of thresholds in dB

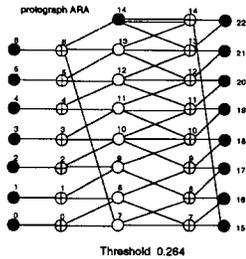


Fig. 9. A rate 1/2 very low threshold ARA protograph

Urbanke [9], [11] mentioned that the degree 1 variable nodes and punctured variable nodes also can be used in LDPC code design but more than that they mentioned that the so called "multi edge" representation can be used in the LDPC code design. The "multi edge" in ARA code design simply means that the structure of interleaver in ARA codes should be based on edge connections in the ARA protograph between middle variable and inner check nodes (right most check nodes), i.e. between repetition and accumulator.

IV. ARA CODED MODULATION

The basic structure of ARA coded modulation is shown in Fig. 10. In the ARA coded modulation construction, the systematic bits are mapped to the MSB in the mapping. The LSB of the mapping is assigned to the parity bits in the ARA code. For ARA coded modulation we also consider another example that uses repetition 4 instead of 3. The threshold of this ARA for binary modulation is 0.56 dB but it shows a lower error floor and performs better with 8PSK and 16QAM in the simulations. The encoder and protograph of this example

is shown in Fig. 11. Simulation results for random type

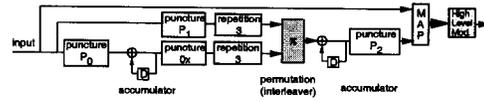


Fig. 10. Basic structure of accumulate repeat accumulate coded modulation

interleavers are shown in Fig. 11 for two examples of rate 1/2 ARA combined with QPSK modulation using Gray code mapping. The simulation results are compared with a rate 1/2 turbo code with well optimized spread interleaver with QPSK modulation. We can also combine the same 1/2 ARA with 8PSK or 16QAM modulations to achieve throughput of 1.5 bps/Hz and 2 bps/Hz respectively using ideal Nyquist filtering. The simulation results are shown in Fig. 12 and Fig. 13. Finally we combined rate 2/3 ARA with 8PSK to achieve throughput of 2 bps/Hz. The simulation results are shown in Fig. 14. For this case we also compared our results with Binary Turbo code combined with 8PSK modulation for input block of 4096 that was reported in [18](Fig. 7), and the best result for turbo TCM (TTCM) that was reported in [17](Fig. 3) for input block of 4000. In all cases we used random type interleavers in our simulations. Thus we observe error floor in BER below 10^{-6} . We are in process of designing spread type interleavers to lower the error floor. In the simulations, we allowed maximum iterations between variable and check nodes to be 100. However during the iteration if the decoder finds a valid code word then iterations are stopped. Thus the average number of iterations is much lower than 100.

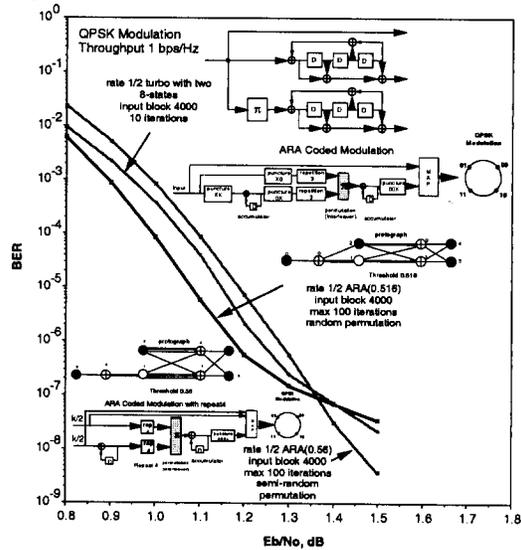


Fig. 11. Simulation results for throughput 1 ARA coded modulation

V. CONCLUSION

In this paper we proposed a new coded modulation scheme called Accumulate Repeat Accumulate coded modulation (ARA coded modulation). The ARA coded modulation as a

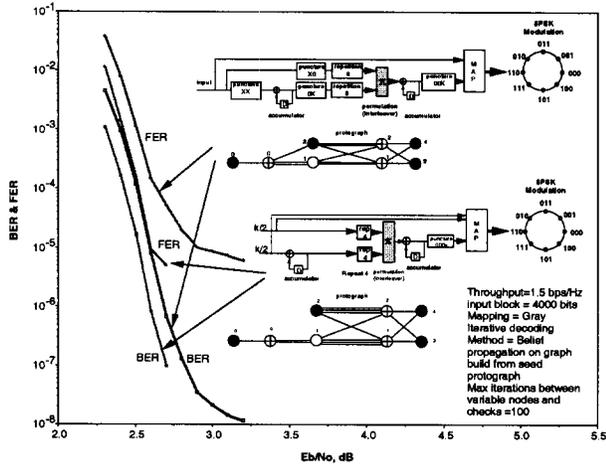


Fig. 12. Simulation results for accumulate repeat accumulate coded modulation with 8PSK, throughput=1.5

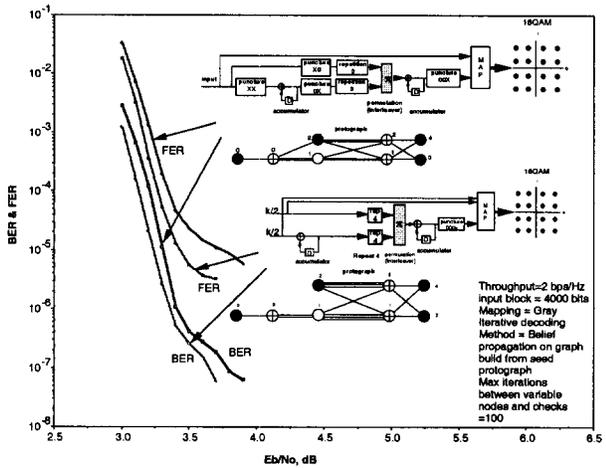


Fig. 13. Simulation results for accumulate repeat accumulate coded modulation with 16QAM, throughput=2

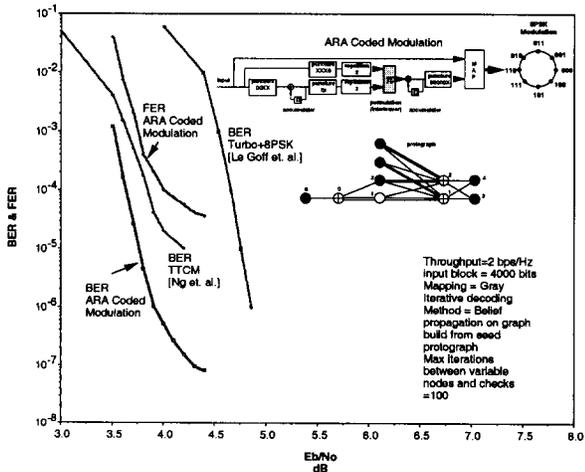


Fig. 14. Simulation results for accumulate repeat accumulate coded modulation with 8PSK, throughput=2

subclass of LDPC coded modulation has a fast encoder, the same encoder with proper puncturing can be used for various types of modulations, the same decoder with message passing on a graph with proper de-puncturing can be used to decode various modulations. Iterative decoding simulation results are provided for QPSK, 8PSK, and 16QAM modulations which are better than turbo coded modulation by few tenth of dB. The ARA codes have protograph representation, that allows for high speed implementation of the decoder.

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