Evaluation of the Telecommunications Protocol Processing Subsystem Using Reconfigurable Interoperable Gate Array

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Abstract -- The current implementation of the Telecommunications Protocol Processing Subsystem Using Reconfigurable Interoperable Gate Arrays (TRIGA) is equipped with CFDP protocol and CCSDS Telemetry and Telecommand framing schemes to replace the CPU intensive software counterpart implementation for reliable deep space communication. We present the hardware/software co-design methodology used to accomplish high data rate throughput. The hardware CFDP protocol stack implementation is then compared against the two recent flight implementations. The results from our experiments show that TRIGA offers more than 3 orders of magnitude throughput improvement with less than one-tenth of the power consumption.

Keywords: CFDP, protocol processing hardware, reconfigurable hardware and deep space telemetry

Introduction and Background

The Consultative Committee for Space Data Systems (CCSDS) File Delivery Protocol (CFDP) was created to automate data transfer across inter-planetary distances. Although CFDP and its complementary CCSDS protocol stack provide an automated, reliable and robust file transfer protocol, they are processor intensive. To offload the communications protocol-related tasks from the Command and Data Handling (C&DH) computer, we developed the Telecommunication Protocol Processing Subsystem for Reconfigurable Interoperable Gate Array (TRIGA) that implements the functionality of CCSDS file delivery and framing layers on a Virtex II Pro FPGA [1].

As show in Table 1, recent NASA JPL missions, Deep Impact (DI) and Mars Reconnaissance Orbiter (MRO), employ CFDP as their file transfer mechanism. Although both missions use CFDP in unacknowledged mode, their implementation strategies differ in the hardware and software partitioning of the protocol stack functions. MRO accomplishes virtually all of the protocol stack layers above the physical layer in software while DI implements Telecommand / Telemetry (TM/TC) framing in hardware. Both approaches pose heavy processing requirement on C&DH computer to support high throughput CFDP communication because software implementations use multiple message queues, pipes and threads to establish communication across the protocol layers and within each layer themselves. As a result, each byte of the payload data to be sent or received using CFDP is copied several times in memory at disjoint locations incurring memory I/O delay and imposing memory space requirements on the C&DH computer. Adding more latency to the CFDP processing, the concurrently executed threads in both of the multi-threaded reference implementations never get a chance to work on a CFDP protocol data unit (PDU) until completion due to the operating system's scheduling constraints. Hence, the cost of thread context switching adds to the CFDP processing latency in software.

TRIGA Architecture

Many of the thread-level latencies and data copies can be eliminated by performing the CFDP protocol stack functions using pipelined hardware modules that take advantage of the inherently parallel and independent nature of protocol stack processing. In TRIGA, the on-chip PowerPC 405 processor performs the transport layer functionalities of CFDP such as initiating, finalizing and keeping track of the CFDP transactions while packetizing CFDP protocol data units, Space Packets and TM/TC frames are left for the hardware modules (Fig. 1). Both inbound and outbound data paths operate separately to reflect the asymmetric nature of deep space communication where outbound traffic far exceeds the inbound traffic to the spacecraft. Each protocol layer on the 32-bit wide outbound data path follows a general structure where the layer's multiplexer finite state machine controls the behavior of the header, payload and trailer generators to fill its hardware FIFO for the lower layer's payload module (Fig. 2). On the 8-bit wide inbound data path, the De-framing module passes valid TM/TC

Frame data on to the Space Packet layer for further processing after examining and removing TM/TC header and trailer fields. The Space Packet layer and CFDP Protocol data unit follows the same parsing strategy as the De-framing layer does. When the CFDP PDU decoding layer detects CFDP control packets such as end-of-file, retransmission requests and acknowledgement messages, it sends an interrupt to the PowerPC processor for updating CFDP transaction status. The PowerPC then initiates necessary action to either the outbound File Data Unit layer or Protocol Data Unit layer on the outbound side to respond to the control message previously received. These protocol processing procedures are performed using on-chip block ram and hardware FIFOs without the need to access external memory. As a result, we maintain a zero-copy send and receive architecture where direct a pipeline exists from the data storage to the physical communication interface.

Discussion and Results

To explore the speedup and power consumption of TRIGA and compare them against MRO and DI CFDP protocol stack implementations, we have to caution that the flight hardware has special design constraints such as Single Event Effects mitigation techniques that ultimately add latency, area and power consumption. In addition, the telecom throughput requirements are set to not exceed the radio transmission throughput, which is directly proportional to the very limited transmitting power and size of the spacecraft antennae. Further, metrics such as power consumption and thread latencies are almost impossible to accurately quantify for the flight implementations because the CFDP functionalities are very closely coupled with the flight systems software that performs guidance, navigation and science tasks. However, we can examine holistically on how much performance and architectural improvement TRIGA offer by looking at the number of physical modules required to perform CFDP and the respective data copies each approach incurs. Table 3 shows the CFDP related system performance for both DI and MRO. Aside from requiring a dedicated hardware module, these software dominant implementations require interconnecting busses and external memory for intermediate data product storage. TRIGA's high throughput CFDP processing can accomplish these tasks with much less power and several order of magnitude improvement in throughput depending on the system level constraints such as data read bandwidth and radio bandwidth.

Using the post place and route FPGA data, we obtained the peak outbound throughput of 3.3Gbits/s and inbound throughput of 850Mbits/s at 106 MHz clock frequency. TRIGA hardware modules consume close to 0.87 mWatts per megahertz with 850 mWatts contributing to static power consumption. (See Fig. 3) Since PowerPC Processor's only duty is to service the interrupts and initiate transactions, its frequency can run as low as a few megahertz. With these performance metrics, TRIGA pave the road to the ubiquitous use of reconfigure protocol accelerator for NASA deep space missions in the near future.

Acknowledgment

The research and development described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology and Cal Poly, San Luis Obispo, under a contract with NASA.

Reference

[1] J. Pang, P. J. Pingree, and J. L. Torgerson, "TRIGA: Telecommunications protocol processing subsystem using reconfigurable interoperable gate array," in press for Proc. of SMC-IT 2006, Pasadena, CA, July 2006.

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Table 1: CCSDS Protocol Stack Implementations

CCSDS Protocol		CCSDS	TRIGA	Deep Impact	MRO	OSI
Uplink to S/C	Downlink from S/C					
		Flight SW	C&DH App	SW	SW	Application
CFDP	CFDP	Transport	SW Stateful			Transport
			HW PDU			
Space Packet	Space Packet	Logical Data Path	HW Packet			Network
Telecommand Space Data Link	Telemetry Space Data Link	Link Sublayer	HW TM/TC			Data Link
Telecommand Synchronization and Channel Coding	Telemetry Synchronization and Channel Coding	Channel Coding Sublayer		Hardware		
					CRC in HW	
R-S /LDPC/Turbo	R-S /LDPC/Turbo	R-S /LDPC/Turbo	N/A	R-S /LDPC/Turbo	R-S /LDPC/Turbo	Physical
RF	RF	Modulation	Ethernet	RF	RF	

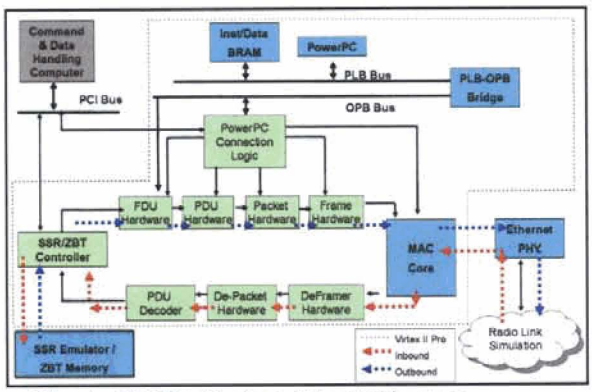

Fig. 1: TRIGA System Block Diagram

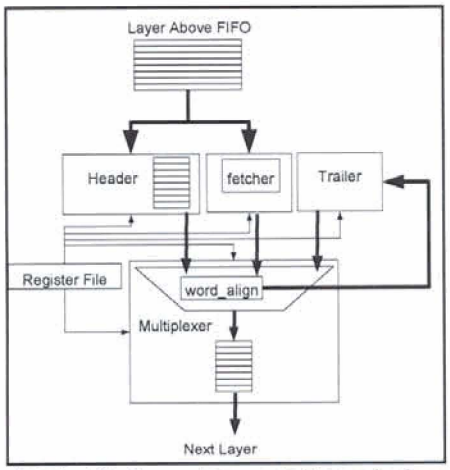

Fig. 2: The Outbound Layer's Generic Structure

Table 2: TRIGA FPGA Utilization

Component	Slices	Slice FFs	LUTS
PPC Con Logic	195	259	274
PPC Peripheral	910	861	992
C&DH I/F	576	486	746
Storage I/F	676	710	876
FDU	806	794	1472
PDU	1015	957	1869
Packet	353	284	628
Frame	1015	957	1869
Inbound	3612	4100	6035
Mac	4654	5828	6308
Total	13812	15236	21069

Table 3: Flight CFDP Stack Implementation Performance

Deep Impact		Mars Reconnaisance Orbiter	
Hardware (Power)	Function (Data Copies)	Hardware (Power)	Function (Data Copies)
Rad 750,DRAM, cPCI Cntrl (8.6 W @ 132 Mhz)	Core CFDP (1)	Rad 750,DRAM, cPCI Cntrl (8.6 W @ 132 Mhz)	Core CFDP(1)
	Packetizing (1)		Packetizing (1)
			Framing (1)
Power PCI (1.5W @ 33Mhz)	Data Transport (1)	Power PCI (1.5W @ 33Mhz)	Data Transport (1)
Telecom HW (7.5 W @ 24Mhz)	Telecom HW SDRAM(1)	Telecom HW (3.9 W @ 24Mhz)	Frame CRC (1)
17.6 W	4 copies	14 W	5 copies
Peak Throughput (20 Kbit/s)		Peak Throughput : 5.2 Mbits/s	

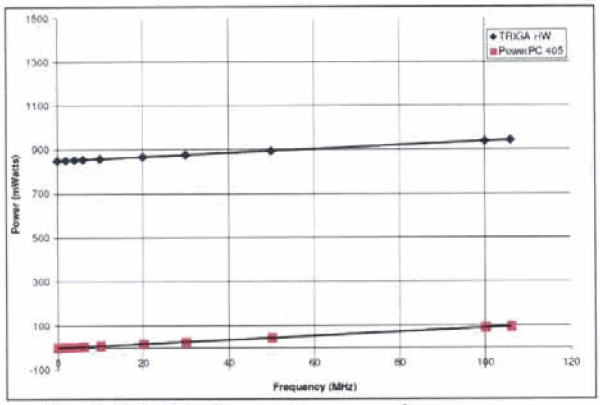

Fig. 3: TRIGA Power Consumption

Evaluation of TRIGA

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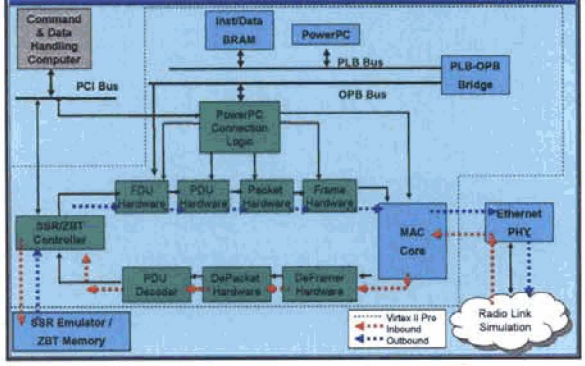
CFDP Protocol

- CCSDS File Delivery Protocol (CFDP)
  - CCSDS - Consultative Committee for Space Data Systems comprised of 30 International space agencies
- Reliable transport that tolerates high, variable round trip latency
- Reliable and Unreliable modes supported for different transfer requirements
- Connectionless Protocol
- Multiple transmissions in flight allowed

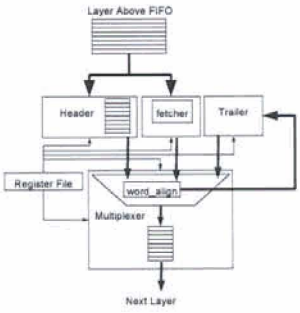
Recent Implementations - MRO

CCSDS Protocol		CCSDS	TRIGA	Deep Impact	MRO	OSI
Uplink to S/C	Downlink from S/C					
CFDP	CFDP	Flight SW Transport	CADH App SW Stateful HW PDU	SW	SW	Application Transport
Space Packet	Space Packet	Logical Data Path	HW Packet			Network
Telecommand Space Data Link	Telemetry Space Data Link	Link Sublayer	HW TM/TC			Data Link
Telecommand Synchronization and Channel Coding	Telemetry Synchronization and Channel Coding	Channel Coding Sublayer		Hardware	CRC in HW	
R-S LDPC/Turbo RF	R-S LDPC/Turbo RF	R-S LDPC/Turbo Modulation	N/A Ethernet	R-S LDPC/Turbo RF	R-S LDPC/Turbo RF	Physical

CFDP Protocol



Generic Outboud Layer



CFDP Stack Implementations

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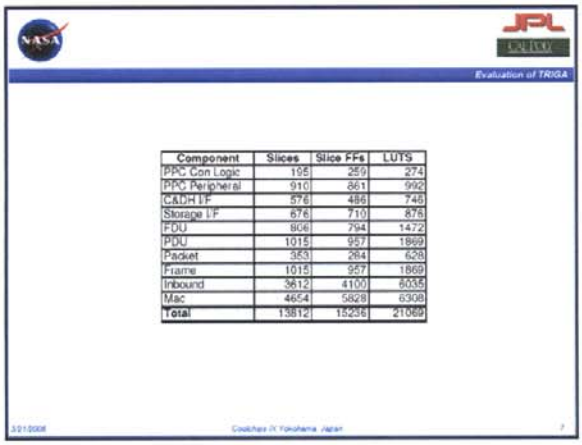

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