Terahertz (frequencies ranged from 300GHz to 3THz) imaging and spectroscopic systems have drawn increasing attention recently due to their unique capabilities in detecting and possibly analyzing concealed objects. The generation of terahertz signals is nonetheless nontrivial and traditionally accomplished by using either free-electron radiation, optical lasers, Gunn diodes or fundamental oscillation by using III-V based HBT/HEMT technology[1-3]. These prior techniques suffered major disadvantages of size, cost, complexity and sometimes even the need of cryogenic cooling[2]. CMOS has never been considered for terahertz applications due to its low cut-off frequency of $f_{\text{max}}$. The highest reported CMOS oscillation frequency to date is 192GHz through a 2$^{\text{nd}}$ order push-push method[4]. We have substantially extended the operation range of deep-scaled CMOS by using a linear superimposition method, in which we have realized a 324GHz VCO in 90nm digital CMOS with 4GHz tuning range under 1V supply voltage. This may also pave the way for ultra-high data rate wireless communications beyond that of IEEE 802.15.3c and reach data rates comparable to that of fiber optical communications, such as OC768 (40Gbps) and beyond.

Our new approach does not rely on device nonlinearities, but employs linear superimposition of multiple phase-shifted ($2\pi/N$ in sequence, where $N$ is an integer greater than one) and rectified fundamental signals ($\omega_0$) to produce a superimposed output signal at the intended frequency of $N\omega_0$.

The algorithm can be comprehended graphically in Fig.1 by taking $N=4$ as an example. Phase shifted signals of $I_p=I_0\sin(\omega_0t)$, $I_{qp}=I_0\sin(\omega_0t+\pi/2)$, $I_{im}=I_0\sin(\omega_0t+\pi)$ and $I_{qm}=I_0\sin(\omega_0t+3\pi/2)$ are generated by a quadrature VCO. These signals are then rectified and linearly superimposed to produce the final output signal of

$$I_{\text{out}} = I_a + I_b = I_0(\sin(\omega_0t) + \cos(\omega_0t)) = \frac{4}{\pi} A_1 I_0 \left(1 - \frac{2}{3 \cdot 5} \cos(4\omega_0 t) + \cdots \right) \quad (1)$$

where $A_1$ is the rectification gain. As clearly indicated in Eq.1, the superimposition has canceled the fundamental, 2$^{\text{nd}}$ and 3$^{\text{rd}}$ harmonics and leaves the 4$^{\text{th}}$ order term with a fundamental-to-4$^{\text{th}}$ Harmonic signal conversion efficiency of

$$\eta_4 = (8/(15\pi) \cdot A_1 I_0)/(I_0) = 8/(15\pi) \cdot A_1 \quad (2)$$
By setting $A_T=1$, the results in $\eta = 17\%$ or $-15.4$ dB, which is significantly higher than that of traditional harmonic generation or push-push approaches [2, 4] in order to achieve the equivalent frequency multiplication factor of four.

This new $4\omega_0$ frequency generation technique has distinct advantages of: (1) higher signal conversion efficiency and output power due to self-cancellation of the fundamental, 2$\text{nd}$ and 3$\text{rd}$ harmonics, (2) simplified external filtering requirement to lower (<4) harmonics leading to more compact circuit design and lower power consumption, (3) the $4\omega_0$ output signal may be phase-locked by a PLL at the fundamental frequency $\omega_0$ for achieving faster settling time and broader locking range.

The circuit schematic shown in Fig.2 explains the proposed linear superimposition algorithm. The fundamental oscillation frequency is chosen as $f_0=81$ GHz, which is about half of the NMOS $f_{\text{max}}$ (160 GHz) for sufficient $g_m$ to commence the oscillation. The quadrature VCO, consisting of cross-coupled twin VCO cores, generates quadrature phases of fundamental signals at frequency $\omega_0$: $V_{Ip}(0^\circ)$, $V_{Im}(180^\circ)$, $V_{Op}(90^\circ)$ and $V_{Om}(270^\circ)$. These signals are then converted into corresponding output currents of $I_{Ip}$, $I_{Im}$, $I_{Op}$ and $I_{Om}$, respectively, via the transconductance stage which also rectifies the output current signals. The four rectified currents are subsequently superimposed to deliver the output signal at the desired frequency of $4\omega_0$ via an inductive load of $Z_L$.

Each VCO core consists of a cross-coupled NMOS pair ($M_1$ to $M_4$) of $W/L=2.4$ $\mu$m/90nm with a differential inductor load of $L=0.3$ nH. These cores are twist-coupled by $M_5$ to $M_8$ with $W/L=2$ $\mu$m/90nm to complete the quadrature VCO. Devices $M_9$ to $M_{12}$ with $W/L=10$ $\mu$m/90nm are used to form transconductance stages with a common output load of $Z_L=0.2$ nH. The transconductance stages rectify input quadrature signals and produce the output signal at $4\omega_0$.

The VCO performance is characterized by JPL with the test setup illustrated in Fig. 3. The DUT output is probed on-wafer using a custom-designed GSG WR3 waveguide probe with a cutoff frequency of 173 GHz, which ensures no signal will pass below the cutoff frequency into the mixer. The oscillator signal is fed into a sub-harmonic mixer (SHM) pumped with an LO signal of 160 GHz. The LO is generated from a synthesizer set at 20 GHz followed by a frequency quadrupler and doubler. Two W-Band PA modules and one variable attenuator are inserted between the quadrupler and doubler to boost the 80 GHz tone while suppressing high-order harmonics. Under various bias conditions ($V_{DD}=1$~1.2V, $I_{DC}=12$~16mA), the output frequencies of more than ten VCOs vary between 319 GHz to 325 GHz.
Figure 4 shows a representative test data of the output frequency and power. The measured output power with a 50Ω load is about -76dBm before calibration. With the test setup loss of about 30dB, the calibrated output power at 324GHz is estimated as -46dBm. Additionally, a -26dBm output power at 81GHz is measured from a separate fundamental-signal-only VCO on the same wafer. Considering the 15.4dB signal conversion loss given by $\eta$ of Eq. 2, this yields $4\omega_0$ output power of -41.4dBm at the 324GHz. The minor output power discrepancy from two methods, -46dBm versus -41.4dBm, may be caused by variations of loss between different test setups and equipment. Figure 5 illustrates measured VCO tuning range of 4GHz by varying the control voltage between 0~2V across the varactor of $C_{var}$. The rejection of lower-order harmonics is also confirmed by measuring the fundamental tone at the output node. No fundamental tone is observed above the -80dBm noise floor. The high fundamental tone rejection at the output node (>39dB) is attributed to the linear superimposition algorithm and the designated inductive loading at $4\omega_0$. The 2$^{nd}$ and 3$^{rd}$ harmonics are beyond the range of our 110GHz spectrum analyzer but should have even lower output power than that of the fundamental tone. Due to the lack of equipment capable of measuring the phase noise directly at 324GHz, we estimate its phase noise level of -78dBc/Hz at 1MHz frequency offset by adding -20Log(4)dB (i.e.-12dB) to the measured phase noise of -90dBc/Hz of the fundamental signal from a separate fundamental-signal-only VCO. Table 1 summarizes the 324GHz CMOS VCO performance and Figure 6 shows the die photo.

In conclusion, a linear superimposition technique is devised to generate terahertz (324GHz) output signal of -46dBm in 90nm CMOS with a fundamental-to-4$^{th}$ Harmonic signal conversion efficiency of 17% or -15.4dB. The associated phase noise is estimated as -78dBc/Hz and -91dBc/Hz at 1 MHz and 10MHz offset, respectively. The fundamental tone is rejected at the output node by at least 39dB without additional filtering. The circuit draws 12mA from 1V supply and occupies a core area of $210 \times 180 \mu m^2$. The frequency tuning range is measured as 4GHz with output power variation less than 5dB.

References


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Fig. 1 Linear superimposition of phase shifted fundamental signals to generate $4\omega_0$ output signal
Fig. 2 324GHz ($4\omega_0$) VCO implementation based on linear superimposition method

Fig. 3 324GHz test setup at JPL
Sub-harmonic mixing frequency is \( (f_{\text{vco}} \cdot 2^2 f_{\text{lo}}) = f_r \), or \( f_{\text{vco}} \cdot 2^2 (20^2 \cdot 2^2) = 3.5 \) GHz, yielding \( f_{\text{vco}} = 323.5 \) GHz.

Fig. 4 Measured \( 4\omega_0 \) or 324GHz output signal at a pre-calibrated -76dBm or post-calibrated -46dBm output power.
Fig. 5 Measured VCO frequency tuning range
### Table 1 324GHz CMOS VCO Performance Summary

<table>
<thead>
<tr>
<th>Functions</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Frequency</td>
<td>324GHz</td>
</tr>
<tr>
<td>Frequency Multiplication Factor</td>
<td>4X</td>
</tr>
<tr>
<td>Calibrated Output Power</td>
<td>-46dBm</td>
</tr>
<tr>
<td>Maximum Fundamental-to-4th Harmonic signal Conversion Efficiency</td>
<td>17% or -15.4dB</td>
</tr>
<tr>
<td>Measured Rejection of Fundamental signal</td>
<td>&gt;39dB</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>4GHz</td>
</tr>
</tbody>
</table>
| Estimated Phase Noise based on Measured Phase Noise at Fundamental | -78dBc/Hz at 1MHz offset  
-86dBc/Hz at 5MHz offset  
-91dBc/Hz at 10MHz offset |
| Supply Voltage                                      | 1V                                               |
| Current Consumption                                 | 12mA                                             |
| Chip Core Area                                      | 210x180μm²                                      |
Fig. 6 Die photo