

SINGLE-EVENT EFFECTS IN HIGHLY SCALED DEVICES FOR SPACE APPLICATIONS

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Abstract

This paper discusses single-event upset (SEU) in memories and microprocessors that are the “drivers” of highly scaled commercial integrated circuits. Despite the decrease in critical charge that occurs for highly scaled CMOS devices, recent test data has shown that SEU rates are actually somewhat lower for scaled devices compared to older devices with larger feature size. Hard errors, which are increasingly important for memories, are discussed along with conventional soft errors. Functional errors in memories and microprocessors are particularly significant, and tend to dominate the response of highly scaled devices from an application standpoint. Predictions for future devices are made using the Semiconductor Industry Roadmap along with recent modeling and radiation test results.

1. Introduction

Single-event upset of microelectronics in space was first reported by Binder, *et al.*, in 1975 [1]. Improvements in semiconductor technology in the ensuing 29 years have resulted in mainstream devices with feature size as small as 0.09 μm , and more than 10^8 transistors per chip. Along with these increases in density and performance, there has been increasing concern about single-event upset in terrestrial applications (from alpha particles and neutrons) that now impact the design of most commercial microelectronics.

The first scaling predictions for single-event upset in space were done by Petersen, *et al.* in 1982 [2]. They predicted that the critical charge would decrease as the square of the feature size, resulting in an extrapolated critical charge of 0.18 fC for a feature size of 0.09 μm . However, the semiconductor industry has been forced to deal with upset from neutrons, produced by cosmic rays in the upper atmosphere, that are present in significant numbers at the earth’s surface. Their concern with this problem causes the critical charge to reach a “plateau” of $\sim 1\text{-}2$ fC, nearly an order of magnitude greater than the extrapolated results from the Petersen relationship. This provides a “floor” for SEU sensitivity of commercial devices that corresponds to an LET of approximately $1.5\text{--}2$ MeV-cm²/mg.

This paper discusses the effects of device scaling on SEU sensitivity for commercial CMOS circuits. Although total dose damage is an issue for space applications, charge trapping is so small in the thin gate oxides used in highly scaled devices that gate threshold shifts are no longer of much concern. Total dose effects in trench isolation structures are potentially important, but tests of advanced microprocessors have shown negligible degradation at levels below 100 krad(Si). For these reasons, total dose effects have not been included in this paper.

2. Scaling Relationships

2.1. General Issues for Conventional CMOS

Device scaling for CMOS is a complex problem, which requires tradeoff of many different parameters [3-5]. Initial scaling predictions were done with constant voltage [6]. Later work reduced power supply voltage, using the concept of constant field scaling where the electric field in the channel region is held constant [4,5]. Doping levels, channel length and oxide thickness are allowed to change with the scaling factor. Constant-field scaling assumes that all key device parameters are scalable. It is oversimplified for power supply voltage (V_{DD}) below two volts because threshold voltage and subthreshold slope, which do not scale, become a significant fraction of V_{DD} .

A different approach was developed in the last ten years where the electric field in the channel region and the field across the gate oxide are allowed to increase [7]. The increased fields are essential in order to get sufficient improvement in device performance. Analysis of scaling effects is quite complex. Older scaling projections overestimated reductions in power supply voltage and threshold voltage for channel lengths below 100 nm. The latest scaling predictions use a modification of this concept, providing separate dimensional scaling parameters for channel length and a less aggressive scaling factor for width and wiring.

The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA).

Scaling is application dependent. Recent work has subdivided scaling into three basic circuit applications: (1) high-performance devices, such as microprocessors, where the main overall criterion is speed; (2) low-power devices, where speed and power dissipation are both involved in establishing design tradeoffs; and (3) memories, which require a different set of tradeoffs. The semiconductor industry has established a “roadmap” that is updated annually [3], projecting the properties of future devices in each of the above categories.

Design criteria for high-performance devices allow active cooling, and aggressive scaling of gate oxide thickness with reduced on/off current ratios. Current projections assign 10 to 20% of the total power to gate leakage, which is a major departure from previous scaling assumptions. This is impractical for space applications, and consequently less aggressive scaling scenarios should be followed when considering high-performance devices in space.

Low power devices require thicker gate oxides to reduce gate leakage. Initial work for low-power scaling used lower power supply voltage compared to high-performance scaling, but recent projections use nearly the same voltages for both scenarios. This is due to the need for high on/off ratios for low-power applications.

Memories require different tradeoffs. The on/off current ratio for memories must be about two orders of magnitude higher than for logic, requiring thicker gate oxides. Changes in device architecture and (for DRAMs) the design of the storage capacitor are key factors in memory evolution. Advanced DRAMs use trench capacitors with very high aspect ratios to minimize cell area. Leakage currents in DRAMs must be very low to meet refresh rate requirements. Variations in threshold voltage occur for several reasons, including statistical fluctuations in the number of channel dopant atoms [8]. This results in large differences in leakage current, requiring lower mean leakage currents in the DRAM array to keep leakage currents in the more extreme part of the distribution within tolerance. Measurements of retention time over the entire DRAM array provide direct evidence of this effect [9].

2.1 Silicon-on-Insulator Technology

Silicon-on-insulator (SOI) CMOS is becoming a mainstream technology. The silicon film thickness is typically 120 – 200 nm for partially depleted SOI. This should result in far less charge collection compared to bulk/epitaxial processes where the charge collection depth is approximately 2000 nm, with a lower soft error rate as well as improved SEU hardness in space for SOI. However, in partially depleted structures excess charge collection can occur because of the parasitic bipolar transistor (unless body ties are used), largely negating the advantage of lower charge collection [10]. Commercial SOI microprocessors have been produced by two mainstream manufacturers during the last three years, and radiation test results for those devices with reduced feature size and core voltage provide real examples of scaling effects that incorporate all of the design changes necessary for scaled devices.

2.2 Device Design Anticipated for the Near Future

Older scaling scenarios assumed that the design of a fundamental MOS transistor changed very little as dimensions were reduced. However, modern MOS devices incorporate many design changes to achieve better performance. These include the use of special “halo” implants under the source and drain region to reduce the “rolloff” of threshold voltage for short channel lengths, and the use of complex retrograde doping profiles in the channel region. In highly scaled devices the doping profile is adjusted in both the lateral and transverse directions in order to confine carriers to the active region beneath the gate. Recent work by Frank, *et al.* projected an improved transistor that is intended for mainstream digital applications in the year 2008 [7]. That device is optimized for 25 nm channel lengths, with a gate oxide thickness of 1.5 nm and feature size of 50 nm. The power supply voltage is 1 V, somewhat higher than that predicted by the semiconductor roadmap.

Figure 1, from that work, shows the subthreshold characteristics of transistors with various channel lengths, with excellent performance down to 20 nm. Note that the on-to-off current ratio is nearly 10^4 , considerably higher than the value assumed in the semiconductor roadmap. Fabrication details include use of very sharp doping profiles in the lateral and transverse directions of the channel region. This structure is probably more representative of mainstream digital device technologies than predictions from the SIA roadmap. The total device area is on the order of $0.01 \mu\text{m}^2$, considerably smaller than the effective diameter of the charge from a heavy-ion strike. This has a major impact on charge collection from energetic charged particles.

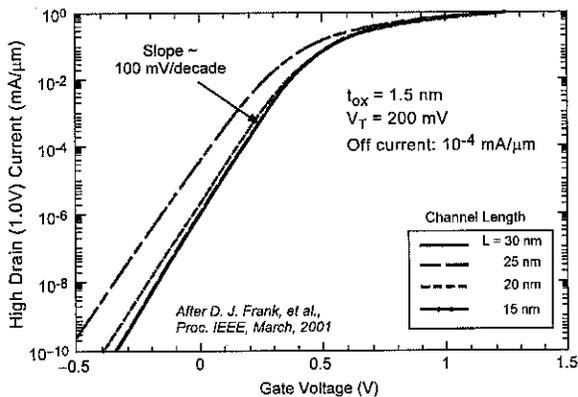
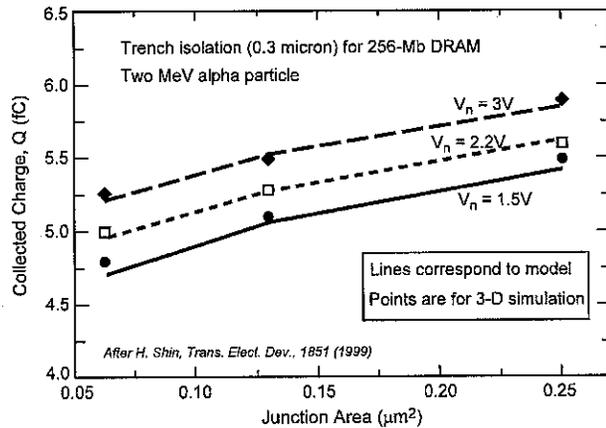


Figure 1. I-V characteristics of an advanced CMOS device with channel lengths of 25 nm [7].

3. Charge Collection in Small-Area Structures

Charge generated from a heavy ion is usually assumed to be proportional to linear energy transfer (LET), and to effectively create a dense line of charge within the structure [11-13]. This concept has worked well for older devices, but will likely require modification when the device area becomes smaller than the ionization track diameter. Much of the charge collection work in the device community has been done using the track diameter and charge density of 5-MeV alpha particles ($\approx 0.1 \mu\text{m}$). Fig. 2, after Shin [14], shows how charge collected from an alpha particle strike was affected by the location of the ion strike within an MOS transistor with different junction area, as well as power supply voltage.



The charge collected from the alpha particle strike is about 25% lower as junction area is reduced, along with slight reductions due to the decreased power supply voltage. The simulations correspond to particle strikes at the center of the drain region, where the structure is most sensitive to upset effects. It demonstrates *one* reason that upset sensitivity does not necessarily increase for highly scaled devices. The effect of small device geometry on charge collection may be even larger for energetic ions in space which have a larger track radius compared to the alpha particle strikes that have been the focus of much of the work by semiconductor manufacturers.

Figure 2. Effect of ion strike position and power supply voltage on collected charge from a 2-MeV alpha particle strike [14].

Circuit design also affects single-event upset. The critical charge depends on the switching margin, transconductance, and total capacitance, which includes the capacitance from drain to substrate, gate capacitance, and stray capacitance in the isolation region. Estimates of critical charge can be determined with the SPICE program, but more precise calculations using 2-D or 3-D analysis codes are required for accurate analysis. It also depends on other design details, such as channel width and circuit loading, as well as differences in circuit implementation that involve multiple transistors in AND, NAND or NOR configurations.

Clock rates and switching chains can also affect critical charge; a chain of gates operating near the frequency limit will result in reduced logic swing as the switching pulse progresses through the chain [7]. This reduces the circuit margin, making the device more sensitive to single-event upset at high frequencies.

4. Radiation Test Results

4.1 DRAMs

Despite their sensitivity to single-event upsets, DRAMs have been used during the last 15 years for solid-state recorder applications on many spacecraft. Older DRAMs had simple response modes, allowing elementary error-detection-and-correction algorithms to correct upsets at the system level. The Clementine spacecraft used an array of 4-Mb DRAMs in a 2.4-Gbit recorder, with a mean error rate of 71 ± 2 errors per day [15]. Moon mapping on this mission was 100% successful; no missing pixels occurred during the six months that the recorder was used.

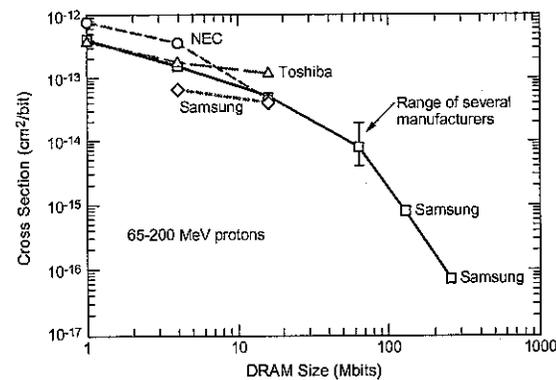


Figure 3. Cross section for proton upset as DRAMs are scaled to smaller feature size

Newer DRAMs are not so easy to use in space because they are far more complex than earlier devices. Upsets in the internal state machine or in control registers can alter the functionality of the memory, creating large numbers of errors that cannot be dealt with in a straightforward manner. Multiple-bit upset from a single ion strike can also occur, with up to *several hundred* errors from a single ion strike for ions with high LETs. However, if one ignores those complexities, the upset sensitivity of modern DRAMs on a per bit basis has actually improved as they have been scaled from the 16-Mb to the 256-Mb generation. Figure 3 compares proton upset results for various devices, normalized to the error rate per bit.

If the error rate were constant, then the cross section should decrease with the cell size. However, it is clear from this figure that there is a large change in the slope of this curve for more advanced DRAMs. The reason for this is changes in the way that the storage capacitor is designed in more advanced DRAMs. Trench capacitors with very large aspect ratios are used, reducing charge collected in the capacitor compared to earlier DRAM technologies.

Another important issue for advanced DRAMs is stuck bits. There are several possible mechanisms, but it is usually assumed that stuck bits are due to localized ionization damage (microdose) caused by the ion, which affects only a single device [16]. Microdose damage causes a shift in threshold voltage, increasing leakage current.

For DRAMs the leakage current must remain very low in order to avoid refresh errors, particularly at moderately high temperatures (50 – 70 °C) which is the typical operating temperature range for DRAM arrays.

Figure 4 shows how the cross section for single-event upset and hard errors depends on linear energy transfer for a 64-Mb SDRAM. The ratio is only about 10,000 to 1, so the relative number of hard errors is small. However, this can affect EDAC in typical space applications because the stuck bits gradually build up during an extended space mission. Not all DRAMs show such large cross sections for hard errors, but the sensitivity of DRAMs to hard errors has steadily increased with scaling.

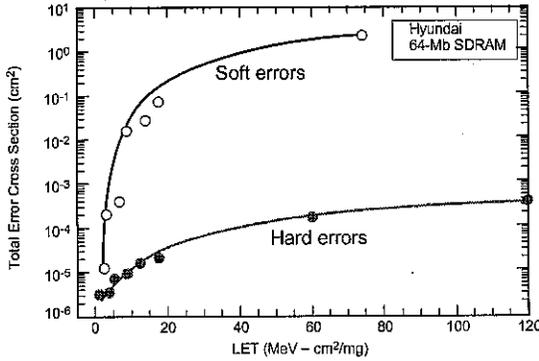


Figure 4. Upset and hard error cross section dependence on LET for an advanced DRAM.

4.2 Microprocessors

Fabrication techniques for microprocessors have advanced more rapidly than for other mainstream semiconductor devices because of the need for extremely high speed in processor applications. Thus, SEU effects in processors provide a good measure of how device scaling affects state-of-the-art devices.

Software can be designed to test device operation at various levels. For example, register-intensive tests can be used that continually evaluate internal registers to isolate SEU effects in various regions of the device. The cache section of modern processors can also be evaluated separately using software techniques. These methods, along

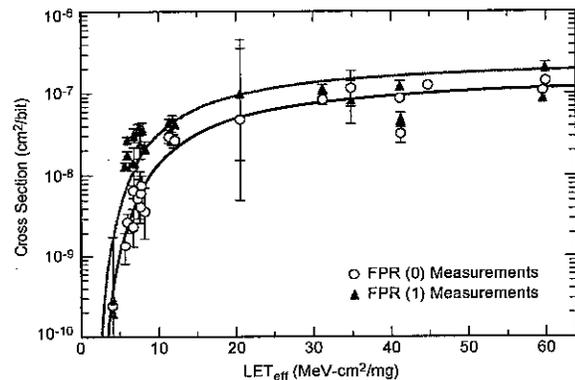


Figure 5. Upset cross section for floating-point registers in the Motorola Power PC750 microprocessor [17].

with tests at different clock frequencies to determine the effects of internal transients on upset rates, allow basic comparisons to be made in the SEU sensitivity of different types of processors, although they do not answer the more practical question of how many upsets will actually occur in a real software application. Figure 5 shows an example of register-level tests for floating-point registers in a Power PC750 microprocessor [17]. In this case there is a significant difference in the cross section for “1 to 0” compared to “0 to 1” transitions. Note that the threshold LET for upsets in the processor is about the same as that of the DRAM in Figure 5, even though the internal design and scaling rules for the microprocessor are quite different.

Although the threshold LET for upset in these processors is very low, the number of upsets that will occur in a high-inclination earth is not that high. Correctable errors will occur roughly once every 24 hours, and uncorrectable errors or “crashes” are predicted every few weeks. (Note however, that the number of correctable errors depends on the specific software that the processor is running). These error rates are low enough to consider these unhardened devices in applications that can tolerate occasional operational malfunctions.

The extreme SEU sensitivity that has often been predicted for highly scaled devices has not developed in practice, as can be seen in the earlier results of Figure 3 for DRAMs. Scaling trends for microprocessors also show some reduction in single-event upset sensitivity. Figure 6 compares upset results for three different generations of Power PC microprocessors [18]. The tests were done at maximum frequency, which increased as devices evolved. First note that the LET threshold is essentially the same for all three generations. The improvement in SEU performance

is essentially due to the decrease in saturation cross section. The upset cross section of the Power PC750 with a feature size of 0.29 μm is slightly greater than the cross section of the G4, with a feature size of 0.2 μm . The core voltage for the two processors are 2.5 and 1.8 V, respectively.

Results for advanced SOI version of the processor are somewhat different. The SOI device has a feature size of 0.18 μm and core voltage of 1.6 V. The cross section is about an order of magnitude lower than that of the bulk processors, which is expected because the SOI structure has smaller area, and cannot collect charge from the substrate. However, the threshold LET is nearly the same as that of the bulk devices, which is inconsistent with earlier scaling projections for SOI devices. This is almost certainly due to excess charge collection because of the parasitic bipolar transistor within the compact SOI MOSFET (the processor is fabricated with partially depleted technology, with a film thickness of about 0.2 μm). Similar results were obtained for a PowerPC processor that was manufactured by IBM on their SOI process, but used a lower core voltage with a feature size of 0.13 μm . Thus, this SOI result appears to be consistent between two manufacturers.

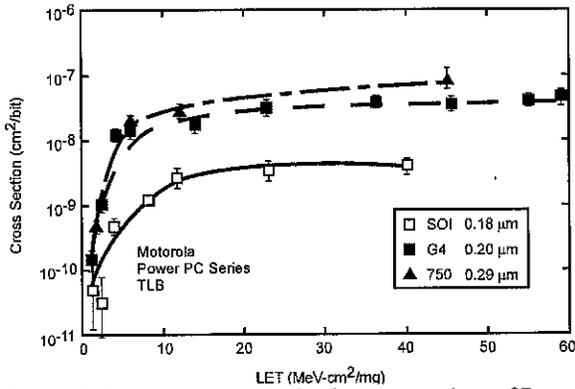


Figure 6. Register error rates for three generations of Power PC microprocessors from Motorola.

5. Discussion

Thus far the LET threshold is essentially unaffected by scaling. Therefore it is possible to examine scaling in microprocessors by means of the saturation cross section. This is shown for several different generations of

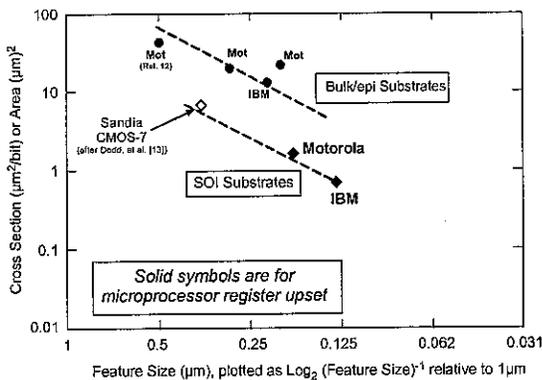


Fig. 7. Saturation cross section for several generations of microprocessors.

microprocessors in Fig. 7. The cross section scales with feature size for both bulk and SOI processors, but the line corresponding to SOI technology is about an order of magnitude lower (these are all partially depleted technology without body ties). The cross section has decreased by more than an order of magnitude for succeeding generations, decreasing the cross section per bit. Although this does not take changes in cache size or architecture into account, it demonstrates that at least to the 0.13 μm node scaling actually improves SEU hardness. The core voltage has decreased from 2.5V for older generations to 1.3 V for the 0.13 μm node, but the SEU results still improve. This trend may eventually reverse, but thus far it appears that the decrease in internal noise margin has little effect on SEU sensitivity.

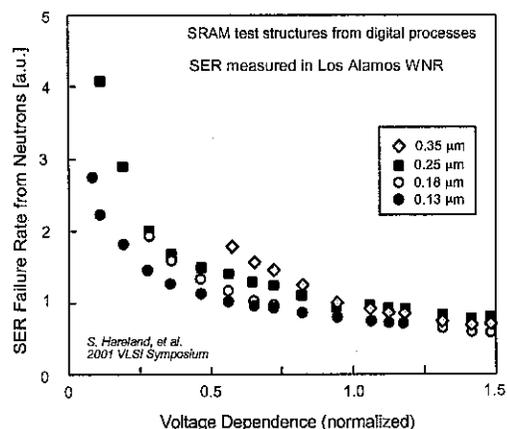
Another concern is clock frequency, which has increased several orders of magnitude with scaling. Only a limited amount of work has been done on frequency effects, partly because of the difficulty of doing tests at very high frequencies and dealing with the high power dissipation problem during radiation tests. However, recent results for PowerPC processors (SOI technology) show an increase of only a factor of two between tests done at a clock frequency of 1-GHz and tests with lower clock frequencies [19]. These results suggest that clock frequency effects are still relatively unimportant.

SOI technology is becoming the dominant technology for processors. Charge collection in SOI transistors is very complicated, and is heavily influenced by specific processing techniques. Body ties are rarely used by commercial manufacturers because of the area penalty. However, other techniques such as special ion implant steps have been investigated to reduce bipolar gain without affecting area [20]. If such techniques are implemented, they could increase the threshold LET, significantly improving the SEU response of commercial devices in space.

In addition to alpha particle upset effects, semiconductor manufacturers are also concerned with upsets from neutrons at ground level. Another example of the concern of mainstream manufacturers about neutron soft errors is shown in Fig. 8, after a paper by a group from Intel Corporation [21]. The data was obtained at the Los Alamos WNR neutron source on 16-Mb SRAMs that are used as test vehicles to evaluate basic performance of different generations of microprocessors. The paper also discusses SOI processes, but the data in the figure is for bulk

CMOS. Their results are normalized to various target power supply voltages, which change with scaling. They predict a slight improvement in soft error rate with scaling, in general agreement with the results obtained by JPL for heavy-ion tests of the PowerPC microprocessor family with similar feature sizes.

This paper has discussed some basic concepts and recent trends for single-event upset in highly scaled devices.



Most of the results were obtained during the last two years, some from specific radiation tests and others from modeling studies. The results show that the radiation susceptibility has actually improved somewhat for device generations that have advanced to the 0.13 μm level, which contradicts earlier predictions. This trend is encouraging, but it may not necessarily continue for devices that are scaled below 0.1 μm . The cross section of partially depleted SOI technologies is substantially lower than for bulk technologies, but the threshold LET is nearly the same. If *fully* depleted SOI circuits become available, there may be significant improvement in threshold LET as well as in cross section that will be a major advantage for space applications. However, fully depleted devices will likely be produced on processes with even lower voltages and critical charge, making it difficult to predict the net effect on SEU.

Fig. 8. Normalized neutron soft error rate for several technology generations, using SRAM test structures. Data were taken at the Los Alamos WNR facility.

Bulk devices will continue to be scaled to smaller dimensions as well. Fundamental considerations of switching energy and noise margin suggest that sudden changes in SEU sensitivity are unlikely, and that the relatively flat dependence of SEU sensitivity on scaling is likely to continue. However, circuit architecture and functional errors will likely become more important as devices are scaled to even smaller dimensions which may increase the difficulty of coping with single-event upsets in space, even if the event rate changes only slightly.

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