

Initial Single Event Effects Testing of the Xilinx Virtex-4 Field Programmable Gate Array

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Abstract

We present initial results for the thin-epitaxial Xilinx Virtex-4 FPGA, and compare to previous results obtained for the Virtex-II and Virtex-II Pro. The data presented was acquired through a consortium based effort with the common goal of providing the space community with data and mitigation methods for the use of Xilinx FPGAs in space.

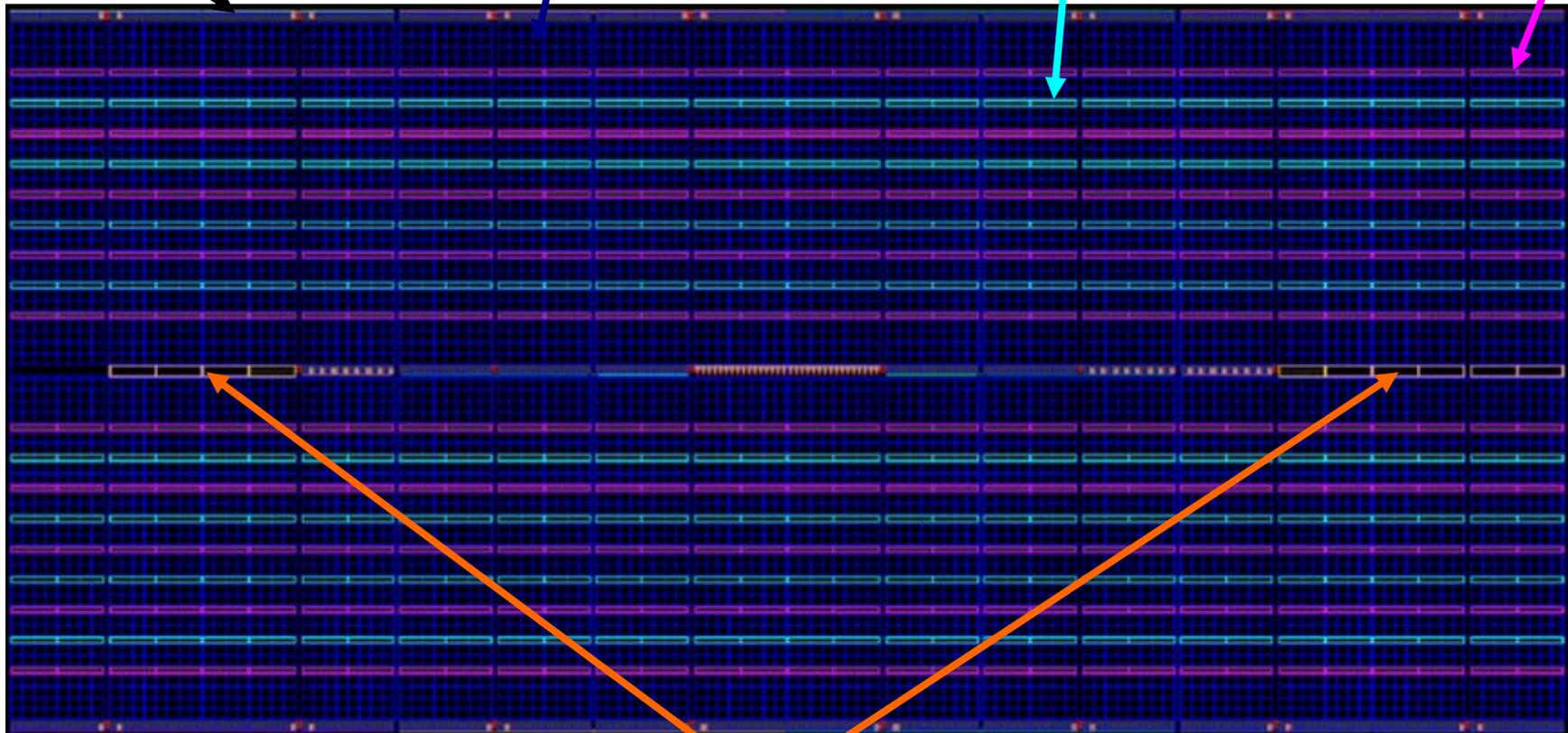
Virtex-4 SX55 Features

Input/Output Blocks

Configuration Logic
Blocks

DSP Blocks

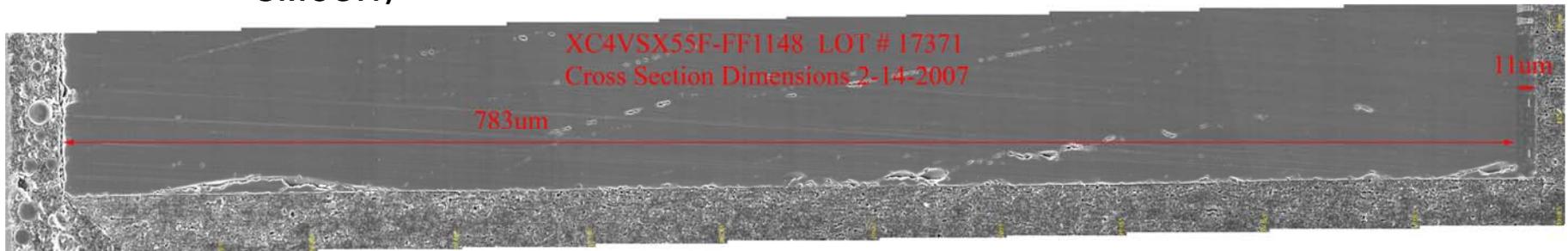
Block RAM



Digital Clock Managers

Device Summary

- XQR4VSX55-FF1148
 - 90nm CMOS Process
 - Flip Chip Geometry
 - Requires Device Thinning (From 780 microns to ~100 microns silicon)



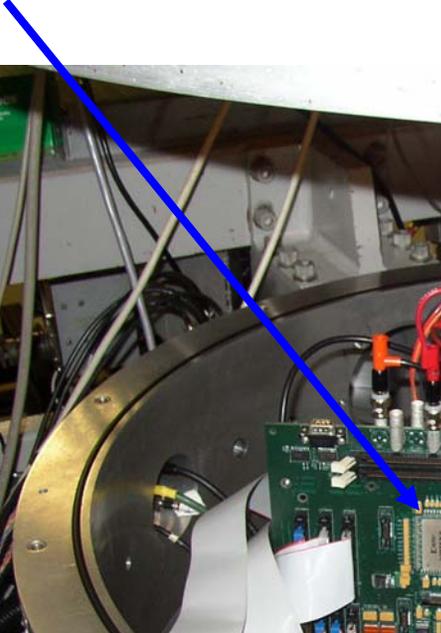
- Thin Epitaxial Substrate Layer (2 microns)

Test Objectives

- Complete Full Static Characterization (Static Cross Section as a function of LET)
 - Single Event Functional Interrupt (SEFI)
 - Latchup (High Temperature and LET)
 - Configuration Logic Blocks (CLBs)
 - Block RAM (BRAM)
 - User Flip-Flops
 - Half-Latches (Weak Keeper Circuits)

Test Setup

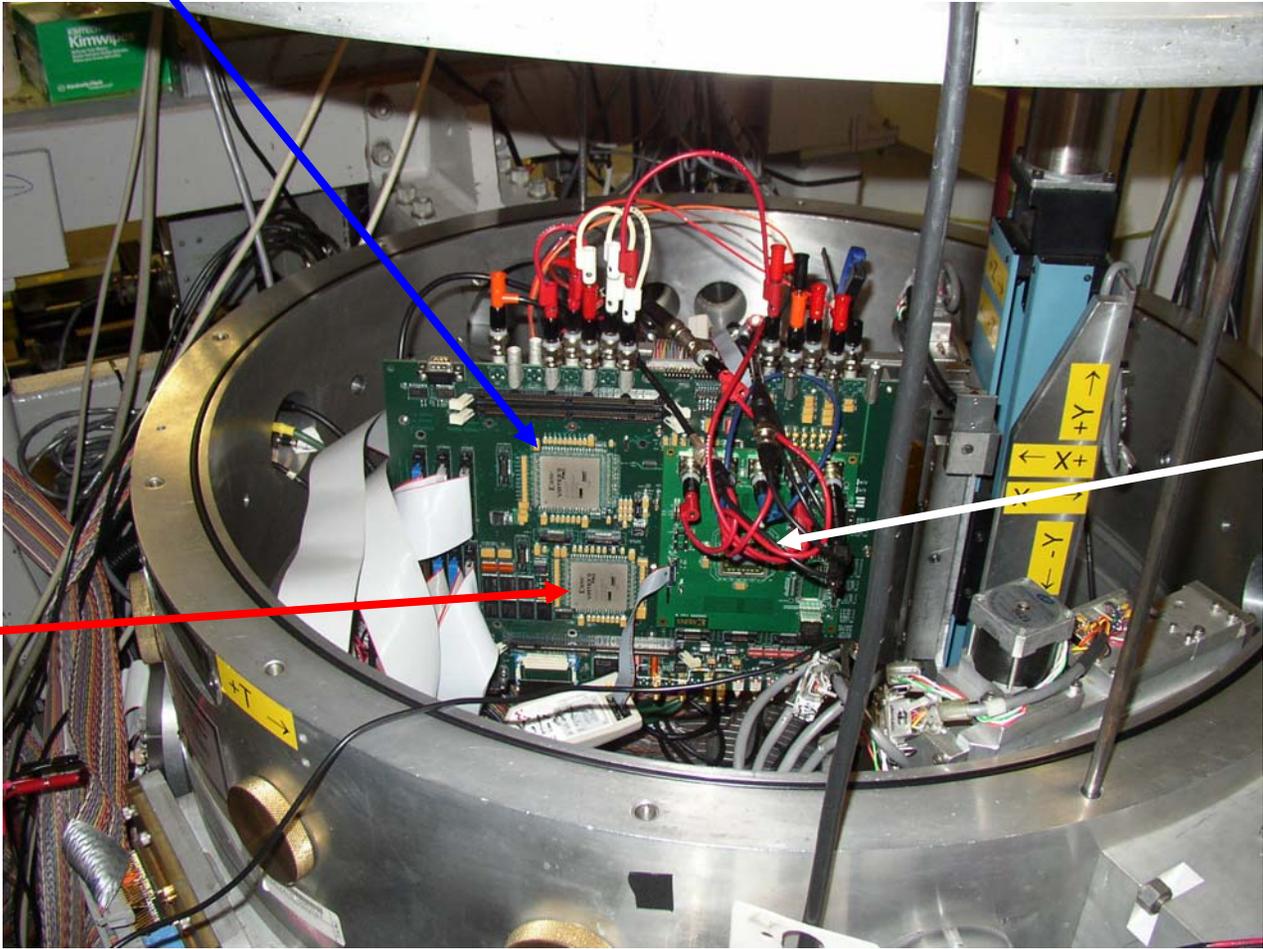
Functional Monitor



Configuration Manager



DUT Daughter Card

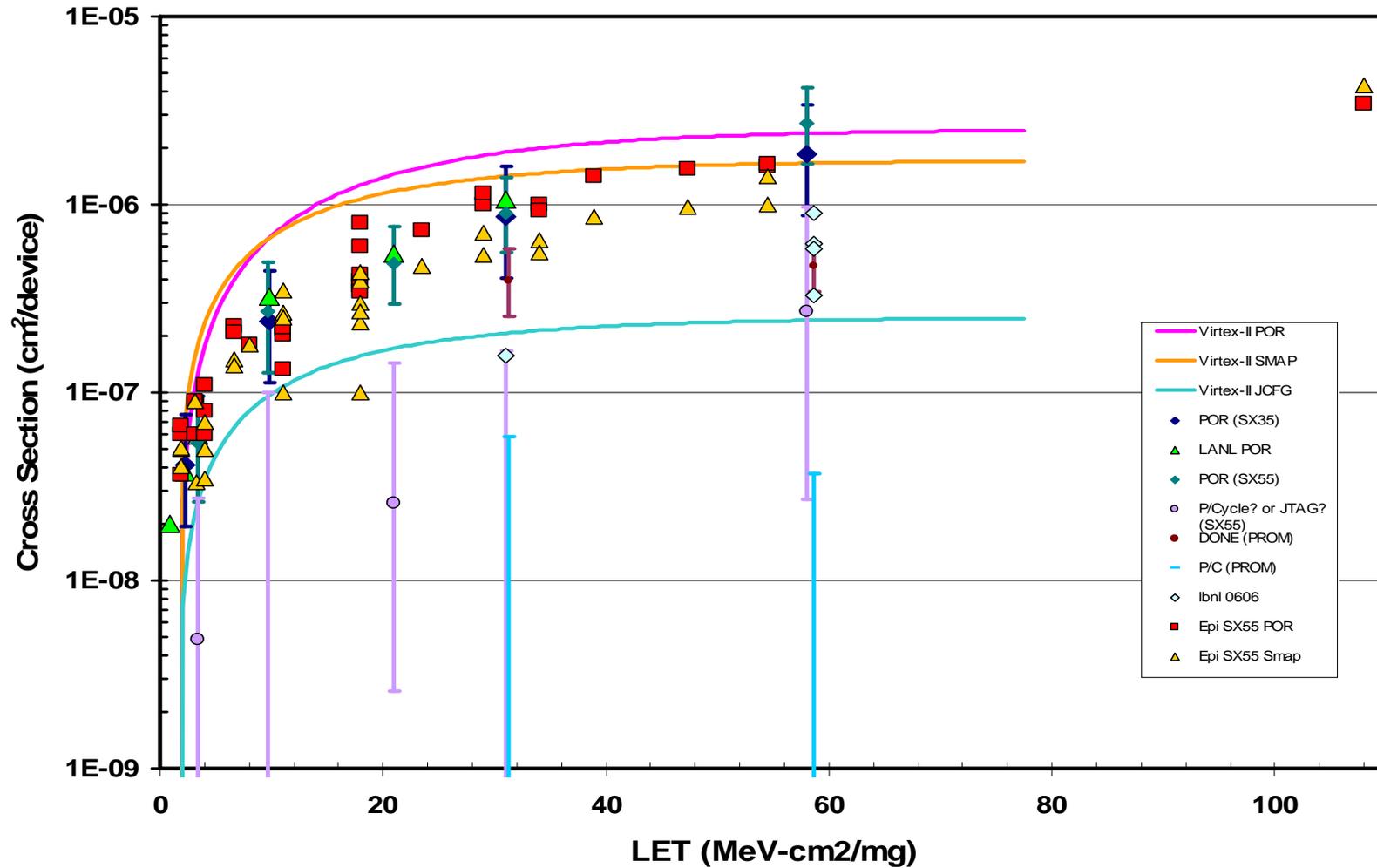


SEFI Test Design and Methodology

- DUT design is nearly irrelevant
 - Usually a functional design that requires a lot of flux
 - Low cross section, therefore requiring high amounts of fluence for good statistics
 - Lesson Learned: Keep extra close track of total dose when collecting SEFI data.

SEFI Results

Virtex-4 POR SEFI Cross Section

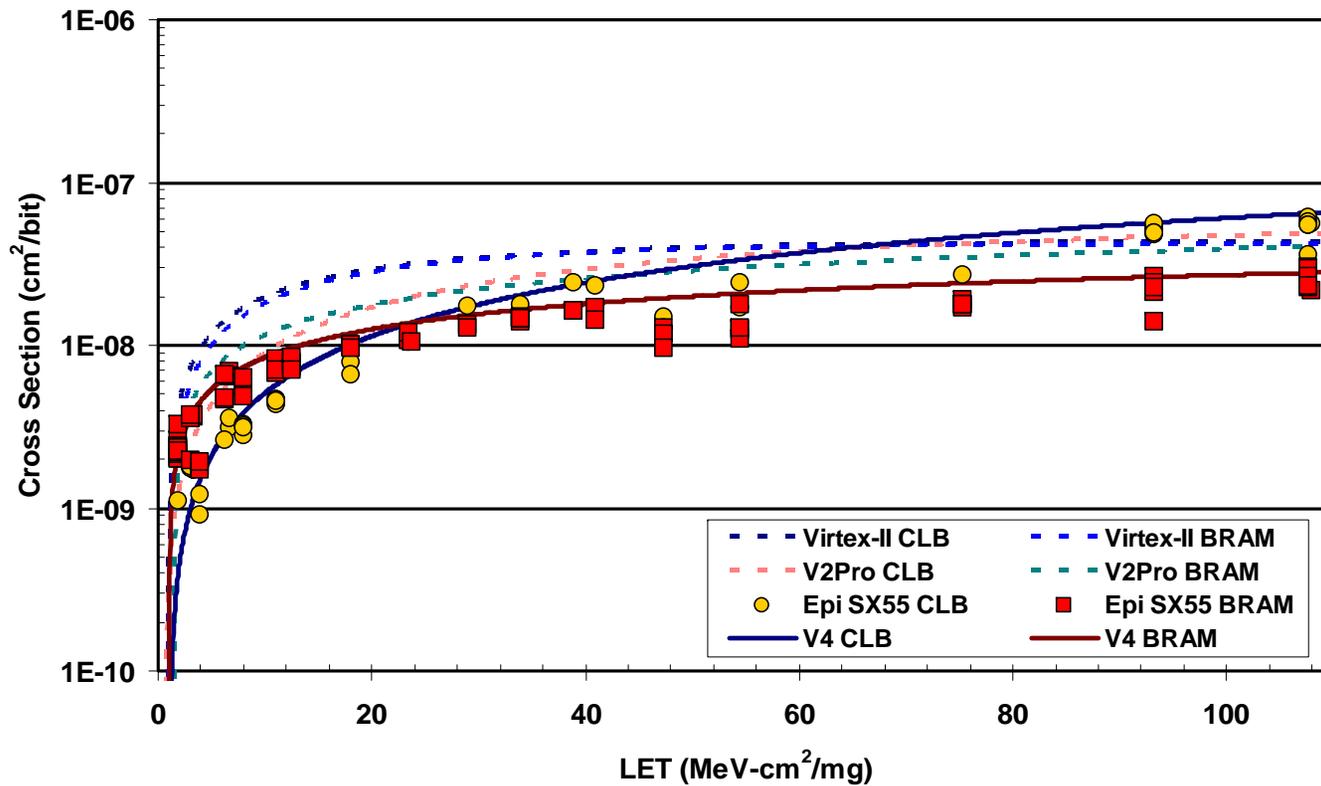


CLB and BRAM Design and Methodology

- Three Methodologies:
 - Low flux, low fluence with a iMACT device readback after irradiation
 - Low flux, low fluence with a configuration readback after irradiation
 - Low flux, low fluence with readback and scrubbing during
- BRAMs tested with fill patterns of both '0' and '1'

CLB and BRAM Results

Xilinx Virtex-4 Heavy Ion SEU Cross Section -- by block

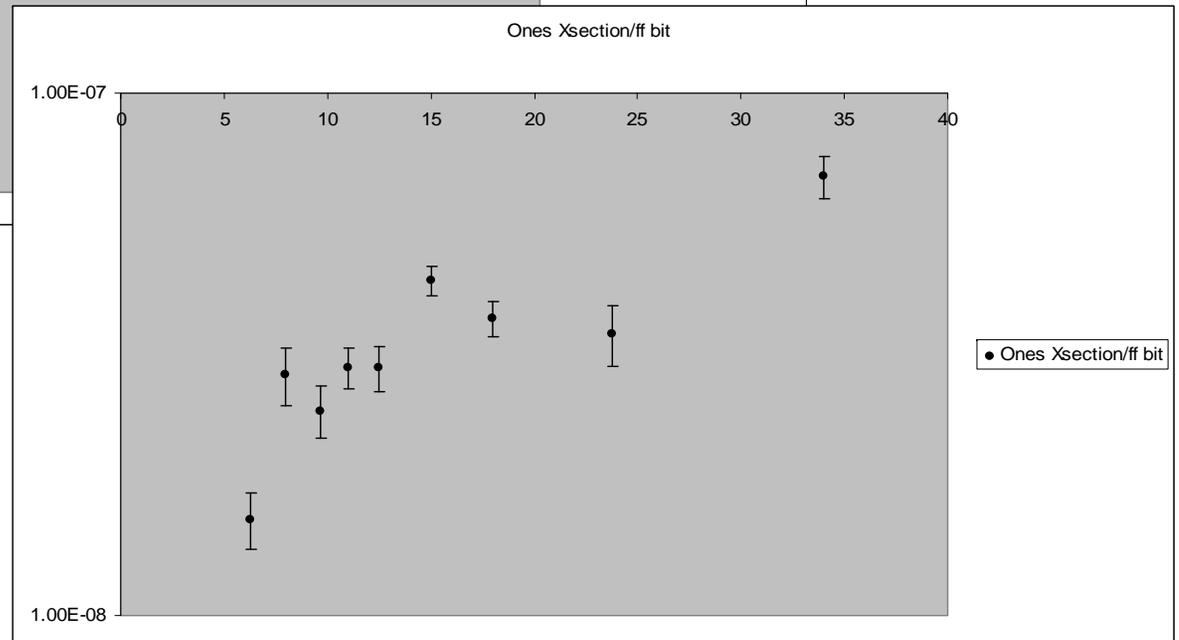
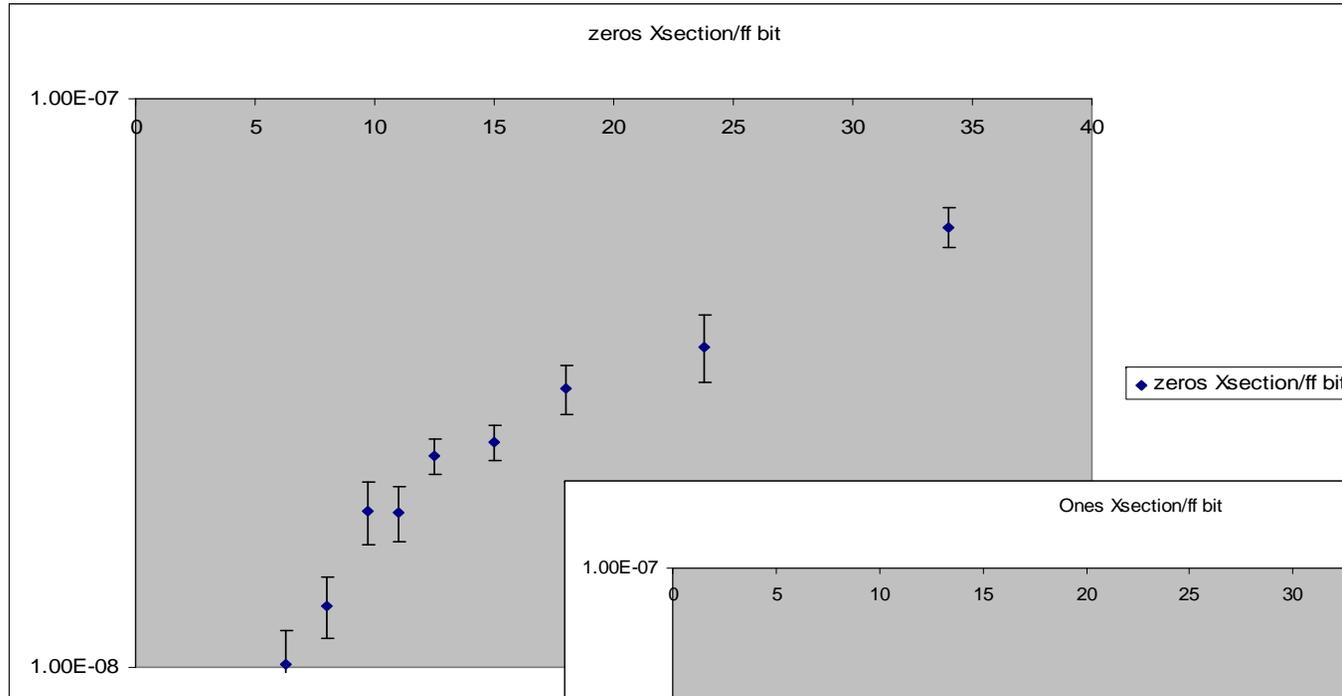


*Error bars are less than the size of the data points

User Flip-Flop Design and Methodology

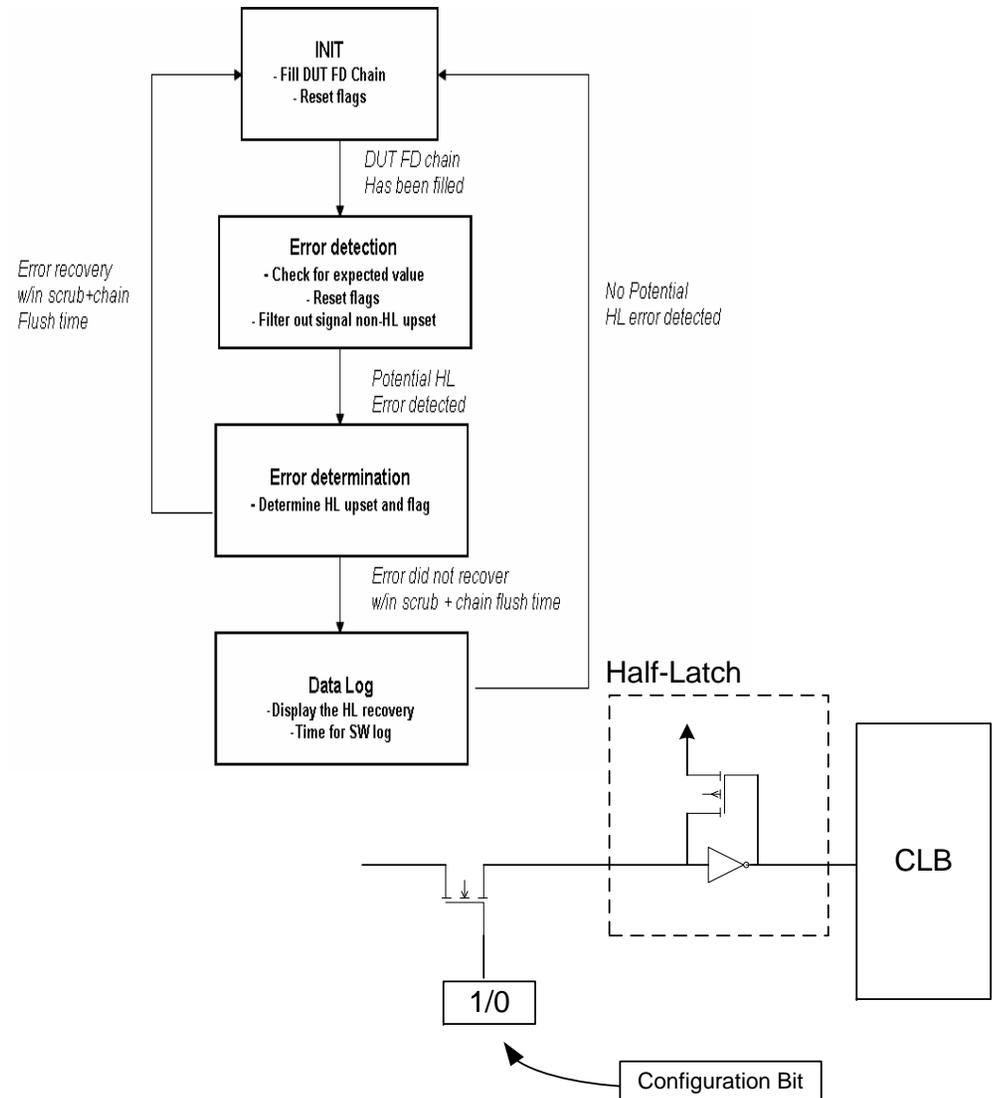
- 33 shift register chains of 1024 flip-flops each were implemented in the DUT
 - The user could select the pattern to be shifted in ('0', '1', or checkerboard)
- Device was irradiated statically at low fluxes
- Errors were clocked out and counted after irradiation

User Flip-Flop Results



Half-Latch Design and Methodology

- Design consists of 32 independent long shift register chains that utilize as much of the device's Flip-Flops as possible.
- Each FD has at least 2 half latches at its CE (clock enable) and RST (reset) ports. The clock rate to the shift register chains is at 32 KHz.
- To detect half latch upsets, 32 independent monitoring state machines exist on a monitoring device running at 32 KHz. Each functional monitoring will provide its corresponding DUT shift register chain with input and verifying the output data.



Half-Latch Results

- History of Half-Latch testing
 - Virtex II—Very low cross-section of half latches that didn't recover
 - Virtex-II Pro—No stuck half latches, but some that took several seconds to recover
 - Virtex-4—No long recovering or stuck half latches
- Conclusion: Half-Latch upsets have improved over technology scaling

Single Event Latchup...

- Latchup was tested in vacuum up to 109 MeV per mg/cm²
- The part was heated to 120° C
- A total fluence of 1X10⁸ ions/cm² was subjected to the device
- No latchup was observed
- No high current phenomenon (as observed in the V-II Pro) was observed during latchup runs

New Phenomenon

- A high current mode was observed during SEFI testing
- Event has a very low cross-section (an order of magnitude less than SEFIs)
- Not SEL
- Several Theories:
 - Encryption Bit
 - New SEFI mode
 - Scrubbing Algorithm error

Conclusions

- Overall fabric performance has improved over last two generations
- No high current at high temperature phenomenon
- No SEL
- SEFI rates approximately the same
- New high current phenomenon, theories will be proven/disproven