Frequency Dependence of Single-Event Upset in Highly Advanced PowerPC Microprocessors

Farokh Irom, Farhad Farmanesh, Mark White and Coy K. Kouba

***Abstract*— Single-event upset effects from heavy ions were measured for Motorola silicon-on-insulator (SOI) microprocessor with 90 nm feature sizes at three frequencies of 500, 1066 and 1600 MHz. Frequency dependence of single-event upsets is discussed. The results of our studies suggest the single-event upset in registers and D-Cache tend to increase with frequency. This might have important implications for the overall single-event upset trend as technology moves toward higher frequencies.**

***Index Terms*— Cyclotron, heavy ion, microprocessor, silicon on insulator, single event effects, single event transient, single event upset.**

I. Introduction

SINGLE -event effects can be a significant problem for devices operating in space, particularly for microprocessors because of their complexity. Radiation tests are often required in order to make estimates of upset rates caused by space radiation. The test results help to determine what kinds of effects are produced and how they can be detected and overcome. Complex failure modes are also of particular interest because they potentially limit ways in which errors and malfunctions can be detected and corrected by hardware or software techniques. As devices become increasingly complex, they are more likely to exhibit complex functional errors.

In recent years there has been interest in the possible use of unhardened commercial microprocessors in space because of their superior computing performance compared to hardened processors. However, unhardened microprocessors are susceptible to upset from radiation space. More information is needed on how they respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, which are designed with lower clock frequencies and higher internal core voltage voltages than recent devices [1-6]. However the trend for commercial silicon-on-insulator (SOI) microprocessors is to reduce feature size and internal core voltage and increase the clock frequency. Commercial microprocessors with the PowerPC architecture are now available that use partially depleted SOI processes with a feature size of 90 nm, an internal core voltage as low as 1.0 V and clock frequency in the GHz range.

As the clock frequency increases, the probability that momentary glitches (single-event transient (SET)) will be captured as a valid upset in combinational logic increases with frequency because the frequency of clock edges increases. Also, as circuit speeds increase, the ability of a given transient to propagate increases. The greater ability of the glitches to propagate and their higher probability of capture by storage elements such as latches, add another concern to single-event effects (SEE) [7]. The SETs become a persistent problem as clock speed continues to increase and will be difficult to protect against, especially in commercial microprocessors where speed is dominant

Previously, we reported SEU measurements for SOI commercial PowerPC's with feature sizes of 180 and 130 nm [8, 9]. These results show an order of magnitude improvement in saturated cross section of SEU compared to results of CMOS bulk counterparts. Recently we reported SEU measurements for the Motorola SOI PowerPC, MPC7448, with feature size of 90 nm. The saturation cross section of the Motorola PowerPC 7448 is more than a factor of 5 lower than that of the older SOI PowerPC microprocessors with feature sizes of 130 and 180 nm.

This paper examines single-event upsets in advanced commercial SOI microprocessors; studying SEU clock frequency dependence of Floating Point Registers (FPRs), D-Cache and functional error ("hangs"). Results are presented for the Motorola MPC7448 SOI microprocessor with feature sizes of 90 nm, at three clock frequencies of 500, 1066 and 1600 MHz.

II. Experimental Procedure

A. Device Description

The Motorola 7448 is fabricated with a highly scaled process, using a feature size of 90 nm. It is build using partially depleted SOI technology without body ties. The Motorola device has a silicon film thickness of 50 nm and internal core voltage ranging from 1.0 to 1.3 V. The maximum

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operating frequency is 1.6 GHz. This device is packaged with "bump bonding" in flip-chip ball-grid array (BGA) packages.

B. *Experimental Methods*

Radiation testing was done at the Texas A&M University cyclotron. This facility produces long-range ions needed for SEU testing through thick materials. Particularly, the 40 MeV/amu beams have enough range that makes it possible to do irradiations in air rather than in vacuum. The ion beams used in our measurements are listed in Table I. Both ions have enough range to penetrate the die. The LET range of 1.7 to 14 MeV-cm^2/mg was covered in the measurements. All irradiations were done using ions with normal incidence. Because of the "flip-chip" design of the Motorola PowerPC, irradiation was done from the back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. The thickness of the die is about 900 μm. The measurement setup is shown in Fig. 1.

Table I. List of the ion beams used in our measurements.

Ion	**Energy per Nucleon (MeV/amu)**	**Initial LET (MeV-cm^2/mg)**	**Range (μm)**
^{20}Ne	40	1.7	1648
^{40}Ar	40	3.8	1070

Radiation testing of the Motorola MPC7448 SOI processor was done using the High Performance Computing Platform II (HPC II) development board from Motorola. This board was chosen because it eliminated the large engineering effort that would be required to design a custom test board for the processor. It provided a basic PROM-based system monitor instead of a complex operating system. This provides far better diagnostics and control of processor information during SEU testing compared to more advanced operating systems. One of the external communication channels provided on this board is a simple serial connection used as a "dumb" terminal.

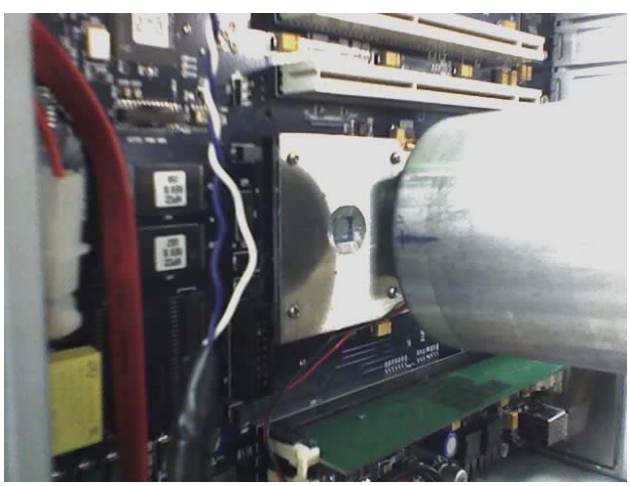

Fig. 1. PowerPC setup in beam line. The factory installed heat sink was replaced with a custom heat sink with an aperture.

The test methodologies used to measure the upset errors in the registers and D-Cache are described in [1] and [8] in detail. Tests were performed on two samples.

Assembly language software programs were written to detect errors in various sections of the processor. It was possible to design software that primarily exercised specific registers or regions, and thus allowed the number of errors to be determined for various registers or for specific operating modes. During some of the tests, the processor became non-functional (program "hangs" or SEFIs – single-event functional interrupts), and these types of errors are of extreme concern in applications because they may require complex procedures to restore normal operation. In most cases it was not possible to determine the underlying cause of these malfunctions because there are many possible ways in which processor operation can be disrupted. However, the relative occurrence of "hangs" was measured and compared to the upset rate obtained for internal registers or other functions of the processor.

We detected hangs by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, it was still operational to the point where normal software could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a hang. In nearly all cases, it was necessary to temporarily remove power from the device in order to recover and reboot the device. The analysis of hangs is complicated by the fact that one is not sure how much beam was delivered to the device before the hang occurred.

These upset results and discussions of their implications are the focus of the present work. SEU cross sections for D-Cache, hangs and Floating Point Register (FPR) are measured at three clock frequencies of 500, 1066 and 1600 MHz and an internal core voltage of 1.3 V. In particular, the results at three frequencies (500, 1066 and 1600 MHz) are compared. The clock frequency dependence of the results of functional tests of the microprocessors as well as the results of failures due to processor malfunctions is investigated.

III. Test Results

A. D-Cache

Figure 2 compares results of SEU measurements for the D-Cache of the Motorola PowerPC 7448 (90 nm feature size) to the results of the Motorola PowerPC 7457 (130 nm feature size). Also, for comparison the results of the Motorola PowerPC 7455 (180 nm feature size) is shown. The core voltage for all three microprocessors was 1.3 V. Even though the Motorola PowerPC 7448 processor has a much smaller feature size than the PowerPC 7455 and 7457, the LET threshold (LET_{th} is defined as the maximum LET value at which no effect was observed at an effective fluence of 1x10^7 ions/cm^2) is not very different. The LET threshold of the SOI PowerPC processors is about 1 MeV-cm^2/mg. The saturation cross section of the Motorola PowerPC 7448 is more than a factor of 5 smaller than that of the other PowerPC processors with feature sizes of 130 and 180 nm.

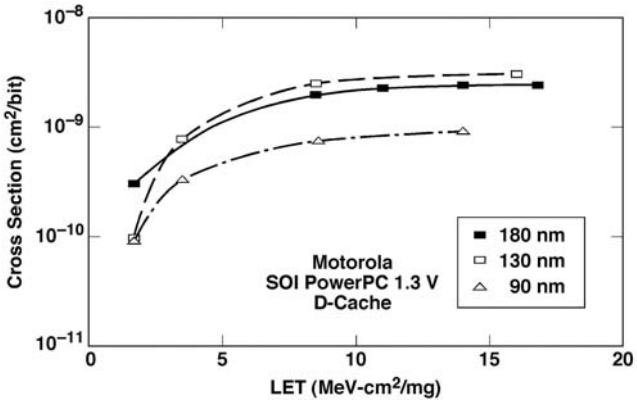

Fig. 2 Comparison of SEU cross-section for the D-Cache of the Motorola 7455, 7457 and 7448 PowerPC's. The core voltage for three microprocessors measurements was 1.3 V. The dashed and solid curves are only guides for the eye.

Figure 3 compares the SEU measurements for the D-Cache of the Motorola PowerPC 7448 at three clock frequencies: 500, 1066 and 1600 MHz. The large number of storage locations within the D-Cache allows more statistically significant numbers of errors to be measured, decreasing the error bars due to counting statistics. The error bars are one sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols.

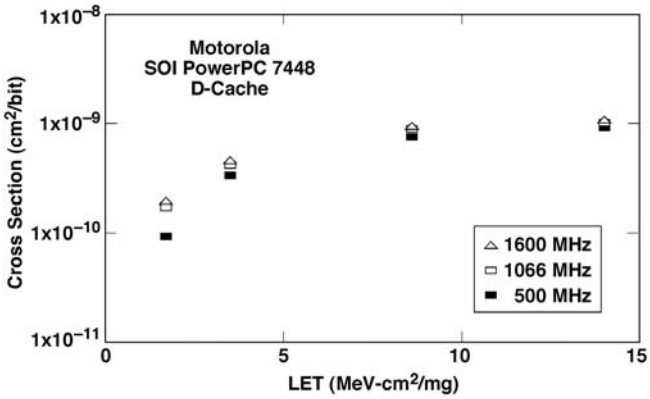

Fig. 3. Comparison of SEU cross-sections for D-Cache with clock speeds of 500, 1066 and 1600 MHz.

There is a clock dependence in the SEU measurements for D-Cache. The results with clock speeds of 1600 and 1066 MHz are larger compared with the results for a clock speed of 500 MHz. However, for the higher LET there is an agreement between the three clock frequencies. This implies that at low LETs the contribution from SETs is significant compared to the legitimate SEUs and their frequency dependence influences the overall SEUs. At high LETs the contribution of SETs is insignificant compare to the legitimate SEUs and the frequency dependence of SEUs vanishes. In order to present the clock frequency dependencies of the data in more detail we have plotted the data at each LET for clock frequencies of 500, 1066 and 1600 MHz in Figure 4. The cross section is plotted on a linear scale while the clock frequency is plotted on a logarithmic scale. Figure 4 clearly shows that the measured SEU increases with clock frequency. The difference in the SEU measurements is caused by the contribution from SETs. A SET in a digital circuit can manifest itself as a SEU in combinational logic cell and it has been demonstrated that the SETs in logic circuits increase with increasing circuit clock frequency [11-14]. We note that our previous measurements of D-Cache for the Motorola PowerPC 7455 with a feature size of 180 nm at two clock frequencies of 350 and 1000 MHz showed a similar clock frequency dependence [10].

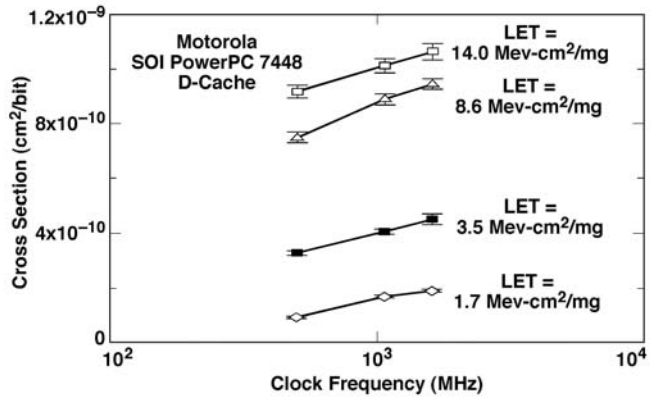

Fig. 4. Comparison of SEU cross-sections for D-Cache at clock speeds of 500, 1066 and 1600 MHz.

B. Registers

Figure 5, compares the SEU measurements for Motorola PowerPC 7448 FPR at three clock frequencies: 500, 1066 and 1600 MHz. The error bars are one sigma and result from Poisson statistics. Figure 5 clearly shows that the measured SEU for FPR increases with clock frequency and there is a clock frequency dependence in the data. The cross section results with 1600 and 1066 MHz clock speeds are systematically larger compared with the results for a clock speed of 500 MHz. Similar to the D-Cache data, this is caused by the contribution from SETs.

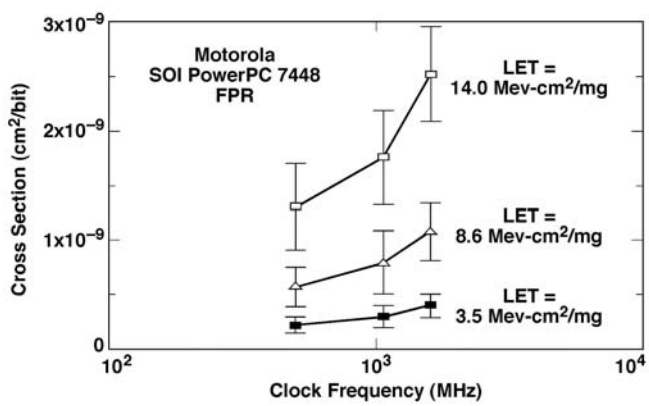

Fig. 5. Comparison of SEU cross-sections for FPR at clock speeds of 500, 1066 and 1600 MHz.

C. Functional Errors ("Hangs")

We also examined complex functional errors ("hangs") where the processor operation is severely disrupted during irradiation. We detected "hangs" by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, and then the processor was still operational to the point where normal software means could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a "hang". In nearly all cases, it was necessary to temporarily remove power from the device in order to recover and reboot the device. However, if a part stays in this mode, no evidence of damage or degraded operation is observed after the part is re-powered. The analysis of hangs is complicated by the fact that one is not sure how much beam was delivered to the device before the hang occurred.

In order to roughly scope problems with "hangs", we calculated the "hangs" cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed, including runs with no observed "hangs". This was done for each LET. Figure 6 compares estimated cross section for "hangs" for three clock frequencies of 500, 1066 and 1600 MHz during heavy-ion SEU measurements of the PowerPC 7448. The SEU cross section for three measured clock frequencies is statistically the same and there is no clock frequency dependence in the estimated cross section for "hangs", although the LET threshold is lower for 1066 and 1600 MHz data.

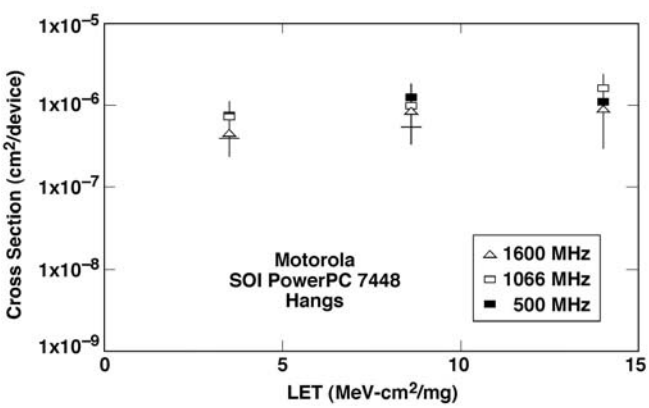

Fig. 6. Comparison of SEU cross-sections for "hangs" with clock speeds of 500, 1066 and 1600 MHz.

IV. Discussion

SEU testing involves writing a test pattern into the entire storage elements (such as registers and cache), irradiating with heavy ions, and then reading the storage element states to determine the number of SEUs. Obviously, clock frequency has no effect on measurements of this kind. However, if the memory is continuously written to and read during irradiation, clock frequency is expected to affect the cross section because there is a larger probability that transients from combinational logic operations will overlap clock edge transitions.

Recent experiments have demonstrated that the occurrence of SEUs in ICs increases with increasing clock frequency [11-14]. In fact, there is some evidence that at high frequencies the dynamic SEU rate may be dominated by errors generated in combinational logic rather than in sequential logic [13, 16]. In combinational logic, the output of the logic element is dominated by the inputs at that time, whereas in sequential logic, the output depends on the switching of a clock. For combinational logic circuits, the dependence of the dynamic SEU rate arrives from two sources: the varying of the sensitive area and varying the sensitive time. The sensitive period around a clock edge increases as the amount of energy deposited increases (higher LET). If the upset occurs just prior to the clock transition, less charge will be needed than if it occurs at an earlier time. If the ion strike occurs at a finite time prior to the clock edge, an upset may still occur, provided sufficient charge has been deposited by the ion so that the voltage transient will still be above the logic threshold for upset when the clock pulse arrives. If the ion strike occurs well before the clock edge, the transient will have decayed by the time the clock transitions, and no SEU will be registered. SEU's originate in combinational logic if the ion strike occurs in a period just prior to the clock transition from high to low, where the period depends on the amount of charge deposited by the ion [15].

Seifert et al., measured the frequency dependence of alpha-particle induced SEU in the 21164 Alpha microprocessor [12]. They found that the SEUs of the cache (which has no dynamic latch nodes) increase with frequency. However, their results suggest that SEUs in the Alpha core logic decrease with increasing clock rate and are dominated by the contribution from dynamic latch nodes. While the SEU increases with clock frequency for reading the content of memory cells, it decreases for upsets generated in level-sensitive transmission gate type latches. This is consistent with our results for the registers and D-Cache. It is also consistent with the expectations and explanation of Benedetto et al. [11] and Buchner et al. [13], that errors are caused by single event transients in coincidence with vulnerability windows associated with clock edges and increase proportionally with frequency.

Also, previous work has shown [15] that at high frequencies (more than 50 KHz) and in presence of ions with large LETs, gates in logic circuits may be sensitive to upsets during a large fraction of their duty cycle. Ions with large LETs will have a greater probability of producing an upset in a logic circuit gate than ions with small LETs because the window during which the gate is sensitive widens as the ion LET increases. Therefore, there will be more time during the clock cycle for which the circuit is sensitive. It is essential to know this information for circuits that operate at very high speeds and that contain gates whose upset sensitivity is clock-dependent, because the higher the speed the more chance there is of an upset occurring.

As device geometries continue to scale, SETs in digital circuits will soon become the dominant single event soft error phenomenon. SETs in digital devices and processors have received less attention at the device level, in large part because SETs have largely been insignificant to the total error rate. The overall soft error rate has been predominately determined by SEUs in the static-latch cells. However, with scaling below 130 nm and clock frequencies in GHz range, SETs are poised to dominate the SEE rate for commercial devices [11]. Also, Dodd et al., have shown that in both bulk and SOI technologies, scaling is predicted to lead to an increased ability for SETs to propagate [7]. Although this is balanced to some extent by the shorter duration of transients induced in scaled technologies, the overall trend is still toward increased SET susceptibility.

Although it is useful and instructive to make comparisons of single-event upset results as microprocessors within a given family evolve, one must remember that these are complex devices, not test structures. Other factors in the processor design may also affect the way that different processors in the series respond to radiation. There are also different requirements for various registers and functions within the device. For example, access time is a critical requirement for on-board cache, but cache single-event upset results may not be representative of other types of registers within the device. Therefore, it is important to evaluate single-event upset for different types of internal and storage elements because the overall upset rate of an operational program in real live application depends on how the various types of storage elements are used as well as their cross sections.

V. Conclusion

This paper has discussed clock speed dependency of SEU from heavy ion in the Motorola SOI PowerPC 7448 microprocessors. The SEU cross section has been evaluated at clock frequencies up to 1.6 GHz. There is a clock dependence in the SEU measurements. SEU cross sections are larger for higher clock speeds. These results might have important implication for the overall SEU as the trend for commercial silicon-on-insulator (SOI) microprocessors is to reduce feature size and internal core voltage and increase the clock frequency.

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