

# Data Converters Performance at Extreme Temperatures

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## Abstract

*Space missions often require radiation and extreme-temperature hardened electronics to survive the harsh environments beyond earth's atmosphere. Traditional approaches to preserve electronics incorporate shielding, insulation and redundancy at the expense of power and weight. However, a novel way of bypassing these problems is the concept of evolutionary hardware. A reconfigurable device, consisting of several switches interconnected with analog/digital parts, is controlled by an evolutionary processor (EP). When the EP detects degradation in the circuit it sends signals to reconfigure the switches, thus forming a new circuit with the desired output. This concept has been developed since the mid-90s, but one problem remains - the EP cannot degrade substantially. For this reason, extensive testing at extreme temperatures (-180° to 120°C) has been done on devices found on FPGA boards (taking the role of the EP) such as the Analog to Digital and the Digital to Analog Converter. Analysis of the results has shown that FPGA boards implementing EP with some compensation may be a practical solution to evolving circuits. This paper describes results on the tests of data converters at extreme temperatures.*

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### 1. Introduction

Planetary exploration and long-term satellite missions require radiation and extreme-temperature hardened electronics to survive the harsh environments beyond earth's atmosphere. Failure to take precautions against these unforgiving environments could lead to disastrous consequences, potentially jeopardizing life,

the vehicle, the mission and future funding. Thus for long-term missions it is essential that all electronics can somehow deal with faults. The traditional approaches to preserving electronics incorporate shielding, insulation and a good deal of redundancy, at the expense of flexibility, power and weight. Newer technologies are taking advantage of materials-based solutions and different circuit topologies; however, it is quite unlikely that it will operate fully at normal temperatures as well as the extreme temperatures as mentioned above.

However, satellites these days have a lifespan of 3 years. Within that time, one could venture far enough to be out of our reach for repairs and the satellite may have to be abandoned. The cost of such an action is tremendous - the Cassini mission alone cost \$3.4 billion. Furthermore, often times we cannot predict the environment that may place the electronics in danger. Electronics that is hardened for only a certain temperature range may have wildly different and unpredicted outputs outside of that range.

For example, the theoretical limit for silicon in the high-voltage regime (1000V) is 150°C [1]. However, temperatures can reach as hot as 470°C on the surface of Venus or dip below to -235°C on Pluto [2]. A novel approach to this dilemma is the concept of Evolvable Hardware (EHW) being developed at the Jet Propulsion Laboratory in Pasadena California. EHW is based on evolution's natural algorithm of selecting individuals who adapt best to an environment, survive and reproduce. The offspring created are similar to the parent but usually varied due to genetic alterations, either in reproduction or mutations.

The in-situ evolvable hardware system consists of two important subsystems: reconfigurable hardware (RH) comprised of functional blocks and reconfigurable fabric and an evolutionary processor (EP) running the evolutionary algorithm (the evolutionary processor). Since the EP is generating the stimulus and evaluating the results, its behavior must be characterized in the entire range of operation of the EHW system. Ideally, the system would not change in performance across temperatures. Temperature coefficients of components cause behavioral changes in the system. Commercial vendors of both ICs and systems typically minimize



## 2. DAC characterization

The AD9772A is a 14-bit single-supply, oversampling digital to analog converter optimized for baseband or IF waveforms. Unfortunately, the waveforms used by JPL spread a broad range of frequencies, which requires both accuracy and speed, which industry usually does not supply. In this case accuracy was preferred over sampling speed because several bits of precision are predicted to be lost due to noise, gain, and temperature effects when on the FPGA board.

A 4-inch ribbon cable was first created to communicate with the DAC. This was taped to the outside of the oven and was wired in, along with banana plugs for power and coaxial cables with BNC connectors for analog output. The ribbon cables' individual lines were then wire-wrapped to two breakout boxes just outside the oven. Two NI-DAQ boards (one for output, one for input) were then wired to the breakout boards with a proprietary cable. Below is a diagram of the setup

A VI was then created in Labview that output 2.5V or 0.5V along 14 analog channels corresponding to a digital value of 1 or 0 on the NI-DAQ output board. The program output every code from 0 to 16383 and for each code read back in (on the NI-DAQ input board) 100 analog values. The program then averaged these values and output a formatted file with the digital value and the corresponding analog value.

A second Labview program controlled the temperature of the oven according to specifications, by controlling the amount of liquid nitrogen used to cool it.

Both programs were run simultaneously and the DAC underwent a test at room temperature (25° C) then subsequent tests from 0° C to -180° C in increments of 30°. Time was provided at each interval for the stabilization of the temperature, a complete testing of digital codes, and about 5 to 6 extra minutes before continuing to the next temperature. Each test took approximately 70 minutes.

The following day the DAC was tested at 60°, 90° and 120° C with a final post-experiment room-temperature test.

The formatted file was then read in by a C++ program that computed the offset, gain, the INL and the DNL. The program output an INL and a DNL file with it that provided their values at each digital code. A few scripts in Matlab then processed all the data for visual display.

A first analysis shows that as the temperature is decreased below -90° the gain begins to increase (Figure 2 and Table 1). This is a significant problem

without compensation. The theoretical gain should be about  $1V/16384$ , which equals  $0.000061V$ . At -180° this is an error of 19.7%. The offset seems to be fairly stable. Significant changes beyond noise and sampling error are not apparent.

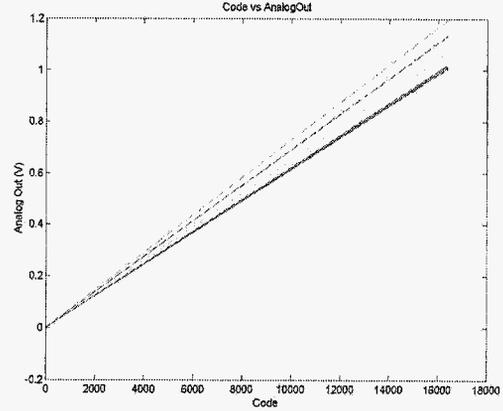


Figure 2: DAC Gain and Offset at different Temperatures.

Temp (°C)	Gain	Offset
-180	.000073	-0.0009738
-150	.000069	-0.0010043
-120	.000065	-0.0009941
-90	.000061	-0.0006235
-60	.000062	-0.0005478
-30	.000062	-0.0006133
0	.000062	-0.0004802
Room	.000062	-0.0011115

Table 1: DAC Gain and Offset

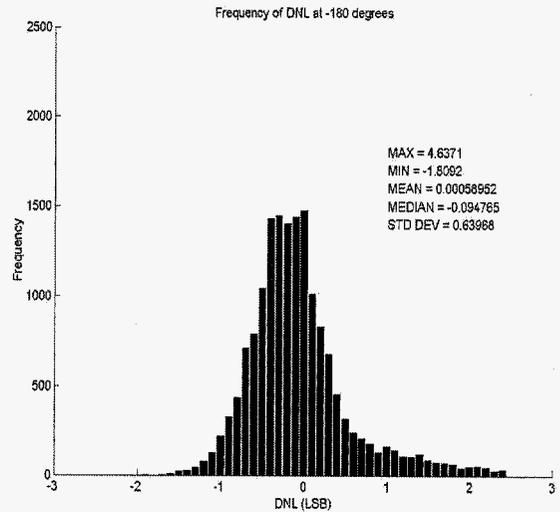
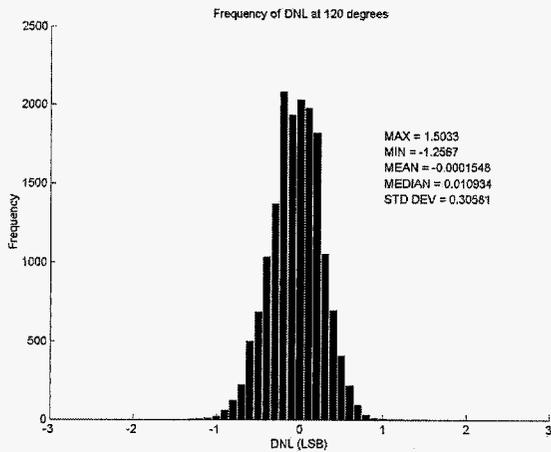
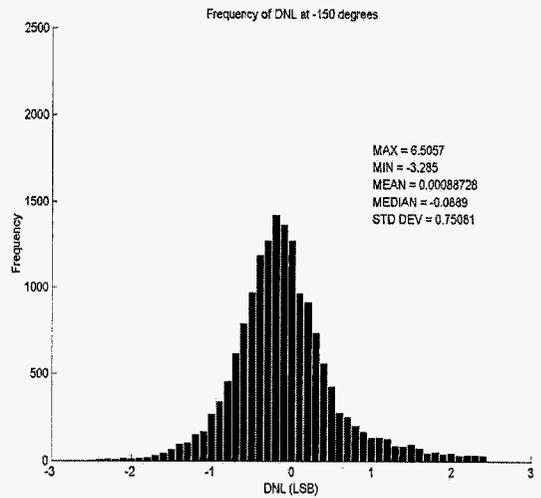
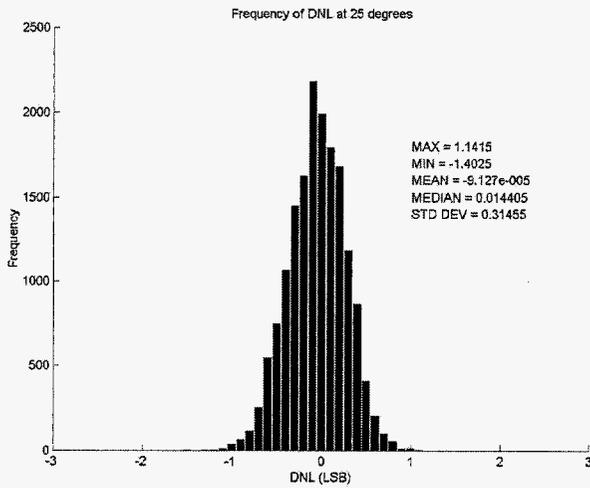
In addition to gain and offset values, the Differential and Integral Non-linearity metrics were used to characterize the DAC.

Differential Non-Linearity (DNL) is computed with the equation:

$$DNL = (V_{d+1} - V_d) / (V_{LSB-IDEAL} - 1) \text{ where } 0 < D < 2^N - 2$$

This records the change from one step to another in the unit of Least Significant Bits (LSBs). The DAC performed very well using the DNL metric. The results show that the chip was not damaged in the process of testing and retained its DNL properties after returning to room temperature. And temperature

increases, the DAC actually seems to perform better. However, it should be noted that slight degradation is apparent in the standard deviation below  $-90^{\circ}$ . The DAC is guaranteed to have values of  $\pm 2.0$  LSBs for DNL in the specified range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The experiment performed qualifies this claim, since only at  $-120^{\circ}\text{C}$  there is a slight shift to the right past  $+2.0$  LSBs (the DNL should stay between  $-1\text{LSB}$  and  $1\text{LSB}$ ). Figure 3 illustrates a histogram of the DNL at various temperatures.

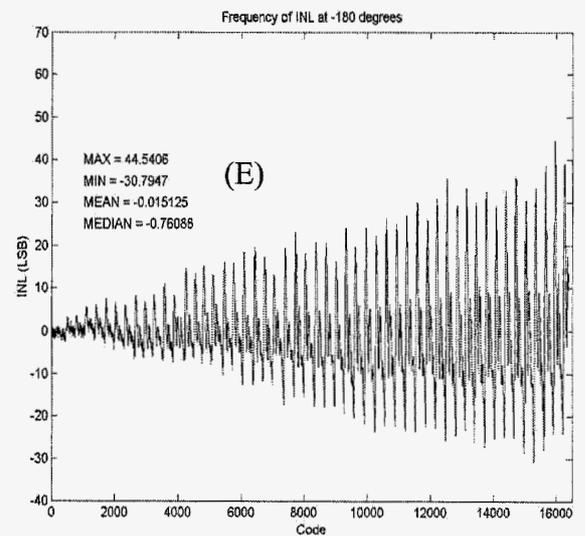
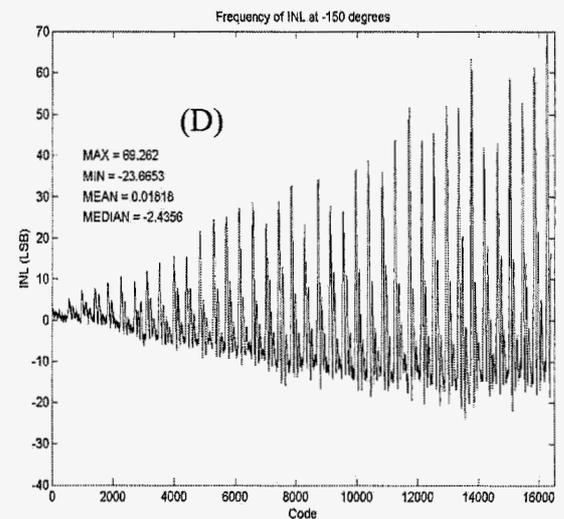
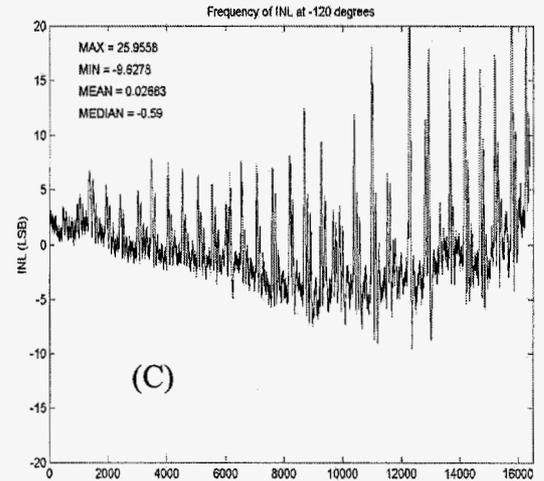
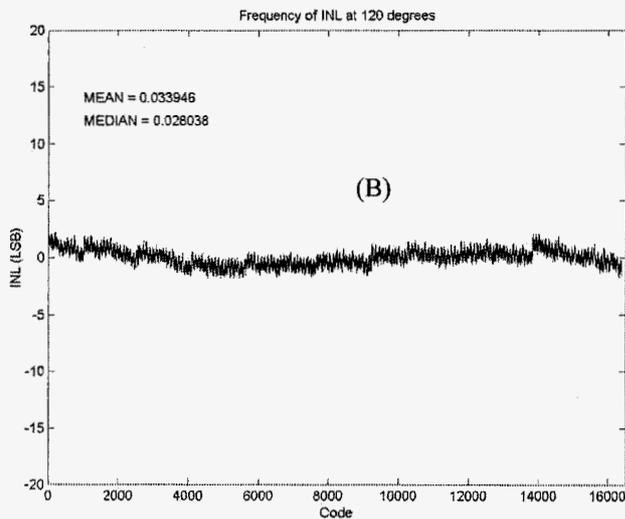
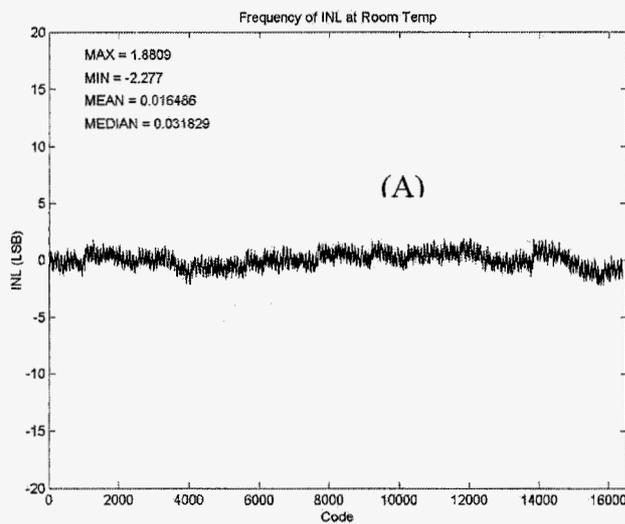


**Figure3:** DNL at 25C (upper left); 120C (lower left); -150 C (upper right); and -180C (lower right).

The Integral Non-Linearity (INL) is computed with the following equation:

$$INL = (V_D - V_{zero}) / V_{LSB-IDEAL} - D, \text{ where } 0 < D < 2^N - 1$$

INL measures the difference between the best-fit line and the sample taken in units of LSBs. The DAC did not perform so well using this metric. Degradation is easily apparent past  $-90^\circ$ , in which the INL oscillates rapidly as the code increases. The INL does adhere to the properties guaranteed on the AD9772A data sheet. INL is typically within  $\pm 3.5$  LSBs between  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



**Figure 4:** Integral Non-Linearity for different temperatures (A) Room Temperature; (B) 120C; (C) -120C; (D) -150C; (E) -180C.

### 3. ADC Characterization

The Analog Devices AD6645 is a 14-bit 80/105 MSPS analog to digital converter maintaining performance up to 200Mhz. It has a differential analog input comprised of pins AIN and /AIN; these input pins take signals with a DC level of 2.4 V and an AC level of +/- .55 V. This allows at differential analog input signal of 2.2 Vpp. This ADC also requires an encode clock signal, which must be fed a high-quality, low phase-noise source to maximize Signal to Noise Ratio. On the evaluation board, there is also an inductor, a capacitor and several resistors that will contribute noise and non-linearity.

An 8-inch 50 mil flat ribbon cable was used to connect the ADC evaluation board to the FIFO board outside the oven. Power lines were brought outside with molded banana cables. The SMA signal jacks on the evaluation board were connected to a SMA-M to BNC-F converter and then brought out using 50 ohm BNC coaxial cable. The FIFO board was then hooked up to a PC through a USB cable. A diagram of the setup is shown below.

Analog Devices included software for data acquisition with the FIFO board. The provided ADC Analyzer, was inadequate to test the ADC since it could only take 16383 samples at a time. To measure INL and DNL accurately using the histogram method, about 4 million samples are needed. For this reason, a Windows macro creator was installed called Autoit and a macro was written to automate capturing 200 sets of data.

Proper technique for testing an ADC involves slightly clipping the input wave. This amounts to several more codes at the boundaries (0 and 16383 in this case) and it allows a more accurate calculation of INL and DNL. In this case a 1.75Vpp covered the full range of the ADC.

For each 30°C increment from -180°C to +125°C, 200 files of 16383 samples were acquired. A quick analysis showed that the ADC board failed some time after 90°C, so a second set of tests were performed to attain better knowledge of when it failed; these tests were performed at 90°C, 100°C and 110°C.

Next a MATLAB script was written to plot a histogram and calculate the mean values. From this histogram, INL and DNL were calculated.

ADCs are often tested using the histogram method. This method relies on the fact that there is a specific probability density function for sinusoidal waves, governed by the equation:

$$p(V) = 1/(\pi * \text{sqrt}[A^2 - V^2])$$

where A = Amplitude of the input sine wave  
V = Voltage

When plotted this equation yields (Figure 5):

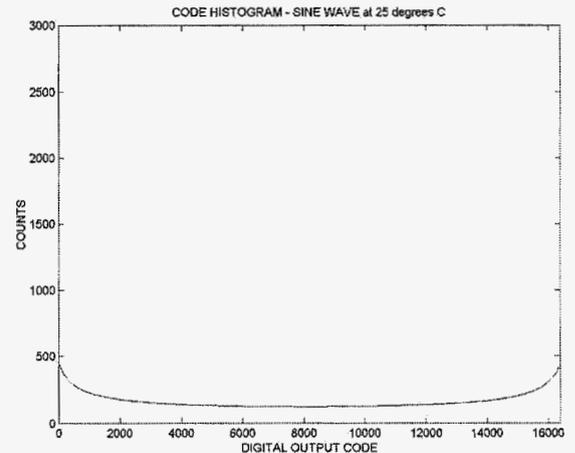


Figure 5: Ideal ADC histogram.

If an adequate number of samples are collected, a histogram of ADC output should mimic this equation closely. Any deviation can be used to calculate Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), which can be used to assess the accuracy of the ADC. A sample at 25°C shows a nice bathtub-like distribution for the AD 6645 under test (Figure 6).

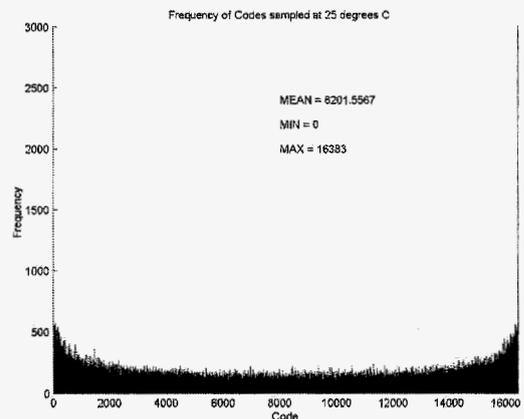


Figure 6: Histogram for ADC at room temperature.

However, at -30°C, a drop in amplitude can be seen with the narrowing of the boundaries (Figure 7). This is likely due the RF transformer, which is not designed for operation at extreme temperatures. At each

subsequent temperature level, the boundaries shrink even further.

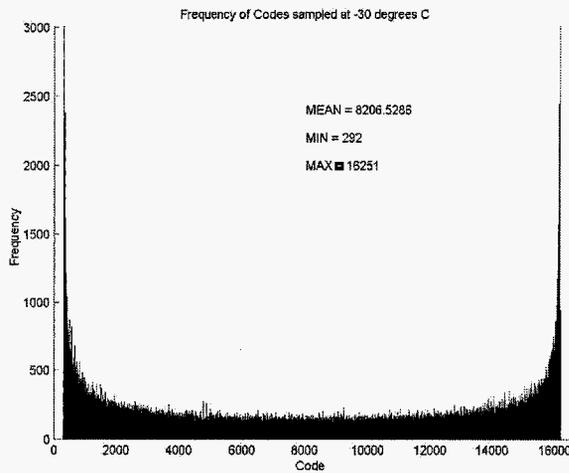


Figure 7: Histogram for ADC at -30C.

At -120°C, more deterioration is observed and a few codes seem to be missing (Figure 8). By -180° several chunks of codes are missing (Figure 9).

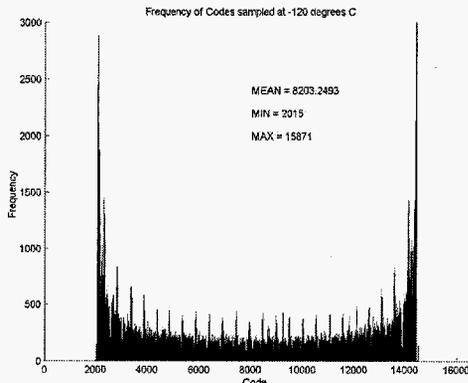


Figure 8: Histogram for ADC at -120C

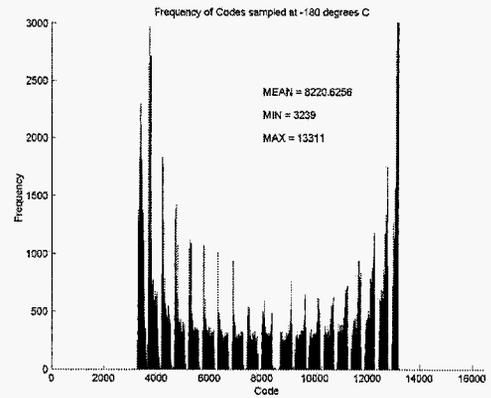


Figure 9: Histogram for ADC at -180C

At high temperatures the evaluation board stops functioning somewhere between 100° and 110°; however this may not be due to the ADC and could be due to the failure of the RF transformer. With an input of 1.75V, the ADC generated more or less a straight line around the mid-point. No parts of the ADC were observed to be permanently damaged, since the room temperature test after the experiments once again yielded a bathtub distribution.

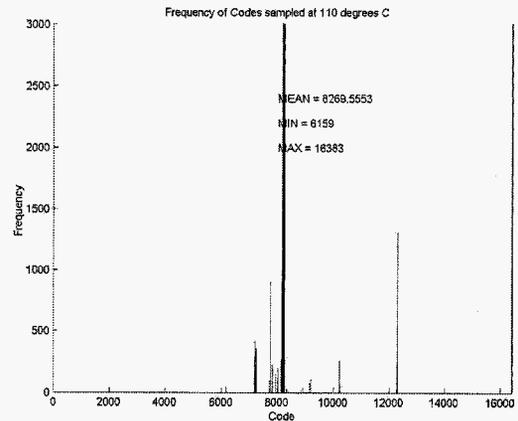


Figure 10: Histogram for ADC at 110C

DNL was defined before as:

$$DNL = (V_{d+1} - V_d) / V_{LSB-IDEAL} - 1 \text{ where } 0 < D < 2^N - 2$$

However, since a wave generator was used to test the ADC, the voltage corresponding to a specific code is not easily attainable, as it was in the DAC. Instead, the plotted histogram can be compared to the probability density function of a sine wave to yield the DNL. This determined by the equation:

$$DNL = [AP_n/IP_n] - 1$$

where  $AP_n$  = actual frequency of samples in nth bin  
 $IP_n$  = ideal frequency of samples in nth bin  
 $IP$  is simply the total number of samples multiplied by the probability function.

The shrinking boundaries at every temperature level below 0°C corresponds to a slight reduction in amplitude output by the ADC. Since this is most likely a deficiency of the RF transformer, it cannot be considered a non-linearity and must be dealt with appropriately.

Standard procedure for testing an ADC is to clip a small portion of the incoming analog signal. For this test a 1.75Vpp was used which was about .15V above the full-scale range the ADC could handle. This limits DNL and INL errors, which are artifacts of a slightly misplaced wave function close to the end boundaries (0 and  $2^N-1$  for full scale range). The drop in amplitude effectively re-introduced these errors. To compensate, the probability density function was shrunk down by specifying boundaries and then laid over the histogram. Any stray codes past this boundary were ignored, simulating a clipping at that code. Figure 11 plots the DNL against the output code at room temperature.

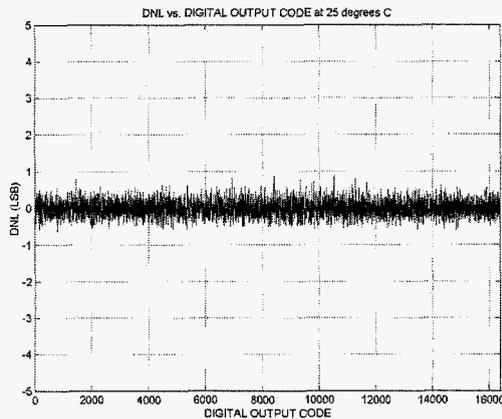


Figure 11: DNL versus output code at 25C.

The ADC performed well under the DNL metric. Virtually no degradation occurs at high temperature until the ADC failed. On the low side though, degradation occurs below -120°(Figure 12) and

codes are missing at -150° and below. Using the equation implemented, a -1 value for DNL occurs only when there is a missing code. However, the results are not a major deviation from specifications in the data sheet until -180° (Figure 13) as Analog Devices only guarantees 12-bit no missing codes.

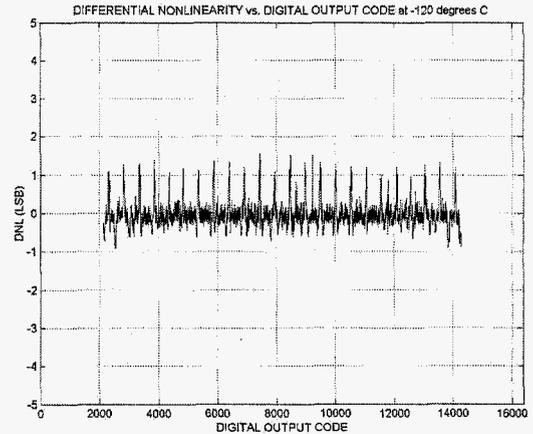


Figure 12: DNL versus output code at -120C.

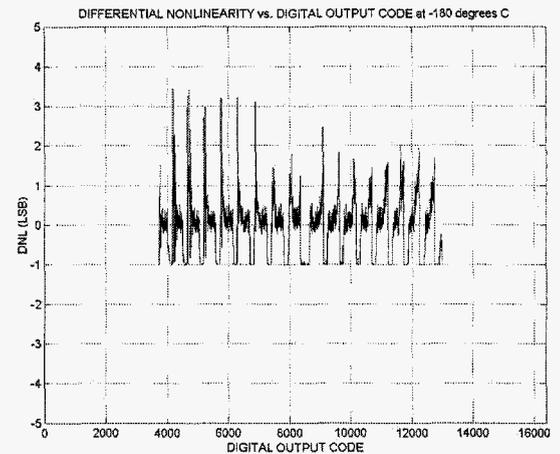


Figure 13: DNL versus output code at -180C.

INL was computed as follows:

$$INL_j = \text{sum}(DNL_n, \text{from } n=1 \text{ to } j) \quad \text{where } j \text{ is the code being analyzed}$$

Reaching as high as 12 LSBs of INL at room temperature (Figure 14), the ADC did not perform so well using this metric. This is evidence that there may have been undersampling. This could not be helped though, since there was a limited amount of time to perform this experiment (200 x 16383 or 3,276,600

samples were taken at the time). This corresponds approximately to a 90% confidence level.

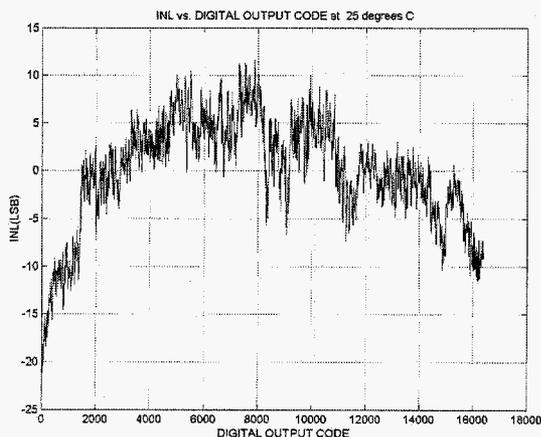


Figure 14: INL versus output code at 25C.

Heat slightly degraded the INL performance of the ADC compared to its normal characteristics at room temperature as seen in the graph (Figure 15).

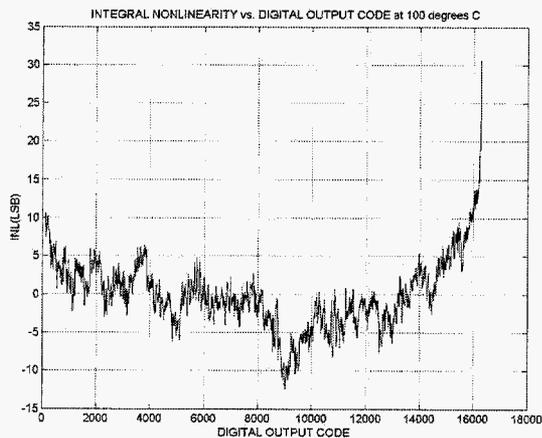


Figure 15: INL versus output code at 100C.

Cold temperature testing on the other hand greatly effected the INL characteristics of the ADC. Degradation begins at -120 (Figure 16) and continues to worsen at lower temperatures (Figures 17 and 18).

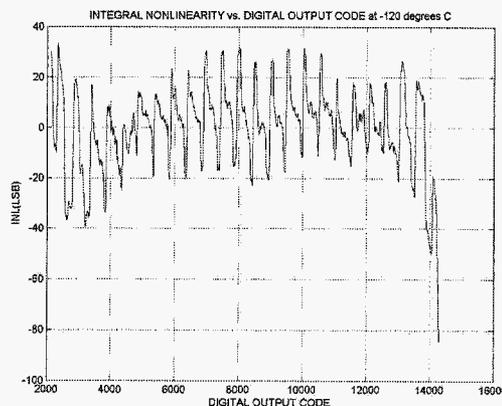


Figure 16: INL versus output code at -120C.

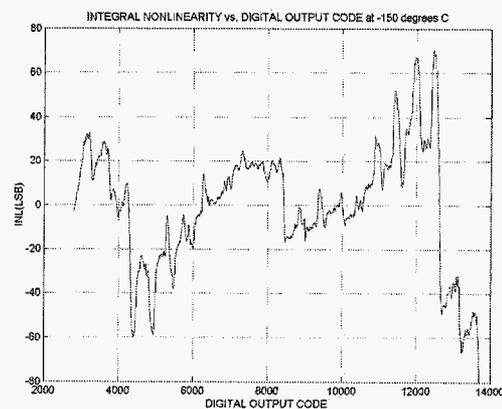


Figure 17: INL versus output code at -150C

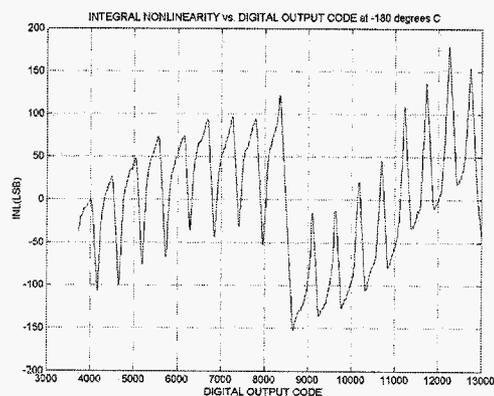


Figure 18: INL versus output code at -180C.

Also, since the sine probability function was superimposed onto the histogram, because of the drop in amplitude, further error is amassed towards the ends of the boundaries. This is shown in the graphs when INL increases or decreases very rapidly towards the

ends. This does not necessarily indicate deterioration in INL; rather, it shows the complications of dealing with an approximate mathematical function.

However, despite all these complications, the ADC should provide enough accuracy at extreme temperatures (-180° to 100°C) as it only loses about 5 to 6 bits of accuracy leaving a 8 to 9 bit ENOB ADC, which is sufficient for our evolvable system.

## 5. Conclusion

Characterization of the evolvable platform is essential to its practical use in applications. Extreme temperature tests were performed upon devices necessary in analog circuits – the ADC and DAC. Though performance deteriorates, with compensation the ADC-DAC chain, can be effective between the temperatures of -180°C to 100°C with 8 to 9 effective number of bits. FPGA boards, taking the role of the EP, using these devices will therefore not be limited considerably by faulty data. In future work an FPGA board will be running an algorithm to evolve filters on Wide Range Transconductance Amplifiers (WRTAs). Preliminary tests show this is a worthy endeavor.

## 6. Acknowledgements

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## 7. References

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