Extreme Temperature Electronics Using a Reconfigurable Analog Array

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*SPAWAR

Abstract—Temperature and radiation tolerant electronics, as well as long life survivability are key capabilities required for future NASA missions. Current approaches to electronics for extreme environments focus on component level robustness and hardening. Compensation techniques such as bias cancellation circuitry have also been employed. However, current technology can only ensure very limited lifetime in extreme environments. Previous work presented a novel approach, based on evolvable hardware technology, which allows adaptive in-situ circuit redesign/reconfiguration during operation in extreme environments. This technology would complement material/device advancements and increase the mission capability to survive harsh environments. This work describes a new reconfigurable analog chip developed by JPL and SPAWAR that is targeted for extreme temperature and evolutionary hardware experiments. Being based on Gm-C technology, this chip can have its functionality tuned and adapted to extreme temperatures through voltage bias adjustment. This tuning process will be controlled by Evolutionary Algorithms. This paper presents details of the reconfigurable analog chip as well as a system level overview. Some early experiments are also described.

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1. INTRODUCTION

In-situ planetary exploration requires extreme-temperature electronics able to operate in low temperatures, such as below –220°C on Neptune (-235°C for Triton and Pluto) or high temperatures, such as above 470°C as needed for operation on the surface of Venus. Extrapolations of current developments indicate that hot electronics technology for >400°C environments may not be ready in time for the 2006-2007 missions, except possibly for "grab-and-go" or "limited life" operations [1]. For extended missions, innovative approaches are needed. Terrestrial applications include combustion systems, well logging, nuclear reactors and dense electronic packages.

The maximum working temperature for semiconductors can be estimated from their intrinsic carrier density, which depends on the band-gap of the material. When the intrinsic density reaches the doping level of the devices, electrical parameters are expected to change drastically [2]. For the high-voltage regime (1000V), the theoretical limit for silicon is 150°C; for discrete devices below 100V, it is expected about 250°C [2]. Materials used up to 300°C include bulk silicon and silicon-on-insulator (SOI) technologies; for higher temperatures, gallium arsenide (GaAs), silicon carbide (SiC), and diamond show promise, and devices have been demonstrated at 500°C [3]. A survey of high-temperature effects and design considerations is found in [4]. A review of the physical limits and lifetime limitations of semiconductor devices at high-temperatures is found in [2].

In addition to material/device solutions, circuit solutions for the compensation of the effects of temperature have also been employed. Circuit solutions that compensate offset voltage and current leakage problems are described for example in [3], where several circuit topologies for high-temperature design, including a continuous-time auto-zeroed OpAmp and an A/D circuit that uses error suppression to overcome high-temperature leakages, are given. Another circuit

for high-temperature operation with current leakage compensation is presented in [5]. Bias cancellation techniques for high-temperature analog application are presented in [6].

All the above solutions are fixed circuit design solutions, and satisfy the operational requirements only over a given temperature range. Once the limits of the range are exceeded, the performance deteriorates and cannot be recovered. In a previous work [7], the authors described the use of reconfigurable chips, which allow for a large number of topologies to be programmed, some more suitable for high-temperature. The interconnections between components could be changed, and new circuits could be configured, in an arrangement that used the on-chip components/devices *at the new operational point on their characteristics*. These experiments were performed in the so-called Field Programmable Transistor Array (FPTA).

This paper introduces a new reconfigurable chip architecture, simply called Reconfigurable Analog Array (RAA). The rationale behind the RAA is to have a set of conventional Gm-C filter architectures whose behavior can be tuned by bias voltages. Recovery at extreme temperatures can then be accomplished by changes in the bias voltages, instead of changing the circuit topology as in the case of the FPTA. One advantage of this new procedure is the potential to achieve higher performance solutions at extreme temperatures.

Circuit reconfiguration can be controlled by evolutionary algorithms or by other simpler stochastic algorithms. Particularly, Evolvable Hardware (EHW) is a research area that investigates the design of circuits by means of evolutionary algorithms. The reader can refer to [8-10] for works in EHW.

The paper is organized as follows: Section 2 reviews the concept of evolutionary circuit design and briefly reviews previous circuit recovery experiments at extreme temperatures. Section 3 provides a system level description. Section 4 presents the details on the RAA chip architecture. Section 5 presents preliminary experiments that illustrate analog filter recovery at extreme temperatures. Section 6 concludes the work.

2. Evolutionary Circuit Design

The idea behind evolutionary circuit synthesis/design and evolvable hardware is to employ a genetic search/optimization algorithm that operates in the space of all possible circuits and determines solution circuits with desired functional response (here the word synthesis is used in most general sense). The genetic search is tightly coupled with a coded representation of the candidate circuits. Each circuit gets associated a "genetic code" or chromosome; the simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. Synthesis is the search in the chromosome space for the solution corresponding to a circuit with a desired functional response. The genetic search follows a "generate and test" strategy: a population of candidate solutions is maintained each time; the corresponding circuits are then evaluated and the best candidates are selected and reproduced in a subsequent generation, until a performance goal is reached. In this project, since device models at extreme temperature are not available, circuit evaluation is done directly in reconfigurable hardware, called *intrinsic*.

An evolvable hardware system is constituted of two main components: reconfigurable hardware (RH) and an evolutionary processor (EP) that acts as a reconfiguration mechanism (Figure 1). In the evolvable system built for a previous effort, the EP was implemented and ran on a stand-alone DSP board. The RH was embodied in the form of a Field Programmable Transistor Array (FPTA-2) architecture, a custom made chip fabricated in silicon.

The Field Programmable Transistor Array (FPTA) presents a cellular architecture, with each cell having a set of transistors, which can be interconnected by transmission gate switches. This architecture allows reconfigurability at the lowest (transistor) level, and it generates a huge search space constituted of different circuit topologies, most of them very different from human designed circuits. More details on the FPTA can be found in [11].

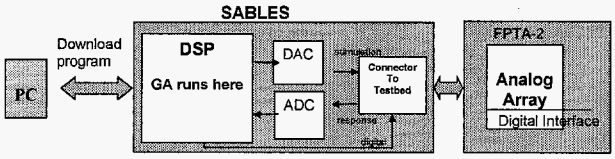


Figure 2. Block diagram of a simple stand-alone evolvable system.

We briefly review one experiment for evolutionary recovery of the functionality of a low-pass filter at 230°C using the FPTA. More details can be found in [7]. The rationale of these experiments was of first evolving the proposed circuits at room temperature. After the functionality is achieved the temperature is increased using a hot air jet [7] until the functionality is degraded. In order to recover the functionality, the evolutionary process is started again at high temperature. Therefore evolution can obtain a circuit that works at high temperature if the search process is

carried on at the temperature in which the circuit is supposed to work.

The objective of this particular experiment was to recover the functionality of a low-pass filter given ten cells of the FPTA2 (Figure 2). The fitness function given below performs a sum of error between the target function (T) and the output from the FPTA in the frequency domain.

$$F = \sum_{f_s=0}^{n-1} (R(f) - T(f)) \qquad (1)$$

Given two tones at 1kHz and 10kHz, the objective is to have at the output only the lowest frequency tone (1kHz). This hardware evolved circuit demonstrated that the FPTA2 is able to recover active filters with some gain at 230°C. Figure 2 shows a view of the cell array in the FPTA2 chip, with the 10 cells used in the experiment labeled from 0 to 9. The input is applied to several cells, while the output is taken from cell 9.

Figure 3 shows the response of the evolved filter at room temperature and degradation at 230°C. Figure 4 displays the same information in the frequency domain. Figure 5 shows the time and frequency response of the recovered circuit evolved at 230°C

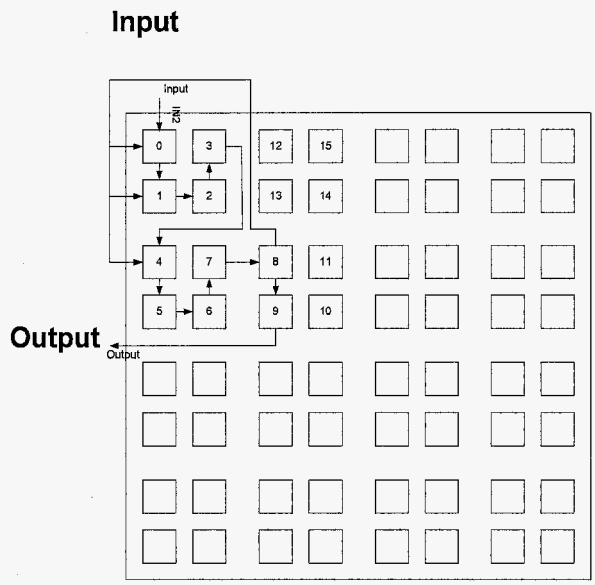


Figure 2: FPTA cells used in the low-pass filter experiment.

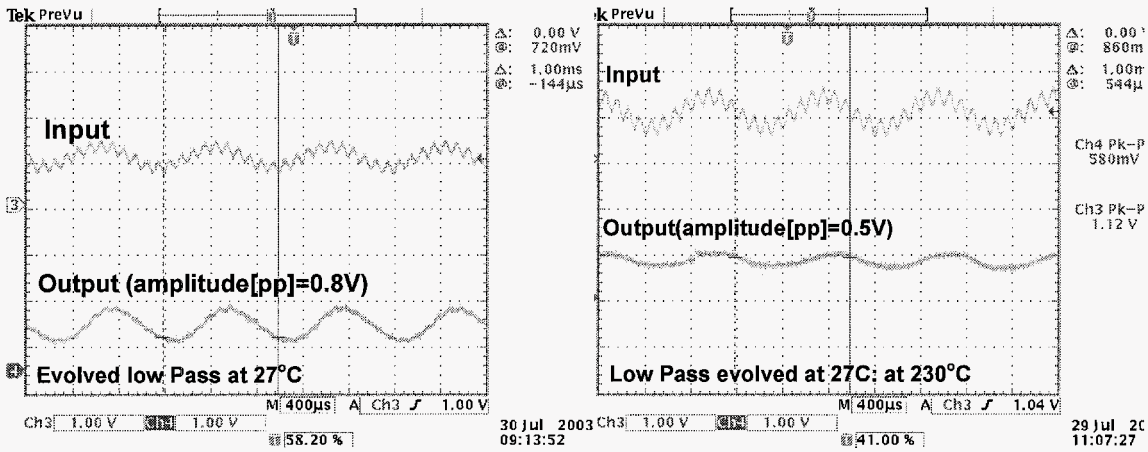


Figure 3: Low-Pass Filter. The graph in the left displays the input and output signals in the time domain. The graph in the right shows the input and output in the time domain when the FPTA-2 was submitted to temperature of 230°C (Circuit stimulated by two sine waves: 1kHz and 10kHz).

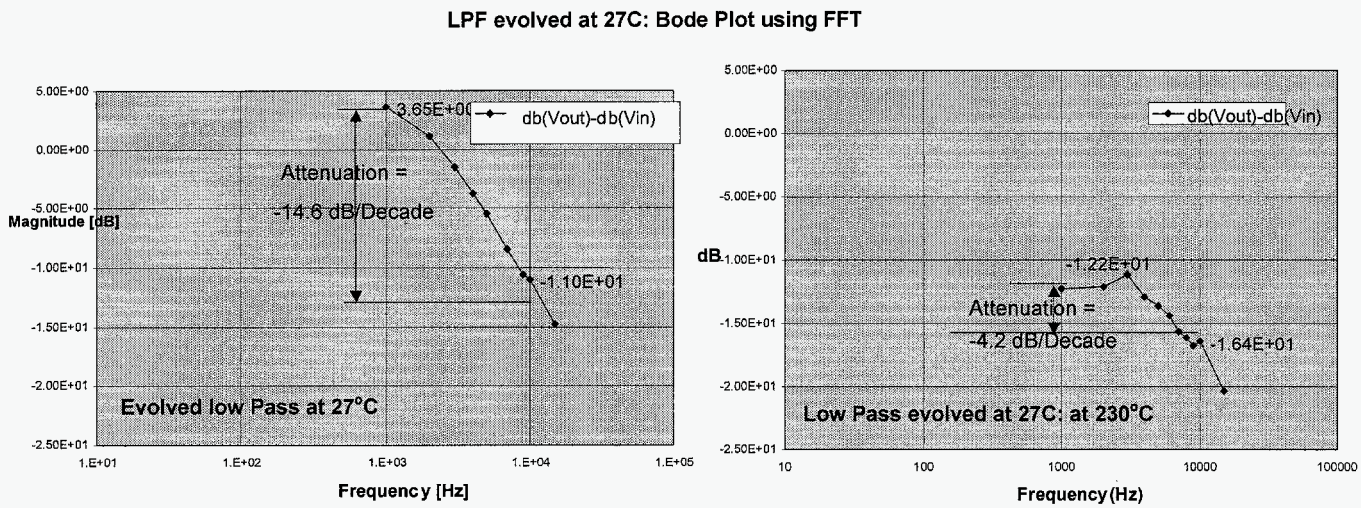


Figure 4: Low-Pass Filter. The graph in the left displays the frequency response of the output signal at room temperature. The graph in the right shows the frequency response of the output when the FPTA-2 was submitted to temperature of 230°C. (Circuit was stimulated by a sine wave with a frequency sweeping from 1kHz and 10kHz).

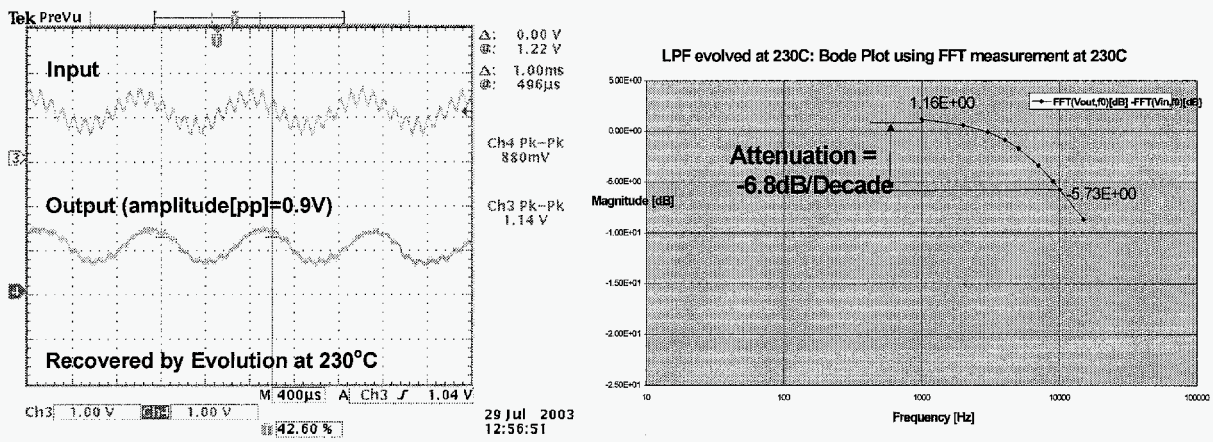


Figure 5: Low-Pass Filter. The graph in the right displays the Bode diagram of the output signals. The graph in the left shows the circuit input stimulus and response in the time domain (Time response was obtained using a stimulation signal made of two sine waves: 1kHz and 10kHz – Frequency response was obtained by sweeping a frequency from 1kHz to 10kHz.)

At room temperature, the originally evolved circuit presents a gain of 3dB at 1kHz and a roll-off of -14dB/dec. When the temperature is increased to 230°C, the roll-off goes to -4dB/dec and the gain at 1kHz falls to -12dB. In the recovered circuit at high temperature the gain at 1kHz is increased back to 1dB and the roll-off goes to -7dB/dec. Therefore the evolved solution at high temperature is able to restore the gain and to partially restore the roll-off.

One limitation of these experiments is that only filters with modest roll-off characteristics (around 20dB/decade) could be evolved or recovered using the FPTA. A new architecture has therefore been devised to address the problem of synthesis of higher performance analog filters, as described in the next sections. Another limitation of this experiments was the fact that only the reconfigurable chip was exposed to high temperatures; the Evolutionary Processor (DSP) was at room temperature.

3. System Level Considerations

One of the objectives of this project is to have both the reconfigurable hardware (RH) and an evolutionary processor (EP) placed inside the extreme temperature chamber. In the previous tests described above, only the reconfigurable hardware (FPTA) was placed in the extreme environment. In other experiments, the EP only was tested in an extreme environment chamber.

Two options were considered to implement the Evolutionary Processor, the DSP as in the previous system and an FPGA. Early tests demonstrated that the FPGA Virtex-II Proto-board withstood lower temperatures then the particular DSP board used in the previous evolvable system [12][13]. Based on these results, we decided to implement

the Evolutionary Processor of the new system using an FPGA.

4. RECONFIGURABLE ANALOG ARRAY

The main objective of the new RAA chip is the implementation of analog filters that can be tuned to meet specifications at extreme temperatures. The use of Gm-C filters was therefore chosen, since these filters can have their responses adjusted through bias voltages [14]. Wide Range Transconductance Amplifiers (WRTA) [14] are the building blocks of these filters. The WRTA topology is shown in Figure 6.

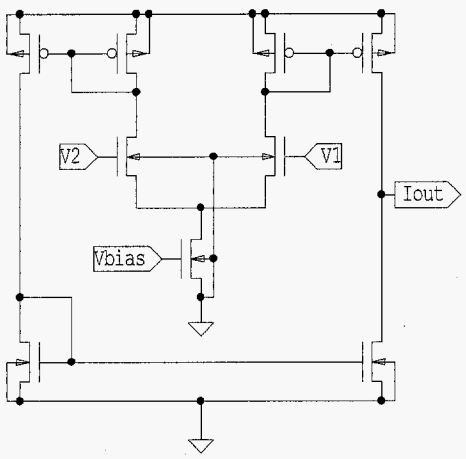


Figure 6 – WRTA Topology.

The WRTA has its transconductance and its IxV characterisics dependent on the voltage applied to vbias in the figure above. Several filter topologies can be implemented using the WRTA. Figures 7 and 8 show respectively a first and a second order Gm-C filters implemented on the RAA chip.

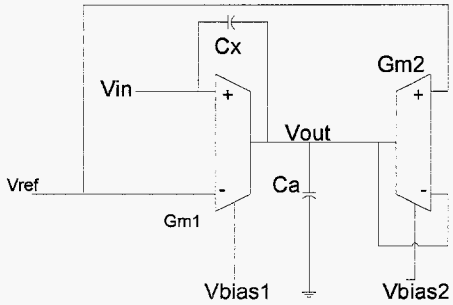


Figure 7: First Order Gm-C Filter.

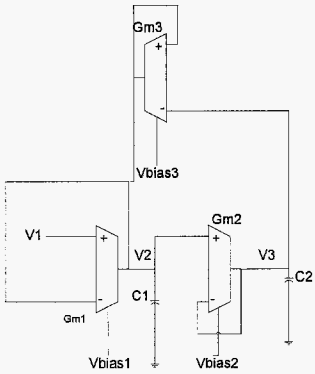


Figure 8: First Order Gm-C Filter.

In the figures above, it can be seen that the filters can have their behaviors adjusted through two (first-order) or three(second-order) bias voltages. The RAA chip is constituted of several arrays of first-order and second-order filters interconnected through switches. Figure 9 illustrates one of these arrays.

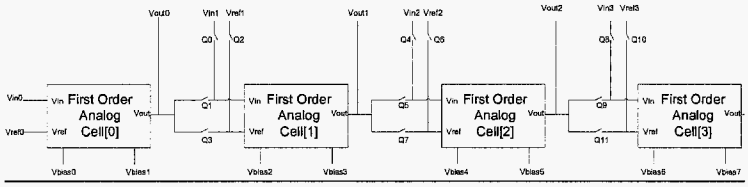


Figure 9: First-order filter array.

Besides the possibility of functionality adjustment through bias voltage changes, the interconnection switches provide an additional degree of flexibility for the implementation of several filter transfer functions (low-pass, band-pass etc).

Besides first and second order filters, the RAA chip also includes other topologies such as biquad, 4th order low-pass, etc.

5. PRELIMINARY EXPERIMENTS

Preliminary temperature tests were performed in the Evolutionary Processor components (DSP, FPGA) and in the analog filters. This section describes temperature tests performed on the analog filter components; the DSP/FPGA tests are described elsewhere [12-13].

We have tested the behavior of Gm-C filter building blocks at extreme temperatures (from -180°C to 120°C). We have also performed preliminary tests on the functionality recovery through changes in the voltage bias.

5.1 WRTA characteristics at Low Temperatures

Current lower and upper limits reduce as the temperature reduces as observed in the figure 10. Device function can be recovered by increasing Vb from 0.8V to 0.85V as observed the experimental shown in the figure 11.

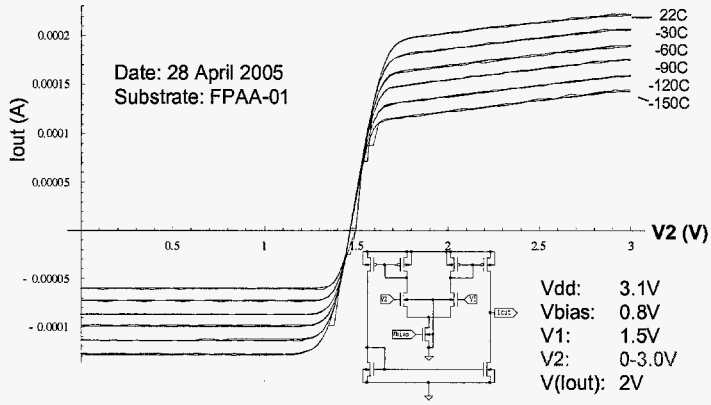


Figure 10: WRTA response change the temperature decreases.

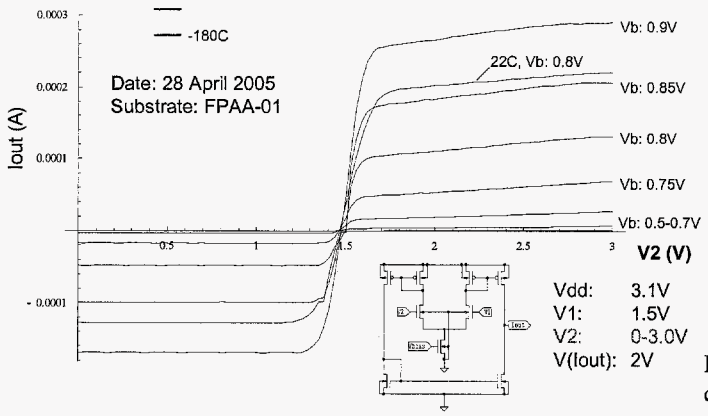
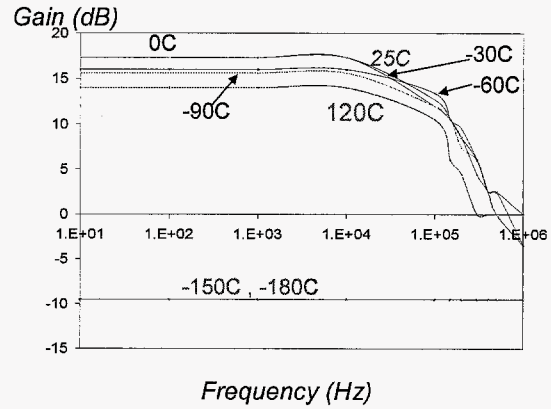


Figure 11: WRTA functionality recovery through Vbias (V2)



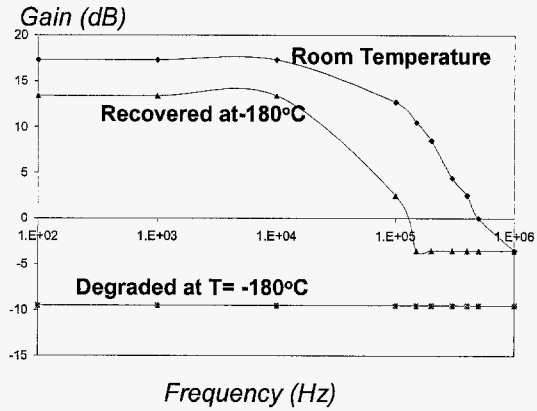


Figure 12: (a) Low-pass filter frequency response as temperature goes down to -180°C; (b) partial recovery at -180°C.

Similar behavior was observed at high temperatures (120°C).

5.2 – First Order Low Pass Filter

The first order low-pass filter shown in Figure 7 was placed in the low-temperature chamber. Figure 12.a displays the frequency response of the filter at different temperatures. It can be observed that the filter response deteriorates below -120°C.

A functionality recovery was attempted through a manual local search over the two bias voltages Vb1 and Vb2 at -180°C. Vb1 and Vb2 were initially at 0.9 and 0.7V respectively. It was observed that a simple change in Vb1 from 0.9V to 0.8V produced a partial recovery in the circuit functionality. This is shown in Figure 12.b.

Even a simple manual recovery method already indicates that this low-pass filter behavior can be recovered at low-temperatures through bias voltage adjustment. Similar results were achieved at high temperatures (120°C).

After the Evolutionary Processor is integrated to the RAA, the recovery process will be implemented by a more powerful search algorithm with potentially better results.

6. Conclusions

The preliminary experiments showed that the functionality of building blocks such as WRTA and first order filters can be recovered at very low temperatures (-180°C) through bias voltage adjustment.

The next step will be the demonstration of the recovery of more complex filters at extreme temperatures from –180 to 120°C. The RAA chip will be integrated with the Evolutionary Processor (FPGA), which will run some kind of Evolutionary Algorithm to search over a set of Vbias values to achieve function recovery. The overall system will be exposed to extreme temperatures.

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