Lead-free vs Tin-lead Reliability of Advanced Electronic Assemblies

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory, California Institute of Technology
Pasadena, CA
Reza.Ghaffrian@JPL.NASA.Gov, (818) 354-2059

This presentation will provide the technical background and specific information published in literature related to reliability test, analyses, modeling, and associated issues for lead-free solder package assemblies in comparison to their tin-lead solder alloys. It also presents current understanding of lead-free thermal cycle test performance in support of IPC 9701A*, Appendix B recently distributed for balloting.

* IPC 9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," Published by IPC, Association Connecting Electronics Industries

Jet Propulsion Laboratory
National Aeronautics & Space Administration
California Institute of Technology

Lead-Free vs Tin-Lead Reliability of Advanced Electronic Assemblies

by

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
(818) 354-2059
Reza.Ghaffarian@JPL.NASA.Gov

Outline

JPL

- Lead Free
  - Current status/Issues
  - Package/Board
- Assembly Reliability
  - Literature data
  - Board integrity/Solder structure after reflows
  - Thermal/Mechanical cycles
- IPC Package Specifications
  - IPC 9701-9706
  - IPC 9701A- Appendix B "Lead-free Guidelines"
- Conclusions

Reza Ghaffarian

Pb Free: Current Status

- Why?
  - "Green" Marketability/Reputation Advantage
  - WEE & Other Legislation (Waste from Electrical & Electronic Equipment)
  - Numerous products worldwide
- Lead Free SAC **(Sn 3.9Ag0.6Cu)**
  - NEMI/IDEALS/JEIDA investigations
  - Min reflow temp 235°C (melt 217°C)
  - Relatively minimum issues with existing package/assembly
- Package Finish Issue (Tin Whisker)
  - Matte tin (low organic content, grain>1 μm)
- Assembly Reliability
  - Minimum data & scatter
  - Inspection criteria redefinition
  - Mixed Pb free & Pb
  - Aassembly/Rework issues

NEMI: National Electronic Manufacturing Initiative
IDEALS: Improved Design Life and Environmentally Aware Manufacturing of Electronic Assemblies
JEIDA: Japan Electronics Industries Development Association
NCMS: National Center for Manufacturing Science

Raja Thaffarian

Pb vs Pb Free

- Tin-lead Characteristics
  - Long history of usage
  - Pb provides ductility in SnPb, no IMC
  - Pb lowers the surface and interfacial energies
  - PbSn angle on Cu, 11° , Sn on Cu 35°
  - PbSn melt is 183°C, reflow 210°C
  - 95Pb5Sn, reflow 350°C, narrow gap 10°C (liquidus/solidus)
- Lead Free
  - Eutectic of Sn with noble metals, Ag, Cu, Au, Bi, etc.
  - Microstructure, mixture of Sn and IMC, e.g Ag_3Sn, plate like
  - Pb-free angle on Cu, 30-45°
  - Higher temperature melt, e.g. SAC **(Sn 3.9Ag0.6Cu)**
  - SnAu, high temp/secondary package, eutectic melt temp 280°C
  - Sn: Whisker, Pest, Cry

Raja Thaffarian

Pb Free: Lead Free Recommendations

- NEMI
  - **Sn3.9Ag0.6Cu**
- European IDEALS
  - **Sn3.8Ag.7Cu**
  - Sn/Ag/Cu & Sn/Ag/Bi + additives
- Japan JEIDA
  - **Sn3.5Ag.75Cu**
  - Sn2Ag.75Cu3Bi, Sn2Ag4Bi.5Cu.1Ge, Sn3Ag3Bi, Sn3.5Ag, Sn3.5Ag2.5Bi2.5In
- NCMS
  - Sn/58Bi, Sn3.5Ag4.8Bi, Sn3.5Ag

Rajen Bhattacharya

Pb Free: Board/Assembly

- Board
  - CTFs varied with surface finish
  - OSP surface finish better than ENIG
  - Multiple reflows (double-sided, rework)
  - Tg for higher reflow exposure
  - Thickness, Warpage, Solder mask, etc.
  - PTH/Microvia integrity/Reliability with high temp. exposure
- Assembly
  - Paste print, similar?
  - Solderability is reduced
  - Voids increase specially with tin-Lead components
  - Pb contamination, 0.1%, strength OK, fatigue/strain reduced, higher than Pb/Sn

Rajen Bhattacharya

Pb Free: Assembly Reliability

- CBGA (IBM)
  - Model, SAC about 2.5 times better (0/100°C)
  - Test results: depends on cycle profile
- BGA 324, 1mm pitch (Motorola)
  - -50/150°C, early trace failure at neck, 1.6 times improvement
  - -40/125°C, no early failure, 1.3 times improvement
  - Failure depends on DNP, not die, thick substrate?
- BGA/CBGA (NEMI)
  - 256 BGA equivalent (-40/125°C)
  - 256 CBGA Better (0/100°C)
- LCC 24 (Swiss Federal Institute)
  - (-20/120°C)- less resistance
- Flip chip with underfill
  - SAC slightly lower, underfill optimization (Auburn)
  - SAC lower (Fraunhofer Institute)

Pb Free: NEMI Conclusions

- Thermal Cycle Results (-40/125°C, 0/100°C)
  - Lead-free only, are equivalent or better
  - Mixed
    - Most equivalent
    - Two worse
    - One better
- Three point bend
  - No differences
- No Electrochemical Migration, IPC-TM-650
- Tin Whisker being investigated
- Many Issues Remain
  - Board ability to withstand higher temp.
  - Component lead finish (tin whisker)
  - Reliability model

Pb Free: Rework Issues JPL

- Rework
  - Thermal profiling
  - Removal of defective parts
  - Site redressing
  - Solder replenishment or flux application
  - New part placement
  - Reflow soldering
- Higher temp for Pb free
  - New equipment?
  - Requires both higher reflow temp. and more time at reflow
  - Damaging on board (pad lift, solder mask,etc.)/adjacent parts
  - Excessive intermetallic growth, cross-contamination
  - Difficult to remove residual solder
- Assembly robustness change by rework
  - Collapse more
  - Loss of self alignment
- Generally lower reliability

Roger Shaffstall

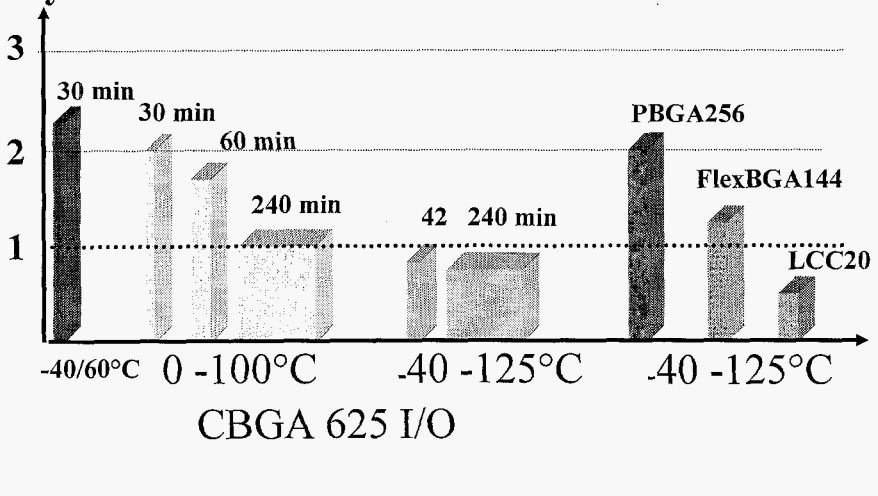
Pb Free: Key Package Issues JPL

- Lead-free require higher temp. reflow (240-260°C)
- Materials properties, e.g. Tg more critical
- Package design
- Die attach
- Flip chip, temp. hierarchy
- MSL (moisture sensitivity level –IPC/JEDEC)
  - 250°C reflow, reduced at least one level, 144LQFP, PBGA- 2 layers
  - 260°C reflow, reduced one or two levels, 2 levels ⇓ for PBGA-4 layers
- Isothermal shear strength
  - Longer life for the same damage level
- Termination finish
  - Tin whisker

Roger Shaffstall

9/10

Relative CTFs Pb Free/Pb



IPC Qual Specs-I

- IPC 9701, Released Jan 2002

"Performance Test Methods and Qual Requirements for SMT"

  - Details on Thermal cycle test and acceptance
  - IPC 9701A- Lead free requirement

- IPC-JEDEC 9702- Released July 2004

"Monotonic Bend Characterization of Board-Level Interconnects"

  - Details on bend test to detect failure due handling, probe test, etc.

- IPC 9703, Draft August 2004

"Mechanical Shock Test Methods and Qual Req for SMT"

  - Details on mechanical shock and drop tests
  - Increase load/drop levels to failure
  - Use specific requirement

11/12

IPC Qual Specs-II

JPL

- IPC 9704, Final Draft Feb-Release July 2005

"PWB Strain Gage Test Guidelines"

  - Solder joint failure due to mechanical loading during probe test
  - Limited to static load, dynamic will be covered later

- IPC 9705, Initial Draft Feb 2005

"Area Array Connector Testing and Reliability"

  - IPC 9701 and additional specific requirement for connectors

- IPC 9706, Initiated Oct 2004- Approved

"Guidelines on Lead-free Implementation for High Reliability Applications"

  - Data being generated by NASA-DOD-Industry on lead-free
  - Reliability data by industry
  - Plots removed from IPC 9701A-lead-free spec

Reza Ghaffarian

Lead-free Guideline- IPC 9701A-Appendix B

JPL

- IPC 9701A, 2nd draft to team July 2005, Oct final draft
- Appendix B, "Guideline for Thermal Cycle Requirements for Lead-free Solder Joints"
  - Moisture sensitivity, use J-STD-020
  - Reference to several models
    - Details covered in IPC 9706
    - Paper to be presented at APEX 2006 by R. Ghaffarian
- Release delayed due to lack of data on dwell- 2 dwells
  - D10 (10 minute dwell)
    - Most efficient
    - Use as "stand-alone", only when modeling understood could be theoretically compared to tin-lead
  - D30+ (30 minutes or higher)- To experimentally induce damage somewhat comparable to tin-lead
- Surface finish
  - Only OSP
- Requalification is required when
  - Solder paste change
  - Lead terminal change

Reza Ghaffarian

CTFs: Summary

JPL

Package Type

- SAC is less for: LCCC, Resistor, Alloy 42 TSOP, CBGA?, PTH?
- SAC is better for: PBGA, CSP?

Thermal Cycle Profile

- Creep (> 0.5 T/Tm), Tm differ from Pb/Sn

CTFs

- SAC lower Beta (wider spread), CTFs depend on risk level
- SAC: Acceleration factor differ from Pb/Sn

So, no absolute ranking!!

Raja Thaffuriun

Acknowledgments

JPL

The research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

The author would like to acknowledge those at JPL and industry, especially IPC 6-10 task team members for their continuous support and discussions on this topic. The author extends his appreciation to program managers at NASA Electronic Parts and Packaging Program (NEPP) including Michael Sampson, Dr. Charles Barnes, and Phillip Zulueta for their continuous support and encouragement.

Raja Thaffuriun