CMOS Active Pixel Sensor Technology and Reliability Characterization Methodology

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Abstract: This paper describes the technology, design features and reliability characterization methodology of a CMOS Active Pixel Sensor. Both overall chip reliability and pixel reliability are projected for the imagers.

Keywords: CMOS Active Pixel Sensors; Imaging Sensor Reliability; Pixel Reliability.

Introduction

Imaging sensors of different varieties are widely used in commercial and scientific applications. CMOS active pixel sensor (APS) imagers are fabricated in standard CMOS processes, which make it possible to integrate the timing and control electronics, sensor array, signal processing electronics, analog-to-digital converter (ADC) and full digital interface on one chip. This helps to achieve a cost-effective highly integrated and highly compact imaging system, i.e. camera-on-a-chip, by utilizing the same design techniques that have been developed over the years for low-power CMOS digital and analog circuits.

A CMOS active pixel imaging sensor was designed by Jet Propulsion Laboratory and manufactured by a standard commercial CMOS production line for space applications. A qualification methodology and reliability analysis approach for imaging sensors has been also developed to include both overall chip reliability and pixel reliability, which is directly related to imaging quality and provides sensor reliability information and performance control.

It should be noted that the environmental, mechanical and packaging evaluation procedures and tests are also part of the qualification plan and practice, but are not addressed herein. In addition, the impact of radiation on the imagers - including Gamma, protons and heavy ions - were presented in.

CMOS Active Pixel Sensor

APS Technology: The image sensor is photodiode-type CMOS active pixel sensor imaging system on chip, designed by Jet Propulsion Laboratory and manufactured by a standard commercial CMOS production line. The imager is a 512 by 512 photodiode pixel array, which can randomly access any window in the array from 1 pixel by 1 pixel all the way to 512 pixels by 512 pixels in any rectangular shape. The minimum interface consists of five wires: Vdd, Ground, Serial Data Input, Serial Data Output and Clock. The imager size is approximately 10 mm by 15.5 mm with pixel size of 12 um by 12 um. The nominal power supply Vdd is 3.3V.

Figure 1 gives a schematic of the photodiode-type active pixel sensor cell. In the pixel sensor cell, the transistors designed for the imagers in our study have a minimum channel length of 0.5um.

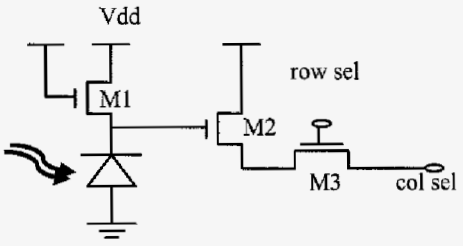

Figure 1. Schematic of the photodiode-type active pixel sensor cell.

Light into the photo-diode generates a small current proportional to the light intensity and photo-diode area. Due to this small photo current, the nMOS transistor (M1) operates in weak inversion. In this region, the gate to source voltage depends logarithmically on the drain current with a constant slope independent of the technology and equal to kT/q, as shown in the following simplified expression for the gate-source voltage for a transistor working in its weak inversion region:

$$V_{gs} = \frac{kT}{q}\ln\left(\frac{L}{W}\frac{I_d}{I_{d0}}\right) + V_{th}$$

where V_{gs} is the gate-source voltage, I_d is the drain current or the photo current, I_{d0} is the I_d at the on-set of weak inversion, W and L are the width and length of the channel of the transistor, T is the temperature in Kelvin and k is the Bolzmann constant. Therefore, the pixel structure yields a continuous signal that is proportional to the instantaneous light intensity.

CMOS Active Pixel Sensor Reliability

Experiment Details: Accelerated testing was performed on the image sensors at elevated bias and temperature levels to accelerate thermally activated failure mechanisms. The image sensors were stressed in parallel and stopped in a pre-set time interval to be monitored one by one for Dark Rate, Linearity, Dark Current Non-Uniformity (DCNU), Fixed

Pattern Noise (FPN) and Photon Response Non-Uniformity (PRNU).

Fixed pattern noise (FPN) is the variation from pixel to pixel when the imager operated as normal with no light input. The FPN is typically measured using the full array. Photon Response Non-Uniformity (PRNU) is the gain difference between pixels and it is typically taken with a field at approximately 50% of full well. Dark Current is the thermally generated electrons discharging the pixel just as if a photon had hit the pixel. Dark Current Non-Uniformity (DCNU) is the leakage difference between pixels with a dark field over a long integration time. All these parameters are functions of temperature and measured during the accelerated testing. Also, Dark Rate and Linearity, defined as the mV/s from Dark Current and PRNU measurements, respectively, were also monitored.

It is very important to ensure that the highest stress temperature cannot exceed the glass transition temperature for the die attach material of the packages, in our case, 117°C. At the same time, the highest stress voltage at each stress temperature should be within the range when the sensor is still framing and functional. The highest voltage that can be applied on the imager when it is still framing was simulated as 6.8V, later confirmed by experiment. The stress conditions were determined as 6.5V at 85°C, 6.5V at 45°C, and 6.0V at 85°C to estimate voltage acceleration factor and activation energy. The total testing sample size was 18 with 5~6 imager sensors for each accelerated stress condition.

During the accelerated testing, the sensors were running at 5 MHz with the clock pulse matching the stress voltage applied on the chips. A green LED carefully designed and tuned on each testing board served as the light source within the chamber for Linearity and Photon Response Non-Uniformity measurements. A typical clock frequency during the mission operating condition is 4MHz.

The imagers were first characterized under each stress temperature condition to determine an appropriate integration time. The integration time was chosen to be 30ms during FPN and PRNU measurements to represent the mission operating condition. The integration time during dark rate and Linearity measurements was chosen long enough for the imagers to reach saturation region for a full characterization of the imaging response.

Chip Reliability Projection: For overall APS chip reliability, Linearity and Dark Rate are the two parameters to be considered since they reflect the overall parametric shift or change on the imaging chips.

Figure 2 shows the linearity characteristics for the worst case chip as a function of stress time. The black symbol indicates the response at time zero while the white symbol indicates response at the end of stress testing. The characteristics trend is representative for all imaging chips under all stress conditions.

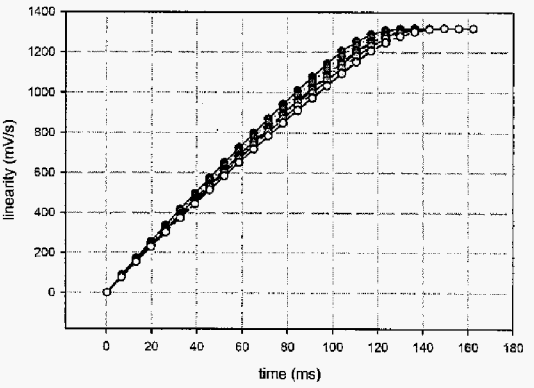

Figure 2. Linearity changes with stress time, black symbols indicate time zero, white symbols indicate at the end of stress.

Figure 2 indicates that it took a longer integration time to achieve saturation when the device was degraded. This information can be also presented by the slope of the linearity curves before the saturation points. The percentage of the slope change of the linearity curves in Figure 2 is plotted in Figure 3, showing almost linear increasing Linearity slope versus stress time in a log-log scale.

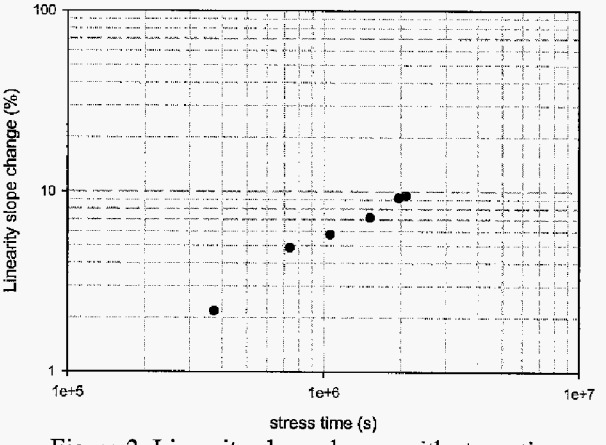

Figure 2. Linearity slope change with stress time.

The behavior of the dark rate is similar to that of Linearity but with smaller degradation rate. Figure 4 shows a representative change of the dark rate slope as a function of stress time in a log-log scale.

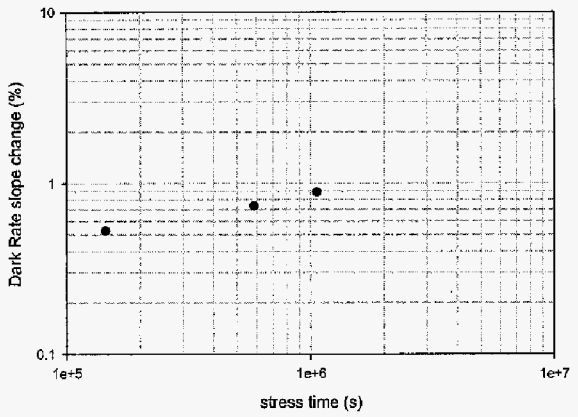

Figure 4. Dark rate slope change with stress time.

Since the Dark Rate and Linearity can indicate the overall sensor performance, the sensor's overall chip reliability can be projected based on the Dark Rate and Linearity degradation.

Assuming the Arrhenius model, $t_{\%} \sim e^{\beta V_o} e^{E_a/kT_o}$, where $t_{\%}$ is the chip life time at certain failure fraction and is determined to be 0.1% in our case; β, V_o, E_a, k and T_o are the voltage acceleration factor, operating voltage, activation energy, Boltzmann's constant and operating temperature in Kelvin, respectively.

The voltage acceleration factor and activation energy were estimated as 0.73 dec/volt and 0.7eV, respectively, for worst case imaging chips. Using 10% degradation for Linearity as the chip failure criterion, the chip life time at 3.3V, 27°C is over 112 years at 0.1% failure fraction with average failure rate of 1 FIT. Life and failure rate can be also generated by using a percentage degradation of Dark Rate as well.

It should be noted that the "failure" criteria used in this reliability projection is defined as a certain level of parametric shifting. Even though this parametric shifting does indicate some performance degradation of the imagers, it is worthwhile to note that the imagers still frame and function very well when the Dark Rate and/or Linearity reaches 10% parametric degradation. In order to estimate life and failure rate associated with the "imaging failures", pixel reliability needs to be projected.

Pixel Reliability Projection: Chip reliability projection indicates reliability for a sensor's overall performance as a function of operation time, but it is difficult to relate it to image quality. Therefore, pixel reliability needs to be considered and projected as well.

The Dark Current Non-Uniformity, Fixed Pattern Noise and Photon Response Non-Uniformity measurements during the accelerated testing recorded the distributions of the photodiode reference voltage for each pixel as a function of stress time, in order to calculate the time-dependent DCNU, FPN and PRNU values.

During the accelerated testing, some of the pixels get "hotter", i.e. leak more than nominal pixels. In addition, the standard deviation of the pixel distribution increases slightly with worst case of 2% change, and the median of the distribution eventually shift.

Based on our sample size of 20 CMOS active pixel sensors (18 for accelerated testing and 2 for characterization testing) with 512 by 512 pixels on each imager, we found that the "hot" pixels tend to be randomly distributed across the pixel array and no signature of the pattern can be found. This may indicate that the imaging chips do not have evident process-related defects or stress-induced weak-link pixels. The hot pixel generation rate is slow at the accelerated stress levels. Based on the limited data, the estimated hot pixel generation rate is approximately one and one-half pixel per decade at 6V 85°C, which gives a rather long projected imager life, assuming a few hot pixels do not have a severe impact on imaging quality. Hot pixels do not seem to induce neighboring pixel to degrade faster. Hot pixels can cause image problems but with a proper refreshing scheme, the impact of hot pixel on imaging quality can be significantly reduced.

The change in standard deviation of the pixel distribution seems to increase faster at the beginning of the accelerated stress conditions and then saturates at about 2% to 3% change. However, due to the limited data sets and small sample size in our study, no further conclusion can be made on the behavior of the standard deviation change.

When the pixel distributions under DCNU, FPN and PRNU measurements have shifted and/or the standard deviations have changed, it indicates a change in black-white scale for imaging. Therefore, by scaling the time-dependent pixel distribution against the initial pixel distribution, images can be generated either by real pixel distribution data or by projected pixel distributions.

The pixel distributions for DCNU, FPN and PRNU did not have significant shift during our accelerated testing. This can be expected since the minimum channel length of the active transistor inside the pixel cell is rather "long", i.e. 0.5 um. Therefore, based on the trend of pixel degradation, the projected pixel distributions can be and needed to be generated to simulate the image quality.

Figure 5(a) shows an original image of Saturn. Figure 5(b), (c) and (d) are the simulated images with 10%, 15% and 20% median pixel degradation, respectively. The degradation on the imaging quality can be seen very clearly from these Figures, thus a so-called "imaging failure" can be determined based on the series of images. For example, if

Figure 5(b) is regarded as an imaging fail, a 10% median pixel degradation is then chosen as the failure criterion. In this case, the imager life is at least an order of magnitude longer than the projected imager life using 10% Linearity degradation.

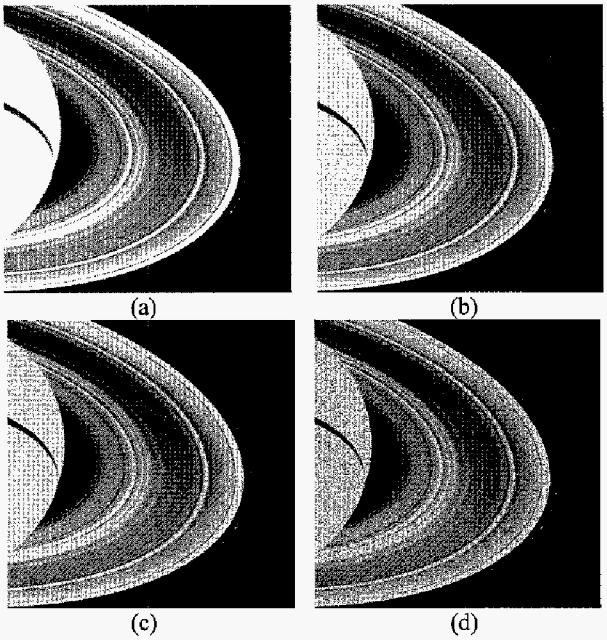

Figure 5. (a) Original image of Saturn; (b) Image with 10% pixel degradation; (c) Image with 15% pixel degradation; (d) Image with 20% pixel degradation.

Another failure mechanism results from the read-out or I/O circuitry. It happens rather suddenly when the imager stops functional totally. Competing with the pixel degradation, which is a relatively slower process, periphery circuitry failure may be much more severe since it will cause a hard failure of the imager. This happened during radiation testing when the imager failed in a sudden owing to the periphery circuit failure.

The pixel reliability is a function of acceptable image quality level and depends on the pixel responses to darkness and light. Acceptable image quality can be chosen based on the same experimental data or simulation results using small degradation percentage increases. It should be noted that the reliability projection based on the worst case parameter degradation, i.e. linearity degradation, gives a much shorter lifetime prediction compared to the pixel projection. Therefore, pixel reliability cannot be overlooked during imaging sensor qualification.

Summary

The technology and design features of a CMOS active pixel imaging sensor, designed by Jet Propulsion Laboratory and manufactured by a standard commercial CMOS production line, are presented. The imager is a 512 by 512 photodiode pixel array, which can randomly access any window in the array from 1 pixel by 1 pixel all the way to 512 pixels by 512 pixels in any rectangular shape.

A qualification methodology and reliability analysis approach for imaging sensors has been also developed and described. In addition to overall chip reliability characterization based on sensor's overall figure of merit, such as Dark Rate, Linearity, Dark Current Non-Uniformity, Fixed Pattern Noise and Photon Response Non-Uniformity, a reliability simulation technique is proposed to project pixel reliability, which is a function of acceptable image quality level and depends on the pixel responses to darkness and light. Acceptable image quality can be chosen based on the same experimental data or simulation results using small degradation percentage increases. The projected pixel reliability is directly related to imaging quality and provides additional sensor reliability information and performance control.

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