Embedded Resistors and Capacitors in Organic and Inorganic Substrates

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Abstract—Embedded resistors and capacitors were purchased from two technologies; organic PWB and inorganic low temperature co-fired ceramic (LTCC). Small groups of each substrate were exposed to four environmental tests and several characterization tests to evaluate their performance and reliability. Even though all passive components maintained electrical performance throughout environmental testing, differences between the two technologies were observed. Environmental testing was taken beyond manufacturers' reported testing, but generally not taken to failure. When possible, data was quantitatively compared to manufacturer's data.

Both technologies performed favorably with some nuances noted for each material set. The resistors were not embedded deep into the substrate structures but were placed on the surface and coated. This served two purposes: the first was that resistors could later be trimmed if they reside on the surface and the second was that it represented worst case for protection of the resistive elements for the reliability testing, mainly moisture exposure. Typically, the PC board solder resist is sufficient to protect the resistors in the PWB resistors. Should there be a pin-hole or damaged area, the environmental protection could be compromised. During the moisture environmental testing, a resistor in the PWB technology failed due to corrosion. The level of concern for this failure mechanism is elevated only for laser trimmed resistors where the coating would be opened and an additional coating is applied following the adjustment. The failed resistor in this study failed at the 1000 hour readpoint of 85%RH/85°C and the failure was not an open but an increase in resistance.

The capacitors exhibited a size relationship to reliability where small capacitors varied in capacitance more than large capacitor sizes selected in this study. The best physical size for the capacitors was found to be between 1 and 2 cm on a side.

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1. INTRODUCTION

Passive components generally refer to electrical components without gain or current-switching capability such as resistors, capacitors and inductors. A majority of the passive devices used in electrical circuitry today are directly mounted on the surface of a printed circuit board (PCB) and are referred to as surface mount passives. Such passives can account for 80%-95% of the total number of circuit components and can consume up to 40% of the surface area of the PCB. [1, 2]

Embedded passives are passives that have been integrated within the printed circuit board, or substrate material. This embedding can take place on a single layer of material, a combination of material layers or even can be achieved by placing a component within a cavity in a substrate.[3] Common embedded substrate materials include, but are not limited to ceramic, silicon, polyimide and FR-4 boards. Research into embedded passives technology originated from the demand for new devices with smaller size, less cost and more features. Although capacitors, resistors and inductors are all candidates for embedding, the greatest interest is currently focused on

capacitors and resistors.[1] By embedding such passive components within the substrate material it becomes possible to create smaller circuit boards. Embedded passives also make it possible to shorten the distance between the passive components and the active components in a circuit assembly. By shortening this distance the circuit receives better signal transmission producing less noise which leads to better electrical performance. [1, 2]

This work utilized thirty (30) printed wiring boards (PWB) and fourteen (14) low temperature co-fired ceramic (LTCC) substrates embedded with resistors and capacitors that were designed/layed out at JPL and purchased for the purpose of assessing reliability of these two technologies in the embedded passives subject area. [1] The goal of this task was to investigate the integrity of embedded components (specifically capacitors and resistors), as well as to evaluate the reliability of the PWB substrates and the LTCC substrates that the components are embedded within. This was accomplished by dividing the substrates into sub-groups and then subjecting each sub-group to a specific environmental stress test. If technology of this sort is found to be reliable, it will allow NASA Programs and Projects to reduce the weight and size required for electronics assemblies within systems by building functioning circuitry into PCB's and/or substrates using embedded passives. [1] A description of the two types of substrates used in this evaluation below:

2. PRINTED WIRING BOARD (PWB)

A printed wiring board is the platform upon which electrical components and devices are mounted. A PWB is not only the physical structure for mounting, but is also the interconnection between components. [4] The printed wiring boards used for this study were organic polyimide boards. The embedded components used in the manufacture of this board are commonly used in the PC board industry, but not many high-reliability PCB shops combine both resistors and capacitors in the same structure. This task was a continuation of last year's NEPP task where a survey was conducted to obtain a record of board shops that could build embedded resistors and capacitors in the same substrate. Boards were then designed and manufactured by selected shops. See Figure 1 below that illustrates the PWBs used in this study:

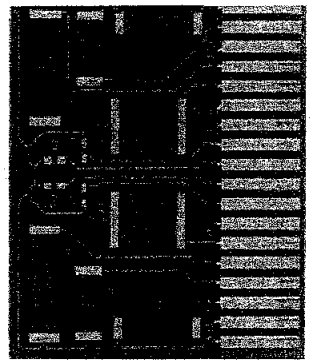

Figure 1 - Photo of PWB substrate with Embedded Resistors and Capacitors. The visible components are the surface resistors. Dimensions of the substrate are 1.5"x 1.8"x .062"

The embedded resistors were designed using the material Ohmega-Ply manufactured by Ohmega Technologies. [1] This material has been in production for decades and has been widely used in the Aerospace Industry. The PWB substrates contain 24 embedded resistors (12 per side). The resistors reside on the surface of the PWB and are covered by the solder resist, as recommended by the manufacturer for environmental protection. The Ohmega-Ply material allows for the resistors to be placed on any layer of the board. The main advantage to placing the resistors on the surface of the PWB is that they can then be laser trimmed to a tighter tolerance. Resistors placed on the interior of the PWB do not allow this luxury. Since many of NASA's future uses will require more precise resistor tolerances, these test PWBs were designed with the resistors on both surfaces, protected only by the solder mask. This also represents a worst case situation as far as the coverage and environmental protection of these devices.

Ohmega Technologies informed the design team of the fact that there is a slight resistance difference due to preferential grain structure orientation caused by the manufacturing process in the raw material. Therefore, the resistors layout and design were chosen based on resistor size and orientation (x and y) on the relatively small PWB. It was hoped that any difference in orientation could be quantified and the reliability assessed by designing the PWB in such a manner. The resistor dimensions can be seen in Table 1. The ratio column describes the number of squares in the resistor (3 squares of 50Ω/□ would yield a resistor of 150Ω, while a resistor made of a ratio of ½square would yield a resistor of 25Ω). The year end report for the FY'03 work described the resistor values measured on these substrates in more detail.

Table 1. Informational table for Ohmega-Ply resistors

Resistor sizes for Ohmega Ply
Largest Length = 0.500"
Smallest Length = 0.020"

#	Orientation	Ratio	Length (in)	Width (in)	Area (in^2)	Area (mils^2)
1	x	3	0.500	0.167	0.08333	83333.33
2	x	2	0.283	0.141	0.04000	40000.00
3	y	1	0.289	0.289	0.08333	83333.33
4	y	1	0.289	0.289	0.08333	83333.33
5	y	3	0.346	0.115	0.04000	40000.00
6	x	2	0.283	0.141	0.04000	40000.00
7	y	1/2	0.020	0.040	0.00080	800.00
8	y	3	0.346	0.115	0.04000	40000.00
9	x	1	0.028	0.028	0.00080	800.00
10	x	1	0.028	0.028	0.00080	800.00
11	x	3	0.500	0.167	0.08333	83333.33
12	y	1/2	0.020	0.040	0.00080	800.00

There are 10 capacitors embedded within the subject PWB substrates. The capacitors are made of a material called Interra HK04 manufactured by DuPont. [1] The capacitor material comes as two parallel copper sheets laminated on both sides of a polyimide sheet (the dielectric of the capacitor plate). During the manufacture of the PWB this material is laminated to the PWB material (FR-4 or as in this case, polyimide) and then subtractively etched to form the parallel plate capacitor. Connection to each plate can be made by vias or copper traces. This technology is limited by the relatively low capacitor value created by the material set. Therefore, it is typically used as a large capacitive plane inside of a PWB which is connected to form another level. The capacitor dimensions used in this study are small in size and value but were designed to illustrate what limitations, if any, the material exhibited. The year end report for the FY'03 work described the capacitor values measured on these substrates in more detail. The capacitor layout/design can be seen in Table 2 that follows:

Table 2: Information Table for capacitors

Capacitor Sizes
Largest Length = 0.75"
Smallest Length = 0.04

#	x & y Length (in)	Area (in^2)	Area (mils^2)
1	0.75	0.5625	562500
2	0.51	0.2601	260100
3	0.51	0.2601	260100
4	0.28	0.0784	78400
5	0.28	0.0784	78400
6	0.16	0.0256	25600
7	0.16	0.0256	25600
8	0.04	0.0016	1600
9	0.04	0.0016	1600
10	0.04	0.0016	1600

3. LOW TEMPERATURE CO-FIRED CERAMIC (LTCC)

Low temperature co-fired ceramic substrates are an alternative to PWBs that offer increased reliability, cost efficiency for high volumes, and high packaging density. LTCC has large benefits in microwave applications. The LTCC manufacturing process starts with a slurry mixture of recrystallized glass and ceramic powder in binders and organic solvents. It is then cast under "doctor blades" to obtain a desired tape thickness. The dried tape is then coiled on to a carrier tape and is then ready for production. The metallization pastes are screen printed layer by layer upon the un-fired or "green" ceramic tape. Then the un-fired ceramic layers are stacked and laminated under pressure. Next, the multilayer stack is fired during the final manufacturing step. The firing temperature is around 900°C for the LTCC glass-ceramic substrate materials. The melting point of the gold metallization is 960°C. The LTCC substrates used for this investigation were manufactured using the Ferro A6M material with gold interconnect metallization. [1] The dielectric in Ferro A6M LTCC tape is a calcium borosilicate, crystallizing glass. The A6-M has a dielectric constant of 6 and very low dielectric loss (<0.002 @10GHz). These ceramic substrates and the gold, copper or silver pastes have excellent physical and electrical properties. See Figure 2 below for a photo of the LTCC substrate used in this study.

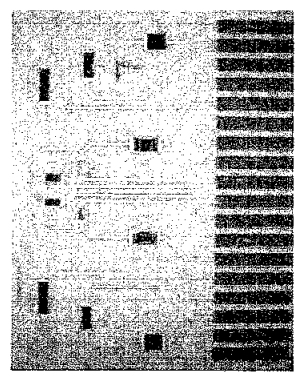

Figure 2 - Photo of LTCC substrate with Embedded Resistors and Capacitors. The visible components are the surface resistors. Dimensions of the substrate are 1.5"x 1.8"x .062"

As was the cause with the PWB substrate, the LTCC substrates contain 24 embedded resistors (12 per side) which exist on both the top and bottom surfaces. These resistors were chosen based on size and orientation, much like the PWB substrates. Even though the substrate design is laid out experimentally like the PWB substrate, the embedded resistors are constructed by a very different method. The LTCC resistors are made of thick-film resistor pastes which commonly consist of conductive powders, insulating glass, crystalline powders and an organic matrix that holds it all together. [5] After firing,

the thick-film paste can be considered as chains of conductive particles in a "sea" of glass. It has been found that the glasses in the thick-film resistor pastes tend to interact with the tape glass. This phenomenon causes a shift in the ratio of resistive particles and results in different square resistance and TCR values. [6] The resistor dimensions can be seen in Table 3 on the following page:

Table 3: Information table for LTCC resistors

Resistor Sizes for LTCC
Largest Length = 0.100"
Smallest Length = 0.010"

#	Orientation	Ratio	Length (in)	Width (in)	Area (in^2)	Area (mils^2)
1	x	3	0.100	0.033	0.00333	3333.33
2	x	2	0.059	0.030	0.00175	1750.00
3	y	1	0.058	0.058	0.00333	3333.33
4	y	1	0.058	0.058	0.00333	3333.33
5	y	1/3	0.024	0.072	0.00175	1750.00
6	x	2	0.059	0.030	0.00175	1750.00
7	y	½	0.010	0.020	0.00020	200.00
8	y	1/3	0.024	0.072	0.00175	1750.00
9	x	1	0.014	0.014	0.00020	200.00
10	x	1	0.014	0.014	0.00020	200.00
11	x	3	0.100	0.033	0.00333	3333.33
12	y	½	0.010	0.020	0.00020	200.00

A capacitor is comprised of two conductors separated by an insulator. In the case of the LTCC substrates, the capacitors are formed by screen printing two gold conductors with a layer of green tape (Ferro A6M) separating the two parallel plates, subsequently co-fired. The capacitor layout and dimensions are the same for the LTCC substrates as for the PWB substrates because the conductor plates and substrate sizes can be the same in physical size.

4. ENVIRONMENTAL TESTING

Small sub-groups of each substrate were exposed to four environmental test conditions to evaluate performance reliability. Reliability of the embedded components was monitored by electrical performance (resistance, capacitance, and dissipation factor). The substrates were also monitored physically by inspection conducted by the CSAM (C- mode Scanning Acoustic Microscopy) test. By subjecting the substrates to various environmental stresses and checking for change in electrical performance it was possible to observe trends in embedded passive performance reliability as well as trends in the material reliability of the substrate. The environmental tests performed included:

- Thermal Coefficient of Resistance/Capacitance
- Thermal Aging
- Humidity Exposure
- Thermal Shock

Initial electrical measurements were taken at room temperature after the substrates were received. The measurements were taken on a Hewlett Packard 4263A LCR Meter. Measurements included resistance and capacitance. Initial capacitance and dissipation factor measurements were also taken on a small sample of PWB and LTCC substrates using a QuadTech 7600 Precision RLC Meter.

4.1 THERMAL COEFFICIENT OF RESISTANCE/ CAPACITANCE

The purpose of the thermal coefficient of resistance/capacitance environmental test (TCR/TCC) is to determine the percent change of resistance/capacitance from the resistance/capacitance at a reference temperature, per unit temperature difference between the reference temperature and the test temperature [7].

The TCR/TCC test was performed on 6 substrates (3 PWB and 3 LTCC) using an Air-Jet PAC-TC-44 Thermal Conditioning System. The test was conducted in accordance with MIL-STD-202 Method 304. The substrates were baked at 40°C for 24 hours prior to the beginning of testing and initial measurements were recorded. The test was performed over a range of pre-determined temperatures. There were two series of test temperatures, a cold cycle and a hot cycle with the reference temperature for each cycle being set at 25 °C. The substrates were first run through the hot cycle with read points at 25°C, 50°C, 75°C and 125°C. Next, the substrates were run through the cold cycle with read points at 25°C, 0°C, -25°C and -55°C. Tolerance for the temperature read point was ±3°C. Results were calculated using the following equation: [7]

Resistance/Capacitance-Temperature Characteristic

$$= \frac{R_2 - R_1}{R_1} \times 100$$

Where:
R_1 = resistance at reference temperature (in same series as test temperature) in ohms.
R_2 = resistance at test temperature in ohms.

4.2 THERMAL AGING

The purpose of the thermal aging environmental test is to determine the effect that elevated ambient temperature has on the electrical and mechanical characteristics of a component after a specified amount of time. After completion of the test, components are then examined for deterioration by physical inspection and electrical performance. [8]

The thermal aging test was performed on 8 substrates (5 PWB and 3 LTCC) using a Delta 9023 Rack-Mount Environmental Test Chamber. The test was conducted in accordance with MIL-STD-202 Method 108. The procedure used called for the substrates to remain in the test chamber for 1000 hours at 125°C elevated ambient temperature with a temperature tolerance of ±3°C. Read points for this test were measured at 25°C and taken at 0, 100, 200, 500, and 1000 hours.

4.3 HUMIDITY EXPOSURE

The purpose of the humidity exposure environmental test is to determine the effect elevated temperature and elevated relative humidity has on the electrical and mechanical characteristics of a component after a specified amount of time. After completion of the test, components are then examined for deterioration by physical inspection and electrical performance.

The thermal aging environmental test was performed on 8 substrates (5 PWB and 3 LTCC) using a Blue M Humid Flow Environmental Test Chamber. The substrates were placed in the environmental chamber at 85°C with 85% relative humidity for a 500 hour specified length of time. Read points for this test were taken at 0, 240, and 500 hours.

In addition to the general electrical characterizations done during the humidity exposure environmental test, dissipation factor measurements were performed on the capacitors at a frequency of 1 kHz for each read point.

4.4 THERMAL SHOCK

The thermal shock environmental test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the shock of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. [9] After completion of the test, components are examined for cracking or delamination as well as abnormal electrical characteristics.

This test was performed on 8 substrates (5 PWB and 3 LTCC) using a Delta 9080 Environmental Test Chamber. The test was conducted in accordance with MIL-STD-202 Method 107. The substrates were to cycle through two pre-determined temperature extremes (the low temperature being -65°C and the high temperature being 125°C) for a set number of cycles. Read points for this test were taken at 0, 72, 200, and 500 cycles.
In addition to the general electrical characterizations done during the thermal shock environmental test, dissipation factor measurements were performed on the capacitors at a frequency of 1 kHz for each read point.

5 CHARACTERIZATION

Additional component characterizations were conducted throughout the duration of this project. Additional characterizations were used to achieve a better understanding about the substrates both electrically and mechanically.

5.1 DISSIPATION FACTOR VS. FREQUENCY

Dissipation factor (DF) describes how well a capacitor holds its charge. By measuring the dissipation factor of a capacitor over a range of frequencies it becomes possible to characterize the electrical performance of a capacitor. For this task, the dissipation factor was determined over a range of frequencies from 1 kHz to 2 MHz for one PWB substrate and one LTCC substrate. Due to the fact that DF was measured for only one substrate of each technology; the intention was to determine an indication of the performance of both technologies, not necessarily to fully characterize the two technologies.

The dissipation factor data for all capacitors within the PWB and LTCC substrates are shown in Figures 3 and 12 below. Both data sets suggest that all capacitors in both technologies exhibit DF that stays essentially constant throughout the frequency range measured in this study. The data shows that the capacitors embedded within the LTCC substrates tend to have a lower dissipation factor than the capacitors embedded within the PWB substrates by a factor of 2, suggesting that the LTCC capacitors hold their charge better than the PWB substrates over a range of varying frequencies. However, it is interesting to note that if the three (3) small capacitors (C8, C9 and C10 – see Table 2) were eliminated from the PWB data, the DF data would be more in-line with the LTCC data. More discussion regarding size affects will be covered in the Discussion Section of this document.

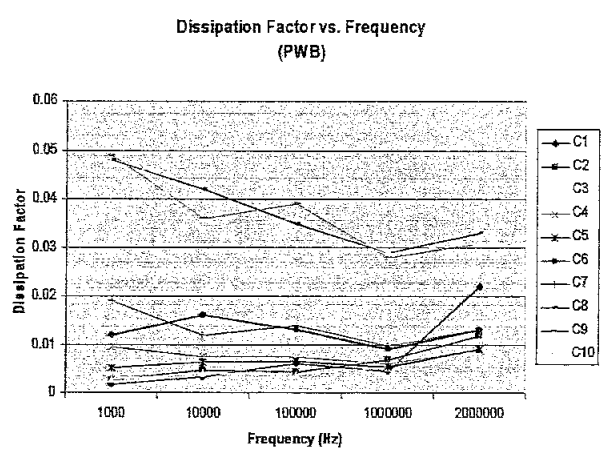

Figure 3 - Dissipation Factor vs. Frequency (PWB)

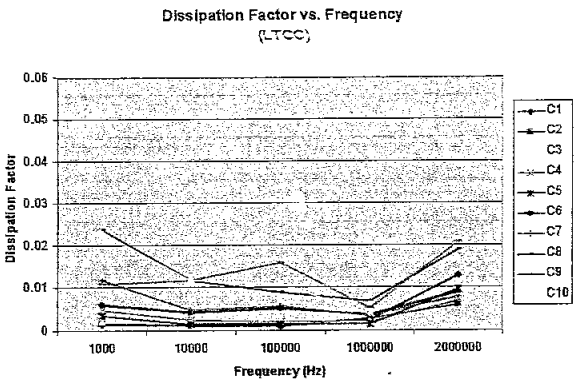

Figure 4 - Dissipation Factor vs. Frequency (LTCC)

5.2 CROSS SECTIONING

Cross sectioning was done for one PWB substrate and one LTCC substrate for the purpose of observing the multilayer design of the embedded components within the substrates. After cross sectioning of the substrates was complete, photos were taken at various magnifications of the embedded resistors and the parallel plates of the capacitors (See Figures 5-116).

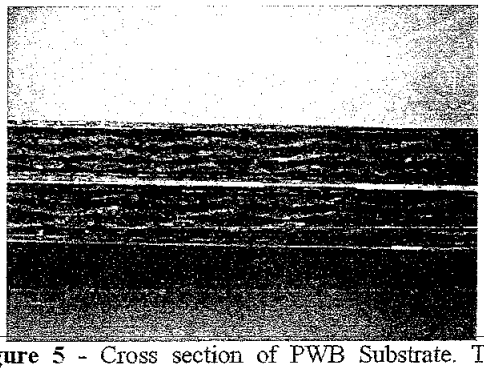

Figure 5 - Cross section of PWB Substrate. The center of the PWB contains the copper parallel Capacitor. The fibers internal to structure of the can also be seen on either side of the capacitor.

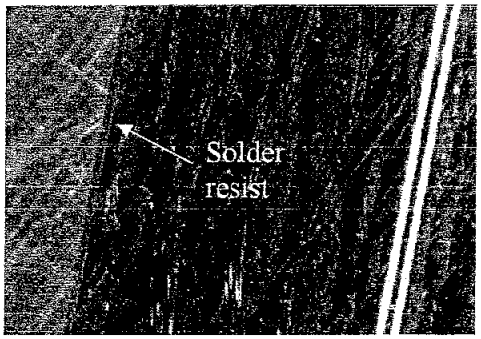

Figure 6 - High magnification of Parallel Plate capacitor (PWB). The edge of the PWB and green solder resist can be seen.

Figure 7 - Cross section of LTCC substrate. The center of the ceramic contains the copper parallel plates of the capacitors.

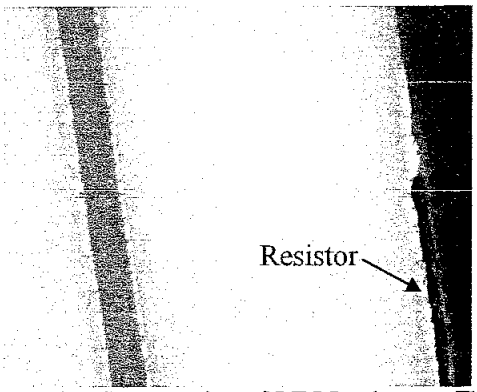

Figure 8 - Cross section of LTCC substrate. The edge of the substrate and resistor can be seen.

5.3 CAPACITANCE VS. FREQUENCY

By measuring the capacitance of a capacitor over a range of frequencies it becomes possible to characterize the electrical performance for a designer to use in a future application. For this task, capacitance was measured over a range of frequencies from 1 kHz to 2 MHz for one PWB substrate and one LTCC substrate. Again, the intention was to determine an indication of the performance of both technologies not necessarily fully characterize the two technologies.

The capacitance vs. frequency data can be seen for both the PWB and LTCC substrates in Figures 9 and 10 below. The PWB and LTCC capacitors showed little, to no variations in capacitance with change in frequency, regardless of size.

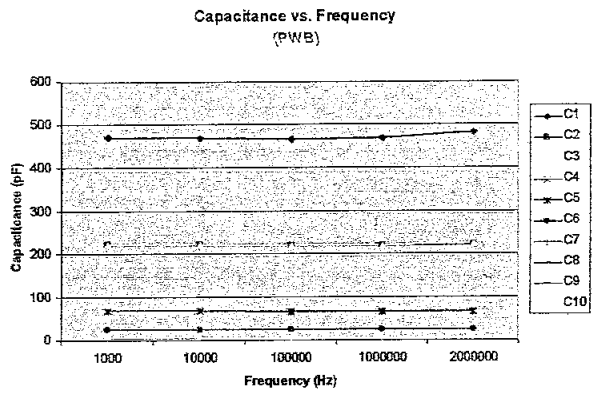

Figure 9 - Capacitance vs. Frequency (PWB)

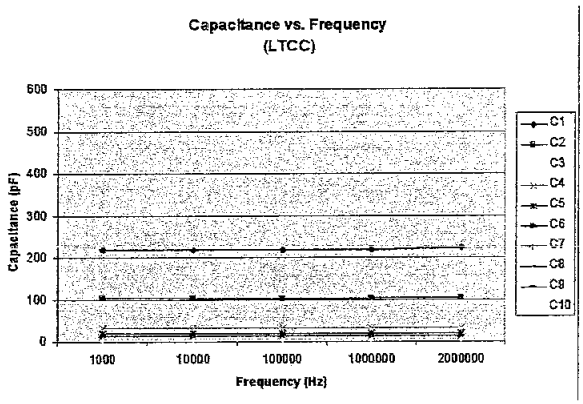

Figure 10 - Capacitance vs. Frequency (LTCC)

6 RESULTS

The measured response to each of the environmental test conditions was chosen to be resistance and capacitance (other measurements were also taken under certain test conditions and were explained in the characterization section of this report). The data for each environmental stress will now be summarized in the following sub-sections. The data presentation method chosen was to normalize the data from each environmental test. Data collected from an individual resistor or capacitor residing on a substrate taken over a particular number of substrates was combined to calculate an average and standard deviation for each test condition. The particular normalization method chosen for this investigation/study was to take each resistor or capacitor value and calculate the percent change for each component at each environmental test read-point. The equation used was the equation shown in the Environmental Testing Section of this report and was modified for either resistance or capacitance for all tests.

$$Percent\ change = \frac{X_2 - X_1}{X_1} \times 100,$$

Where:
X = can be resistance or capacitance
X_1 = the reference value

Once all of the data was normalized, an average and standard deviation was calculated for each read-point. This data was then plotted on a graph of percent change versus a particular read-point. A read-point could then be collected at a temperature, as with the TCR and TCC measurements, or time exposure in a chamber or number of cycles.

6.1 Thermal Coefficient of Resistance (TCR)

The TCR data was obtained using the equipment and procedure described in the environmental testing section. The TCR data for the PWB substrates are shown in Figure 11. The equivalent TCR data for the LTCC substrates are shown in Figure 12. For the temperature range of -55°C to +125°C the PWB technology exhibited a smaller change than did the LTCC technology. Both graphs depict changes that are within the respective manufacturer's quoted data. The negative slope in the PWB data is also consistent with the manufacturer's experience with polyimide board materials.

The explanation for the tighter data set in the PWB resistors over the LTCC resistors can be explained by the way the resistor materials are deposited. The PWB resistors are manufactured by depositing a thin film of NiP to a copper carrier substrate while the LTCC resistors are deposited by screen printing of a thick-film resistor paste which commonly consists of conductive powders, insulating glass, crystalline powders and an organic matrix that holds it all together. [5] As explained previously in the background section, these resistors can be considered as chains of conductive particles in a "sea" of glass after the firing process. The glasses in the thick-film resistor pastes tend to interact with the LTCC ceramic tape glass and can cause a shift in the ratio of resistive particles and therefore results in different square resistance and TCR values. On the other hand, a thin film process, such as the PWB resistor process, is very consistently controlled; thus yielding very consistent results.

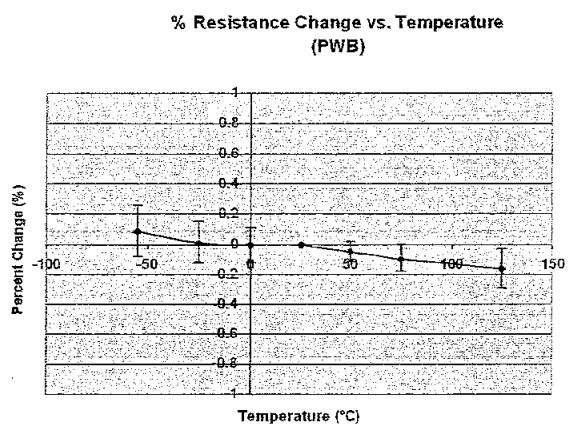

Figure 11 - Thermal Coefficient of Resistance Test data (PWB).

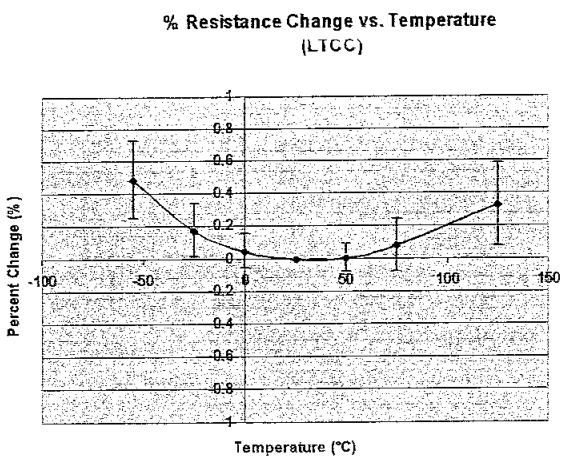

Figure 12 - Thermal Coefficient of Resistance Test data (LTCC).

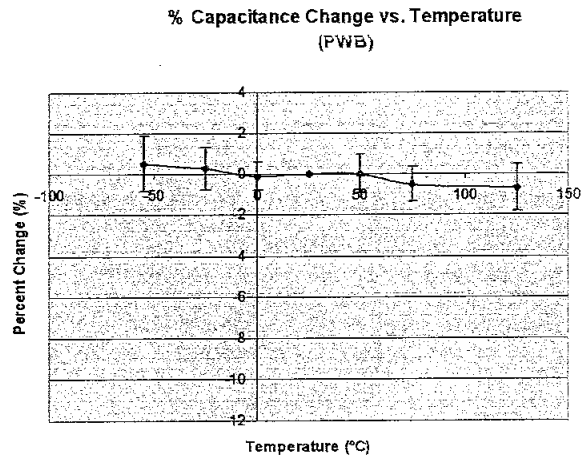

Figure 13 - Thermal Coefficient of Capacitance Test data (PWB).

6.2 THERMAL COEFFICIENT OF CAPACITANCE (TCC)

The TCC data was obtained using the equipment and procedure described in the environmental testing section. The TCC data for the PWB substrates are shown in Figure 13. The equivalent TCC data for the LTCC substrates are shown in Figure 14. For the temperature range of -55°C to +125°C the PWB technology exhibited a smaller change than did the LTCC technology.

As was the case for the tighter PWB data set with the TCR test, the tighter data set in the PWB capacitors over the LTCC capacitors can be explained by the way the capacitor materials are deposited. The PWB capacitors were manufactured by using two parallel copper foils separated by a thin polyimide film. Both materials' thickness and physical and electrical properties are easy to control. Whereas the LTCC capacitors are manufactured by two parallel plates made from a gold thick-film paste which contains gold particles in a sea of glass (see the above TCR discussion). These thick film conductors' glass interacts with the LTCC substrate glass content and varies the value of the capacitor.

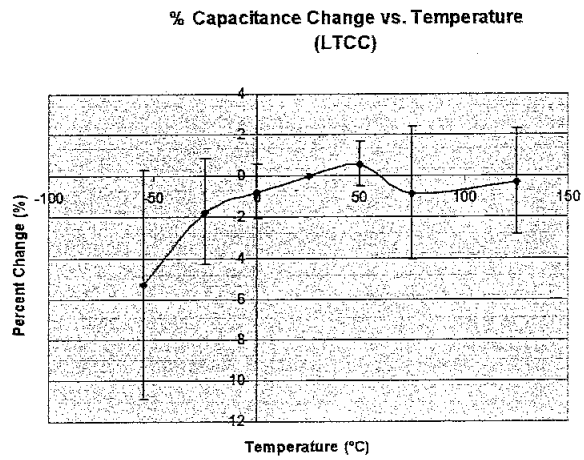

Figure 14 - Thermal Coefficient of Capacitance Test data (LTCC).

6.3 THERMAL AGING

The thermal aging test data was obtained using the method described in the environmental testing section. The raw data was processed as described in the beginning of this section to produce % change data that was plotted versus the read-point (in this case time – in hours).

6.3.1 EFFECTS ON RESISTANCE

The resistor thermal aging data for the PWB substrates is shown in Figure 15. Similarly, the resistor thermal aging data for the LTCC substrates is shown in Figure 16. For the duration of 1000 hours at an elevated ambient temperature of 125°C the LTCC substrates exhibited a smaller change in resistance.

The smaller change over time displayed by the LTCC substrates can be explained by material properties. The LTCC substrates are 100% inorganic ceramic, glass and metal which are fired at elevated temperature conditions in air at nearly 900°C. Further exposure to elevated temperatures in air (such as 125°C) would have little effect on the change of resistance. It is interesting to note that the resistors and conductors of the PWB substrates are metal systems (the resistors are NiP and the conductors are copper with the edge connectors made of gold) and should not be affected by the elevated temperature like the LTCC system. However, the elevated temperature was conducted in air (not an inert gas) and it is likely that oxygen reacted with the NiP resistor material and changed its properties. Figure 15 illustrates how the resistance changed with time exposure in the chamber and it appears that the oxidation effects have not saturated (i.e., leveled off) even after 1000 hours. The Ohmega website does not indicate that placing the resistors near the surface would cause them to perform differently than constructing the resistors internal to the PWB. But these results suggest that there may be some difference when compared to the reported data on the website. The solder resist provides some protection to these surface resistors, but under these test conditions it has allowed the resistance to change up to ~4%. The LTCC materials are more stable under the test conditions than the PWB materials.

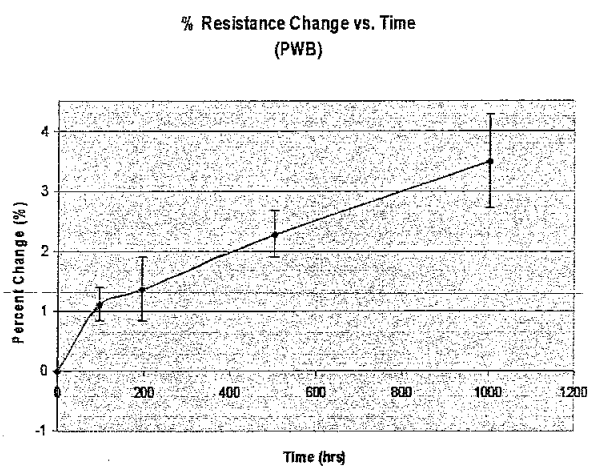

Figure 15 - Resistance Thermal Aging Test data (PWB).

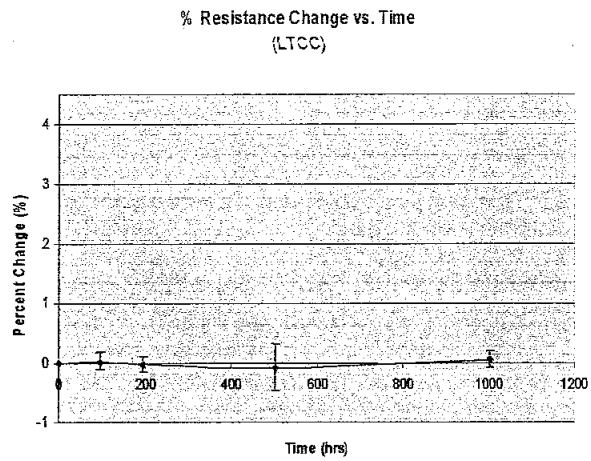

Figure 16 - Resistance Thermal Aging Test data (LTCC).

6.3.2 Effects on Capacitance

The PWB and LTCC capacitor data from the thermal aging test can be seen in Figures 17 and 18 below. The explanation for the change in capacitance over time of exposure to an elevated temperature can be found from the way that different materials react at different temperatures. At an elevated temperature a polyimide material is going to have a higher thermal coefficient of expansion than that of a ceramic material. Thus, as time increases, the polyimide substrate is going to experience more localized distortion (in the area around the copper parallel plates). The variation in capacitance seen in the LTCC data can be explained by the fact that the LTCC capacitors are manufactured by two parallel plates made from a gold thick-film paste which contains gold particles in a sea of glass (see the above TCR discussion). These thick film conductors' glass interacts with the LTCC substrate glass content and varies the value of the capacitor. The largest variations in the data can be seen by closer inspection of the effect of capacitor size for both the substrate technologies (see the Size Effects section later in the report). For both technologies, it can be shown that the smaller the capacitor physical size, the greater the variation in the data. Some of the large percent change reported in the data can be attributed to limitations in the measurements; i.e., small changes in the actual measurement can result in large percent change as seen in Figures 17 and 18. It is suspected that the distance between the parallel plates of the capacitors are changing (increasing) and that the high temperature exposure affects the small parallel plates the most in the PWB substrates.

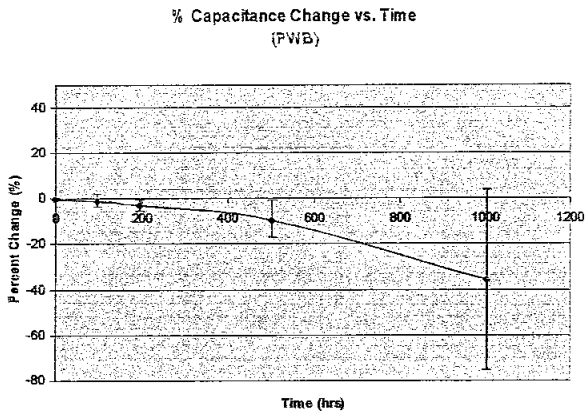

Figure 17 - Capacitance Thermal Aging Test data (PWB).

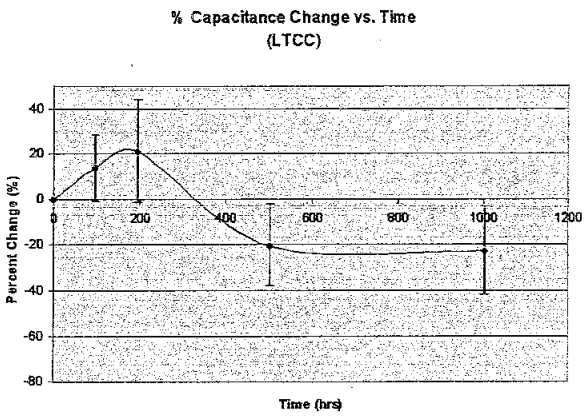

Figure 18 - Capacitance Thermal Aging Test data (LTCC).

6.4 HUMIDITY EXPOSURE

The humidity exposure test data was obtained using the method described in the environmental testing section. The raw data was processed as described in the beginning of this section to produce % change data that was plotted versus the read-point (in this case time – in hours).

6.4.1 EFFECTS ON RESISTANCE

The humidity exposure data for resistance in both the PWB and the LTCC substrates can be seen below in Figures 19 and 20. The graphs show that the LTCC substrates exhibited less change over time in the elevated temperature, elevated humidity chamber than the PWB substrates did. The increased percent change observed in the PWB substrates is most likely due to the fact that the PWB resistor film is composed of NiP. When exposed to elevated moisture and temperature conditions, oxy-hydroxide can form on the NiP film increasing resistance in the film and affecting the electrical performance of the resistor. In contrast, the LTCC substrates consist of gold, ceramic and glass and a thick-film resistor paste fired in air. When placed in elevated moisture and temperature conditions these materials are not likely to be affected and as a result no or little change is observed in the LTCC substrates over time.

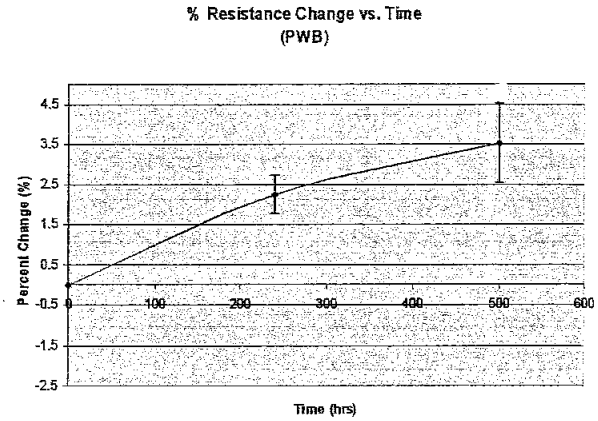

Figure 19 - Resistance Humidity Exposure Test data (PWB).

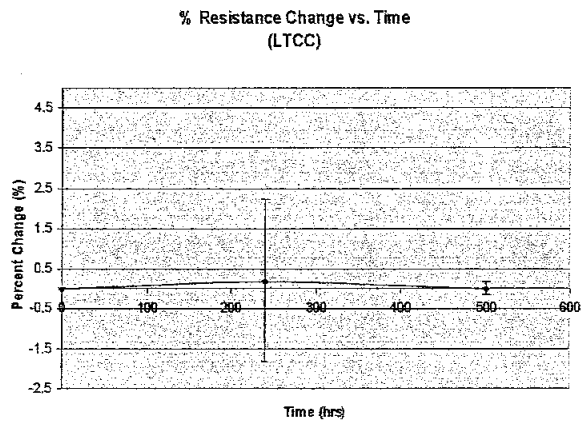

Figure 20 - Resistance Humidity Exposure Test data (LTCC).

The data obtained for back resistor #12 on PWB substrate #62 is not shown in Figure 19. This resistor was omitted from the data because it exhibited unusual electrical behavior. This resistor was deemed to be a failure as it exhibited a 227.5% increase in resistance between the 240 hour and 500 hour read points. Examination of the resistor under an optical microscope revealed that moisture penetrated the solder resist near resistor #12 and caused some corrosion of the resistor (see Figures 21 and 22). In both figures, there is an appearance of an area where the moisture entered the solder resist near the upper right corner of the resistor. This could be the result of a scratch, weak point or thin spot in the resist. At this time, the exact cause of the moisture penetration is not known.

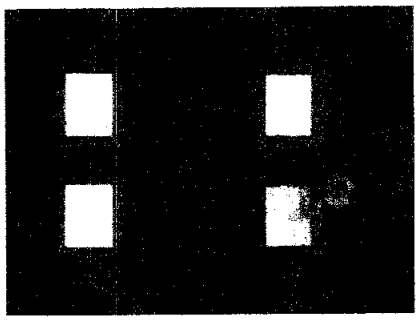

Figure 21 - Optical photograph of resistor #12.

Figure 22 - High magnification of failed resistor #12.

6.4.2 EFFECTS ON CAPACITANCE

The capacitance humidity exposure test data for the PWB substrates are shown in Figure 23 below. Similarly, the same data for the LTCC substrates are shown in Figure 24. The parabolic type shape of the curve observed in the PWB data can possibly be explained by a shifting or "warping" of the substrate material over the course of time in an elevated temperature and elevated moisture atmosphere. There are at least two forces being exerted on the substrates; one force relates to the humidity exposure and the other is due to the elevated temperature. Both combine to change the capacitance as well as moisture in the polyimide dielectric layer.

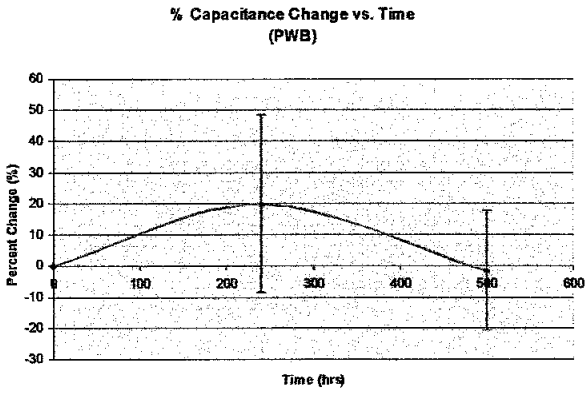

Figure 23 - Capacitance Humidity Exposure Test data (PWB).

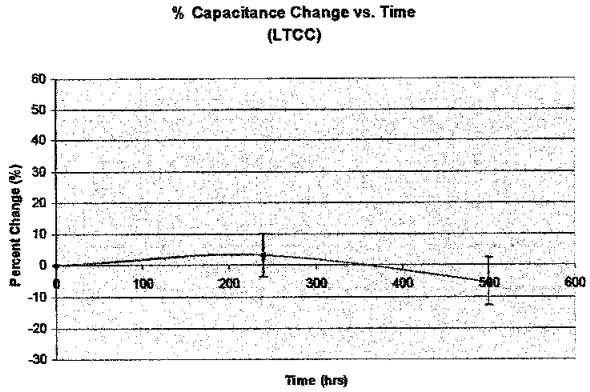

Figure 24 - Capacitance Humidity Exposure Test data (LTCC).

6.5 Thermal Shock

The thermal shock test data was obtained using the method described in the environmental testing section. The raw data was processed as described in the beginning of this section to produce % change data that was plotted versus the read-point (in this case time – in cycles).

6.5.1 EFFECTS ON RESISTANCE

Below are the graphs for effects on resistance from the Thermal Shock test on both the PWB and LTCC substrates (See Figures 25 and 26). The data from the thermal shock test effects on resistance for the PWB and LTCC substrates mimic the data from Thermal Aging (see above data). The main difference is the magnitude of the percent change, suggesting that the mechanism for causing the change is the same in both stresses. Both stress tests were conducted in air and reached 125°C. The thermal shock stress test spent less total time at the elevated temperature and therefore oxidized the PWB resistors to a lesser degree; thus producing a smaller change in resistance.

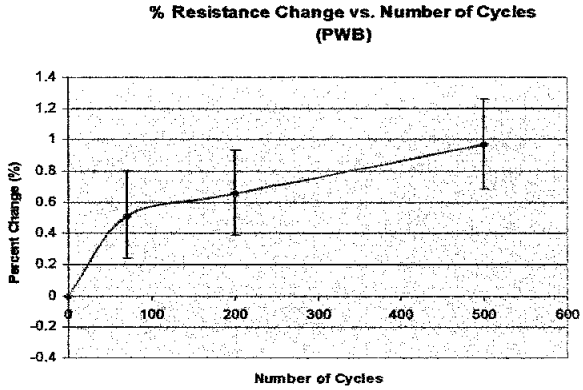

Figure 25 - Resistance Thermal Shock Test data (PWB).

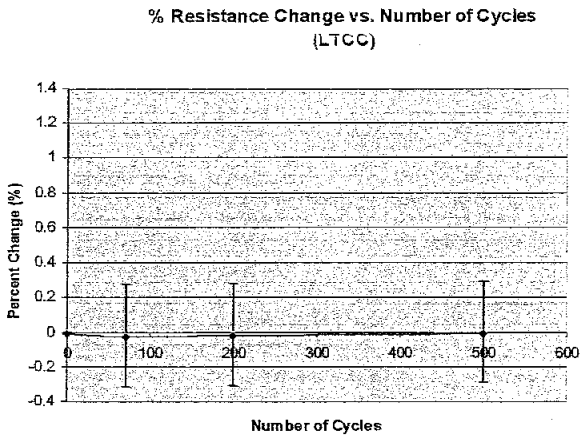

Figure 26 - Resistance Thermal Shock Test data (LTCC).

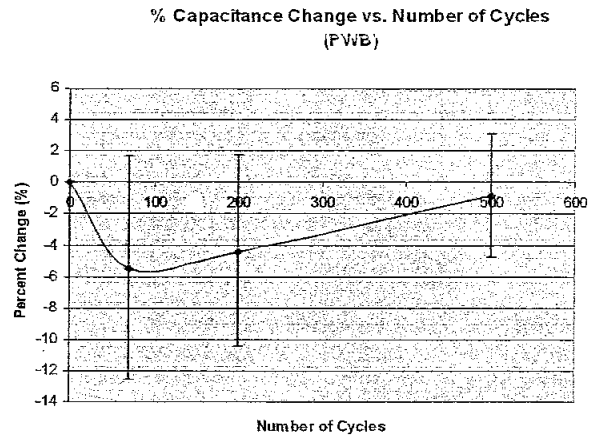

Figure 27 - Capacitance Thermal Shock Test data (PWB).

6.5.2 EFFECTS ON CAPACITANCE

The effects of the thermal shock test on capacitance can be seen for PWB in Figure 27 and for LTCC in Figure 28. The tighter data set observed in the graph for the LTCC substrates can be explained much like the explanation for the capacitance data set in the thermal aging test (see above section). The TCE for a polyimide material is much higher than the TCE for a ceramic material. Because of this, the PWB would be expected to encounter greater distortions in the material. These distortions could affect the distance between the parallel plates of the capacitor resulting in changes in capacitance over time. As localized distortions continue to occur the distance between the capacitor plates may increase and decrease causing variations in capacitance trends. Figure 27 would suggest that overall the materials set in the PWB experience localized distortions due to the induced thermal/mechanical stresses and then "settle down" to initial physical condition (i.e. plate separation, etc.) and yield the same capacitance as the initial measurements. Some of that may occur but upon closer inspection of the individual capacitors (see the Size Effects section) one can observe that the data is scattered positively and negatively and just happens to look like Figure 27.

The slight variation in capacitance evident in the LTCC data can again be explained by manufacturing process of the LTCC substrates in which the glass particles in the thick-film paste of the capacitors interacts with the LTCC substrate glass content and varies the value of the capacitor (see the above TCR discussion). Also, in the Size Effects Section, the data for all capacitors vary both positively and negatively.

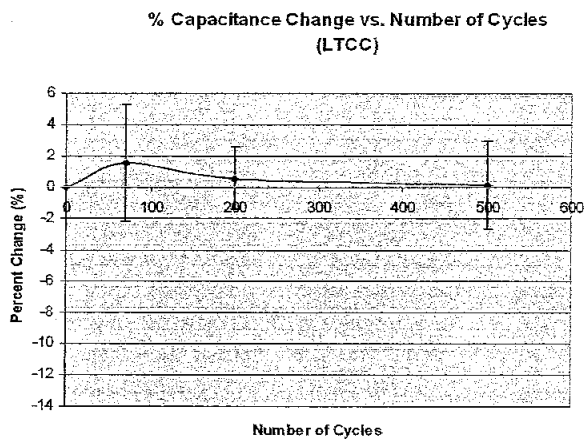

Figure 28 - Capacitance Thermal Shock Test data (LTCC).

7 DISCUSSION

7.1 GENERAL SUMMARY OF RESULTS SECTION

In general, both PWB and LTCC technologies test results obtained in this body of work agree with the manufacturer/literature with a few discrepancies as shown below in Summary Tables 4 and 5. Table 4 shows the data for the PWB technology. The stresses that stand out as exhibiting concern are: thermal aging (capacitance) and humidity exposure (resistance and capacitance). Table 5 shows a summary of the LTCC data. The stresses that stand out as exhibiting concern in that technology are: thermal aging (capacitance), humidity exposure (resistance). In the PWB technology, the humidity exposure test contributed to a resistor that exhibited resistance uncharacteristic of the general population of resistors. In this case, the resistor is classified as a failure. The failure mechanism is attributed to corrosion as a result of moisture penetrating the solder resist as discussed in the results section.

Table 4. Summary Table of the Data Collected in this Study Compared to the Manufacturer (PWB)

Environmental Test	Max % Change / Average % Change	Manufacturer/Literature Reported Data	Remark & Condition
TCR	0.4% / 0.2% (-20 PPM/°C)	0.4% (-60 PPM/°C) [10]	MIL-STD-202-304 Hot cycle: 25°C, 50°C, 75°C, 125°C Cold cycle 25°C, 0°C, -25°C, -55°C
TCC	4.6% / 0.7%	Percent Change: 3.0% [11]	MIL-STD-202-304 Hot cycle: 25°C, 50°C, 75°C, 125°C Cold cycle 25°C, 0°C, -25°C, -55°C
Thermal Aging (Resistance)	8.1% / 3.5%	Not specified (Alcatel Bell Percent change: 0.1%) [10]	MIL-STD-202-108 Ambient Temp: 125°C Test length: 1000 hours
Thermal Aging (Capacitance)	97.9% / 35.8%	Not available	MIL-STD-202-108 Ambient Temp: 125°C Test length: 1000 hours
Humidity Exposure (Resistance)	227.5%* / 7.2% 5.4%* / 3.5%	Percent Change: 0.75% Ambient Temp: 40°C Relative humidity: 95% Length of test: 240 hrs [10]	Ambient Temp: 85°C Relative humidity: 85% Test length: 500 hours *Including failed resistor value
Humidity Exposure (Capacitance)	116.1% / 19.9%	Not available	Ambient Temp: 85°C Relative humidity: 85% Test length: 500 hours
Thermal Shock (Resistance)	2.1% / 1.0%	Percent Change: 1.0 % Test length: 25 cycles [10]	MIL-STD-202-107 Low temp: -65°C High temp: 125°C Test length: 500 cycles
Thermal Shock (Capacitance)	24.1% / 5.4%	Not available	MIL-STD-202-107 Low temp: -65°C High temp: 125°C Test length: 500 cycles

Table 5. Summary Table of the Data Collected in this Study Compared to the Manufacturer (LTCC)

Environmental Test	Max % Change / Average % Change	Manufacturer Reported Data	Remark & Condition
TCR	1.0% / 0.5% (-30 PPM/°C)	±200 PPM/°C Hot cycle: 25°C, 50°C, 75°C, 125°C Cold cycle 25°C, 0°C, -25°C, -55°C [5]	MIL-STD-202-304 Hot cycle: 25°C, 50°C, 75°C, 125°C Cold cycle 25°C, 0°C, -25°C, -55°C
TCC	18.6% / 5.3%	Percent Change: 20% Hot cycle: 25°C, 50°C, 75°C, 125°C Cold cycle 25°C, 0°C, -25°C, -55°C [12]	MIL-STD-202-304 Hot cycle: 25°C, 50°C, 75°C, 125°C Cold cycle 25°C, 0°C, -25°C, -55°C
Thermal Aging (Resistance)	3.2% / 0.1%	Percent Change: 0.8% Ambient Temp: 125°C Test Length: 500 hours Applied bias: 5V [13]	MIL-STD-202-108 Ambient Temp: 125°C Test length: 1000 hours
Thermal Aging (Capacitance)	63.6% / 22.8%	Percent Change: 6% Ambient Temp: 60°C, Relative Humidity 90% Applied bias: 50V Test Length: 100 hours [14]	MIL-STD-202-108 Ambient Temp: 125°C Test length: 1000 hours
Humidity Exposure (Resistance)	17.1% / 0.2%	Percent Change: 1.2% Relative Humidity 85% Test Length: 500 hours [13]	Ambient Temp: 85°C Relative humidity: 85% Test length: 500 hours
Humidity Exposure (Capacitance)	22.2% / 5.2%	Percent Change: 6% Relative Humidity 85% Test Length: 500 hours [12]	Ambient Temp: 85°C Relative humidity: 85% Test length: 500 hours
Thermal Shock (Resistance)	2.1% / 0.02%	Percent Change: 2% Low temp: -55°C High temp: 160°C Test length: 300 cycles [13]	MIL-STD-202-107 Low temp: -65°C High temp: 125°C Test length: 500 cycles
Thermal Shock (Capacitance)	10.2% / 1.6%	Not available	MIL-STD-202-107 Low temp: -65°C High temp: 125°C Test length: 500 cycles

7.2 EFFECTS OF COMPONENT SIZE

The component sizes for this work were described in an earlier NEPP Report [1] and described again in Tables 1 – 4. The constraint on the component sizes was limited to the size of the substrate and by the manufacturer's range of component sizes used in the past for other customers. The resistor values are not determined by the area of the resistor but rather the number of squares in the circuit trace. The largest target value of resistance was 3 squares and the smallest value was 1/3 square. In PWB substrates the resistors were made with 50 Ω/□ and yielded values of between 25Ω to 150Ω, while the LTCC resistors were made with material that was 100 Ω/□ and yielded resistor values ranging between 50Ω and 300Ω.

The design for the capacitors was accomplished in much the same manner [1] but the values are proportional to the size of the capacitor plates. Since the two technologies were comprised of different materials the capacitance values were different. Figures 29 and 30 illustrate the values as a function of area for the two technologies used in this work. From the figures it can be seen that the PWB capacitors yield nearly 2X the values of the LTCC substrates for capacitors of the same area.

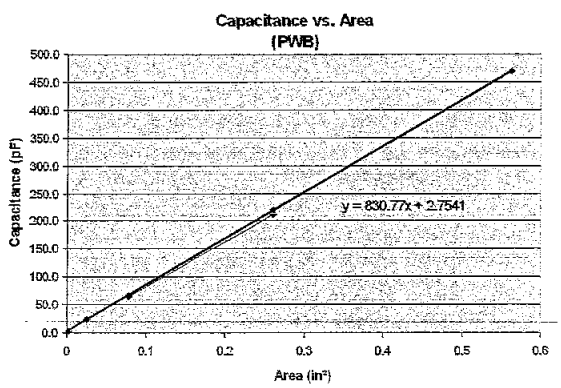

Figure 29 - Capacitance versus size (PWB).

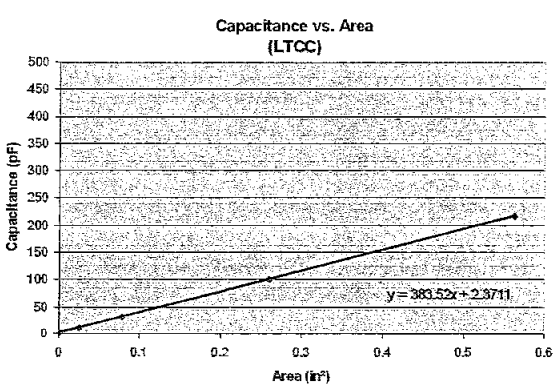

Figure 30 - Capacitance versus size (LTCC)

The substrates used in this evaluation were designed with different physical sized components as described in Tables 1 - 4. There was an effect of embedded component size observed numerous times during the data analysis. In the Characterization Section of this report it was noted that smaller capacitors had higher DF values as shown in Figure 3. In that figure, if the smallest capacitors were eliminated from the data set the PWB capacitors would have performed similarly to the LTCC capacitors.

In the Thermal Aging Section of this report, it was also mentioned that the capacitance response showed effects of size when the individual capacitor sizes were plotted. Figure 31 shows the effects of capacitor size for the PWB technology. Notice that as the capacitor size is reduced, the greater the effects of the % change. In fact the smallest capacitor (0.016in^2) exhibited nearly 100% change in capacitance. Figure 32 shows the effect of capacitor size for the LTCC technology. Although the response is different than the PWB substrates, the end results are nearly the same; the largest capacitor did not change in value during the test.

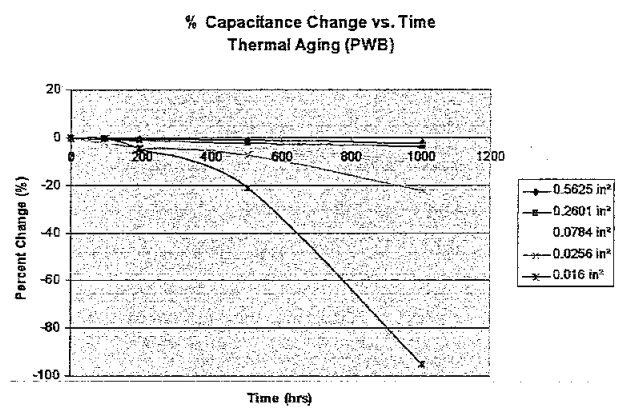

Figure 31 - Effects of capacitor size (PWB) for Thermal Aging Stress.

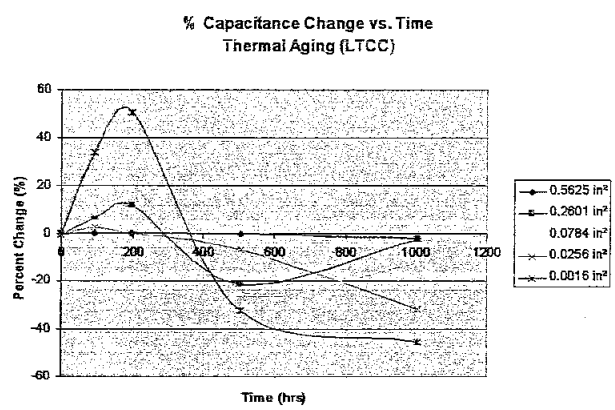

Figure 32 - Effects of capacitor size (LTCC) for Thermal Aging Stress.

Another example of size effects on capacitance can be seen in the thermal shock data for the PWB. Figure 33 is a graph of the capacitance results for Thermal Shock plotted individual for sizes. Notice that if the two smallest sizes of capacitors were eliminated from the data, all of the remaining capacitors would vary less that 2%.

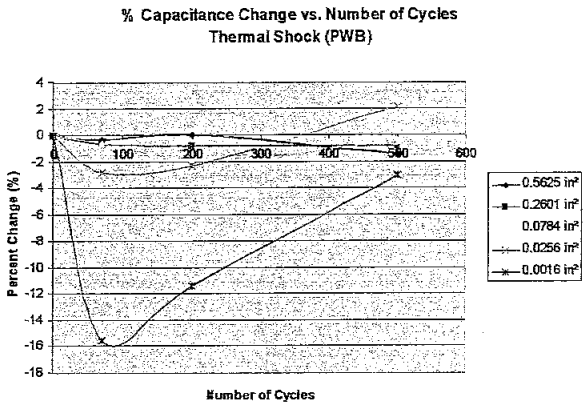

Figure 33 - Effects of capacitor size (PWB) for the Thermal Shock Stress.

The data for the PWB technology in the Humidity exposure test strongly indicates that there is a size effect present. The smaller capacitors are affected most. Figure 34 shows the effect of size for the Humidity Exposure Stress. It may be possible that moisture affected the polyimide board material initially causing the outer layers of the material to swell, forcing parallel plates of the capacitors closer together. As the distance between the parallel plates is decreasing, it correspondingly causes an increase in capacitance. As the substrates were further exposed to the elevate moisture environment, the entire system (i.e. the polyimide film between the parallel plate conductors) became saturated causing it to swell as well thus dimensionally stabilizing the system, resulting in the capacitance returning to near the initial values. The dielectric constant of the polyimide film (between the parallel plates) has also likely changed due to the addition of moisture. The LTCC substrates data spread is not as large because the elevated temperature environment has less of an effect on a ceramic material than on a polyimide due to ceramics higher temperature tolerance.

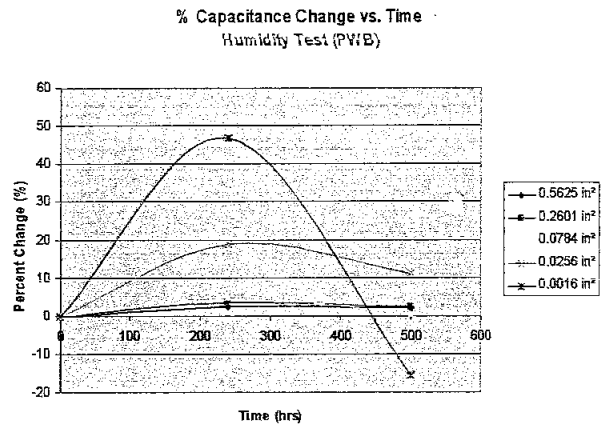

Figure 34 - Effects of capacitor size (PWB) for Humidity Exposure test.

Concurrently, it is also likely that the combination of humidity and elevated temperature of the test caused the substrate material to distort in shape as time in the elevated temperature/humidity chamber increased. It was observed that the change in capacitance tended to be larger for the smaller capacitors. The data spread showed that the smaller capacitors values changed most, possibly because the smaller capacitors were exhibiting the affects of more localized distortions. Localized distortions in the substrate material may have been restrained by the stiffening effects of the metal plates of the larger capacitors; meaning that the larger the capacitor, the less likely the area around the capacitor would be susceptible to deformation. Therefore, the larger capacitors were better able to help maintain the substrate material's original shape and better able to hold the distance between the parallel plates of the capacitor constant, whereas the smaller capacitors were not, thus changing the distance between the parallel plates, resulting in changes in capacitance.

7.3 EFFECTS OF EMBEDDED COMPONENT ORIENTATION

The PWB resistor manufacturer suggested that there was a slight difference in resistance based on x and y orientation which was related to the manufacturing process. The resistors in the substrates were laid out with x and y orientation in order to investigate this phenomenon. Figure 35 shows the data for resistors in x and y orientation for the Thermal Aging Stress. As can be seen there is not a significant difference for this effect. This data was typical for all stresses and only Figure 35 is shown as an example.

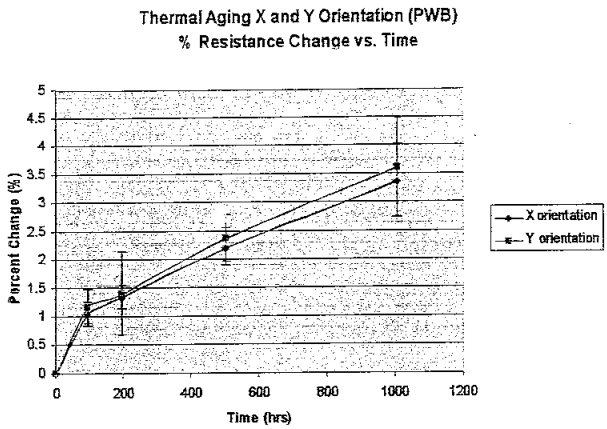

Figure 35 - Graph of % Resistance Change versus Exposure time at 125 °C (PWB). Both resistors in x and y orientation are shown as well as error bars (one standard deviation).

7.4 EFFECTS OF RESISTORS ON SURFACE

The effects of the resistors residing on the surface of the substrate versus buried in the interior is claimed by the manufacturer to not affect reliability. The data collected in this study did find a resistor in the PWB technology that increased in resistance over 200% with the corrosion mechanism causing the increase. There was a weak point in the solder resist near the resistor as shown in Figure 22. Obviously in this case, the resistor would not have corroded if it was protected by additional layers of material such as if it were buried in the interior of the PWB.

The thermal aging tests conducted in this body of work also resulted in the resistors changing in value by an average of 3.5% for the PWB technology. In contrast, the LTCC resistors changed in value by 0.1%. It is suspected that the resistor material was affected by the oxygen in the high temperature chamber penetrating the thin solder resist coating. It is not known if placing the resistors in the interior of the board would result in more stable resistors. Future work should include a comparison of the buried resistors versus surface resistors.

RECOMMENDATIONS

The overall impression of the technologies evaluated in this body of work is that they merit further investigation by NASA for possible use in NASA Projects. Initial data from the organic based system are very consistent; i.e. the values of the as-constructed resistors and capacitors exhibited small standard deviations from the mean value, while the initial measurements of the ceramic based technology exhibited more scatter in the data. [1] As discussed earlier, it is believed that the PWB process is more consistent primarily due to it being from an industry established high volume process while the LTCC components are from a more emerging low to medium volume process. Also, the nature of the construction of the LTCC components is harder to control as it consists of conductive (or partially conductive) materials suspended in a glass matrix. How the particles touch and conduct current is something that is inherently more difficult to control than thin film/foils of material, as in the PWB process.

The high temperature processing and properties of the LTCC materials showed that the materials and processes were more stable over time and exposure to stress than the PWB materials. For all conducted tests the resistors of both technologies were very consistent and varied by no more than a couple of percent over the life of the test. The largest differences were found to be in the capacitors of both technologies. However, due to the layout of the capacitors on the substrate the effect of size could be factored out of the data. Both capacitor technologies showed a size effect that if the small capacitors were not designed into a future project, data from both technologies would be consistent. The manufacturer of the PWB capacitor technology stated in a technical paper that capacitors should remain below about ½ in on a side as the capacitor plates in larger capacitors would be more likely to distort. [16] Our findings did not seem to support these recommendations as the smaller capacitors varied more than the larger capacitors. However, the recommended size by Dupont was the size that we found to be the most consistent in value over the conducted testing.

Based on the reliability stress data collected in this study several recommendations can be made for future work in NASA.

PWB Technology (Organic)

Recommendation 1:
Surface resistors are very dependent on solder resist integrity. If resistors are placed on the surface for purposes of laser trimming to tolerance, an additional coating is recommended.

Recommendation 2:
Capacitor size should not be less than 0.5 in x 0.5 in (400pF) based on the above discussion. This 'cut-off' is dependent on the design. If a design can withstand a larger variation in capacitance, a smaller capacitor could be used. For most designs larger not smaller capacitor values will be required (Figure 29).

LTCC Technology (Inorganic)

Recommendation 1:
Capacitor size should not be less than 0.75 in x 0.75 in (250pF) based on the above discussion. This 'cut-off' is dependent on the design. If a design can withstand a larger variation in capacitance, a smaller capacitor could be used. For most designs larger not smaller capacitor values will be required (Figure 30).

FUTURE WORK

Work to be performed in the future should include a comparison of these technologies to an actual equivalent circuit. Performance at high frequency should be investigated and compared for LCR response effects.

Future work should also include a comparison of surface resistors versus buried resistors as well as characterizing the electrical stress (i.e. current flowing through the components) effects on the components.

Qualification stress testing should include a preconditioning of the substrates to a known condition (of moisture) and then place the substrates through a solder reflow profile three times prior to the stress conditions. This would be particularly useful to fully understand the PWB technology and is analogous to the JEDEC Preconditioning for Plastic Encapsulated Microcircuits (JESD22-A113C).

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