



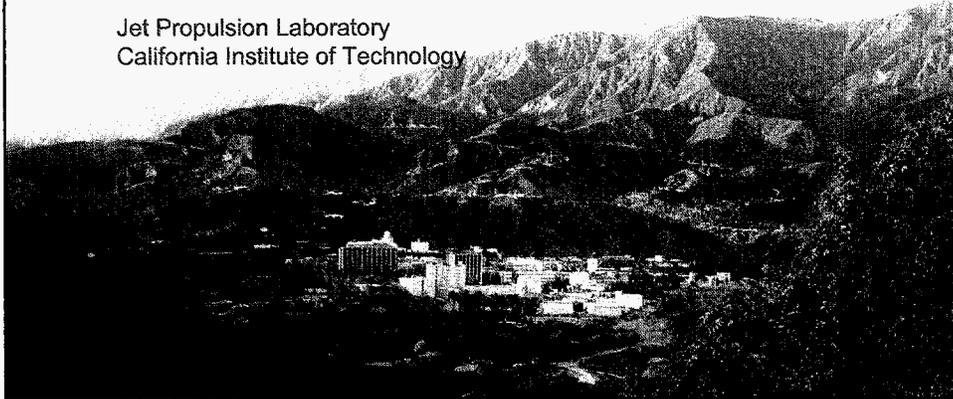
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Qualification Strategies of Field Programmable Gate Arrays (FPGAs) for Space Application

October 26, 2005

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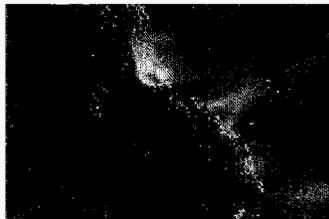


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Historical

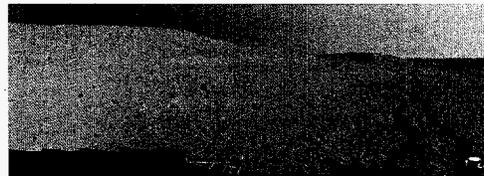
- FPGAs have been used in spacecraft for over 10 years.
- There have been over 100 launches and 300 satellites that had FPGAs on board.
 - Echo star
 - International Space Station
 - Hubble Space Telescope, etc..
- Modern spacecraft design have >40 FPGAs on board.
- FPGAs are used in high reliability & extreme environ. applications

Recent JPL examples:



Deep Impact

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Spirit in the Gusev crater

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FPGA Applications in Space

- What FPGAs provide:
 - High gate densities
 - Rich on-board architectural features
 - Large I/O counts with multiple I/O standards
 - Less volume and weight but greater performance
- Broad range of Applications:
 - Navigation activities
 - Star tracking
 - Sun sensing
 - Cameras
 - Radio communications
 - Motor Control
 - Lander Pyrotechnics
 - Bus communications:
 - I2C
 - PCI

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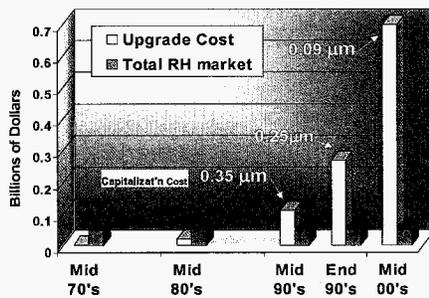
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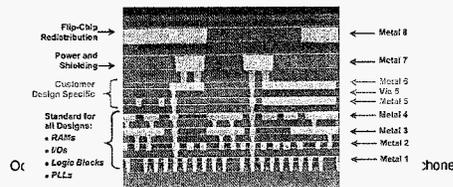


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Programmable Devices are Here to Stay --It is All About Cost



- Cost of manufacturing is exponentially increasing
- Space market is flat
- ASIC design cost is skyrocketing
- Programmable devices will be used in more applications
- Future trend: Via programmable devices are a commercial trend that may move into space market



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FPGA Fabric is Getting More Complex

- As CMOS continues to shrink, features for spacecraft targeted FPGAs continue to grow:
- Actel:
 - RTAX - 180nm antifuse technology
 - Up to 4M system gates and equivalent 500K ASIC logic gates.
 - Up to 840 I/O's w/ multiple standards
 - 540Kb embedded memory
- Xilinx:
 - Virtex II Pro - 150nm CMOS technology
 - Up to 6M system gates
 - Up to 1104 I/O's w/multiple standards
 - 3648Kb total user memory
- Others (Aeroflex, etc.)



FPGA Functionality is Growing

- As FPGA features increase, so do the complexity and capability of the FPGAs.
- Variety of embedded IP now available:
 - Various DRAM and SRAM interfaces
 - SDR/DDR DRAM and SRAM
 - Network FCRAM
 - QDR SRAM
 - Dedicated multiplier blocks for DSP applications
 - LVDS and LVPECL I/O
 - Embedded Processors
- As FPGA complexity increases, so does the complexity of qualification and risk management of these devices.
- *Qualification methodologies must evolve as FPGA technology evolves.*



Specifications Relating to FPGAs - Are they still relevant?

- MIL-STD-883E
 - Method 5005.13 - Qualification and Quality Conformance Procedures
 - Method 5010.3 - Test procedures for screening, qualification, and quality conformance requirements for complex monolithic microcircuits. (*min of 4,500 transistors!*)
 - JEDEC143 - Solid State Reliability Assessment and Qualification Methodologies.
- Much of the intent of these specs is still viable, yet they need to be updated for the density and capability of modern FPGAs.
- Modern issues:
 - Cost of testing FPGAs electrically has increased dramatically.
 - Ability and knowledge to adequately provide test coverage as also increased.
 - Need of multiple test structures.
 - Reduce tolerance to input signals and board conditions.
 - Handling new packages
 - Cost of devices reduces sample sizes
 - Burn-in of foundry developed nanometer scale CMOS not strongly justified.

**FPGA reliability assessment has to be re-evaluated
with consideration for application and cost**



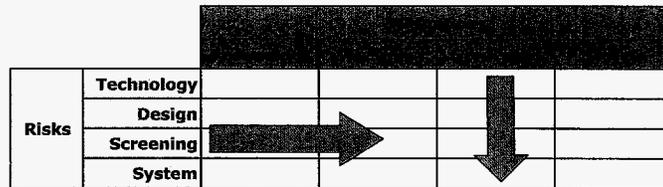
Risk Management as a Basis for Qualification

- Risk management is defined for this application as “the process of determining what areas could produce a reduction in performance and/or an actual failure of an FPGA device.”
- Once these possible failure areas have been identified, plans and methodologies are implemented to address and mitigate the concerns.
- This approach provides a qualification plan that is application specific based upon the knowledge base of technology, mission, and system requirements.
- A multi-tiered approach to qualification can then be developed to provide a robust, layered risk reduction methodology.
- Such a multi-tiered approach allows for “trade-offs” of various tests and screens to provide realistic cost management capability for missions while explicitly acknowledging risk.



Risk Management through Mitigation

- The following areas are identified as the risk reduction foundation:
 - *Technology*
 - *Design*
 - *Screening*
 - *System*
- Conceptual matrix shows multiple options to mitigate risk.
- Reducing risk by addressing concerns as early as possible in the device development and manufacture is preferred.
 - This saves costs and improves quality.
- *The role of the FPGA vendor in this task is critical.*
 - The complexity of the devices require input and technical review and comment from the vendor.



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Qualification Risk – Technology New Materials

- FPGAs provide inexpensive access to cutting edge technology
- Device Physics level process development is the key metric for risk reduction.
- Degradation mechanisms related to the operation of the part need to be identified and characterized.
- Scaling technologies require that many different concerns be addressed:
 - Voltage constraints
 - Standby and Operating Power
 - Hot Carrier Degradation
 - Electromigration and Voiding
 - Threshold Variation and Leakage
 - Oxide Integrity
 - Soft Errors
 - Programming Issues
- Proper qualification of FPGAs require successful resolution of these.

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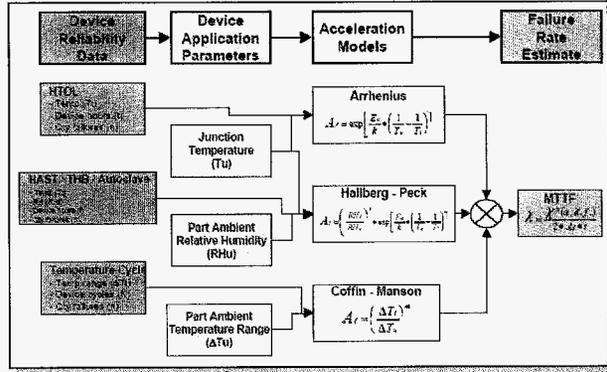
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Qualification Risk – Technology

A close interaction with vendors needed

- Technology qualification the responsibility of the FPGA vendor (and their foundry if necessary).
- Requires specialized test structures and complex analysis to obtain predictions for lifetime and failure rate.
- Information needs to be available to FPGA consumer to ensure robust processes are being used for the intended applications.



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Qualification Risk – Technology

New screening approaches

- Testing FPGAs has become a major technical undertaking.
- As feature sizes enter 150nm and below, testing methods that were valid, reliable, and cost effective at larger feature sizes may no longer be so.
- Parameters such as intrinsic leakage tend to increase in deep submicron processes to a level where traditional test limits cannot be reliably applied.
- Tests such as IDDq, VDDmin/max are generally anticipated to have an end of useful life at very small feature sizes.
- Screening for subtle defects such as resistive paths and timing defects are more difficult. This increases the chance for test escapes and possible failures in the end application.
- Innovative approaches that integrate thermal cycling, voltage stressing and functional testing are being developed to sort good die with possible latent failures from good die that have no latent failures.
 - Allow for proper acceleration of stress conditions to reveal failure mechanisms and latent defects.

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Qualification Risk – Technology Yield vs. Latent defects

- Defect screening is essential to achieve the levels of device quality and reliability demanded in today's and tomorrow's applications.
- Screening at the earliest feasible point in the process is fundamental to achieving good reliability as well as high yields.
- Fatal defects associated with yield loss have been linked with latent defects that affect device reliability.

$$R = Y^k$$

where $k = \text{Area}_{\text{reliability}} / \text{Area}_{\text{yield}}$

- Therefore, yields can be one of the earliest predictors of subsequent device reliability.
- Even wafers/lots with high yields can contain devices with latent defects.
- The screening of these latent defects is essential to achieve excellent reliability.
- Die that have passed these tests can be made available to the customer at a premium.

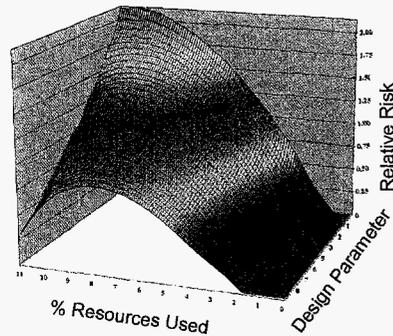


Qualification Risk – Design Mapping the risk response

- FPGAs are dominated by the design process.
- The most impact the customer can have on risk mitigation is during the design process. This includes:
 - Operating frequency
 - Specific consumption and utilization of FPGA resources
 - Margin to failures, etc.
- Relative Reliability risk of the FPGA as a function of time, $R_{\text{risk}}(t)$ is defined as:

$$R_{\text{risk}}(t) = F(d1, d2, d3, \dots)$$
 where $d1, \text{ etc. are design parameters.}$

- Being able to produce an empirical mapping (response surface) of these parameters is critical to assessing risk.





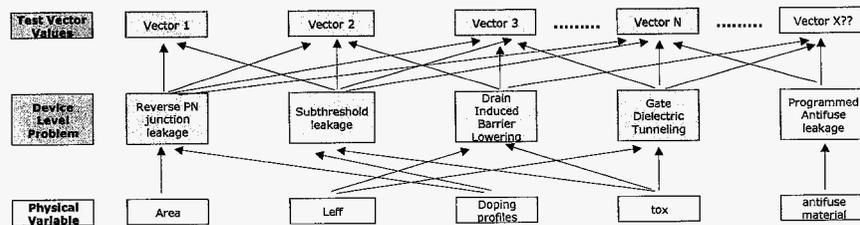
Qualification Risk – Design Guidelines

- Variety of design defects that need to be tested for and screened:
 - Address Faults
 - Defects in the address lines and address decoder
 - Stuck-at Faults
 - The logic value of a stuck-at memory cell is always 0 or 1
 - Transition Faults
 - A rising (falling) transition fault fails to undergo a 0-1 (1-0) transition when written
 - Many others...
- Both core logic features and interconnects need to be tested.
- Interconnect Coverage
 - Overall Interconnect test coverage needs to be > 99%



Qualification Risk – Design Correlate test to physical variable

- Mapping of Electrical Testing to Device Phenomena remains a major area for development.
- Test vectors need to be constructed to be able to map to underlying physical mechanisms that cause reliability degradation.
- The relationship of the design being tested to test vector used to the device level parameter being examined is very complex.
- The role of specifically designed test circuits is becoming more and more important and relevant to proper qualification of FPGAs.





Qualification Risk – Design Test circuits gain importance

- Ring oscillator based circuits are frequently used because they provide a relationship between electrical measurements such as power (P) to device related parameters:

$$P \sim CV^2 f_{\text{switching}} \sim N_{\text{stages}} * V_{\text{dd}} * q_{\text{max}} * f_{\text{switching}}$$

- Built In Self Test (BIST) architectures and approaches remain an important part of the testing and debug phase.
 - They utilize the regularity of an FPGA by implementing small test circuits repetitively over FPGA's CLB arrays.
 - Each test circuit targets a specific path and determines conformance of the path delay according to a test clock.



Qualification Risk – Design Temperature

- Aggressive scaling of CMOS devices has made power dissipation and thermal management issues very challenging.
 - Sub-threshold leakage power grows exponentially with temperature.
- Assumptions of a constant temperature model through out the device are becoming too simplistic.
- Analysis has shown temperature gradients exist on a single silicon die.
 - Different activities at the same time (sleep modes, functional-block clock gating, etc.)
 - Local variations across the power bus resulting from unequal heating of a metal interconnect due to Joule heating.
- Temperature gradients can affect signal integrity and performance.
- Delay can increase 5%-8% for every 10°C delta in temperature.
- CAD tools must have temperature algorithms included during routing to help address this condition.



Qualification Risk - Screening

- Screening is designed to detect manufacturing defects and possible early life failures.
- This is becoming more and more difficult with each new generation of FPGAs.
- FPGAs made on commercial high volume foundry technologies have sophisticated yield management and defect reduction programs.
 - Likelihood of manufacturing defects has been reduced.
- 3rd party testing and burn in for a single mission can cost ~\$1M.
- The amount of engineering knowledge needed to provide adequate test coverage really only resides with the device manufacturer.
- *The FPGA provider must be thought of as member of the spacecraft team, not merely a component provider.*
 - All the items previously discussed in this presentation are the responsibility of the manufacturer.
 - Spacecraft development organizations are responsible to audit and review such information.



Qualification Risk - System

- The FPGA vendor can provide critical review and application implementation information.
- How the FPGA is actually implemented can result in reliability issues if not done correctly.
 - Including the vendor directly as part of the design and system allows for proactive implementation of all possible design best practices.
- Vendor review in areas including requirements for:
 - I/O Pin Capacitance and Termination
 - Edge Rates
 - Output Drive Strength and Slew Rate Control
 - Simultaneously Switching Noise
 - Signal Integrity
- Example: Ground Bounce:
 - Ground bounce tolerance has dropped from 800mV to 300mV for modern FPGAs.
 - Flip chip lead inductance is dropping while modern PCB inductances are increasing.
 - As a result, substantially more ground bounce voltage now develops across the PCB.
 - The vendor can provide detailed review of PCB-FPGA interaction to ensure all specifications have been met and understood.



Example Risk Matrix

- A multi-tiered approach to provide a robust, layered risk reduction methodology.
 - Three different levels for three different levels of risk.
- Allows for "trade-offs" of various tests and screens to provide realistic cost management capability for different missions.
- System level reliability analysis is included as method to understand mission specific reliability risk using most up to date failure models.
- Operational exercise of final system board(s) is considered critical to provide final check for device performance to mission requirements.

| | Qualification Level | | |
|---|---------------------|---------|---------|
| | Level 1 | Level 2 | Level 3 |
| Technology | | | |
| TDD/HCJ/NBTJ/EM | X | X | X |
| Life test data on 3 lots (>2000Hrs) | X | | |
| Design | | | |
| Design Parameter Sensitivity | X | X | X |
| Theta J and power | X | X | X |
| Criticality Analysis | X | X | |
| System Level Reliability Analysis | X | X | |
| Screening | | | |
| Wafer level programming screens | X | X | |
| High yield area die selection | X | | |
| Tri-temp Functional Testing | X | sample | |
| Burn In | N/A | sample | |
| Life Test on flight lot | X | X | |
| System | | | |
| 500 Hr Operational Exercise of Flight Board | X | X | X |
| Vendor supported implementation design review | X | | |

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Conclusions

- Spacecraft now depend on using FPGAs for many critical tasks and operations.
- Modern FPGAs have evolved into profoundly complex silicon systems.
- Qualification and risk management of such complex systems requires new approaches.
- The end user can be considered as a part of the manufacturing cycle.
 - Particularly where programming is required.
- A vendor-user team needed to integrate engineering information from a variety of sources.
- A matrix approach to qualification has been presented that:
 - Complements historical specifications
 - Highlights the importance of device physics as a cornerstone to qualification.
 - Provides levels of risk management that expressly document trade offs.
 - Stresses the role of the FPGA vendor as team member in the development of modern spacecraft.

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