Open-Systems Architecture of a Standardized Command Interface Chip-Set for Switching and Control of a Spacecraft Power Bus

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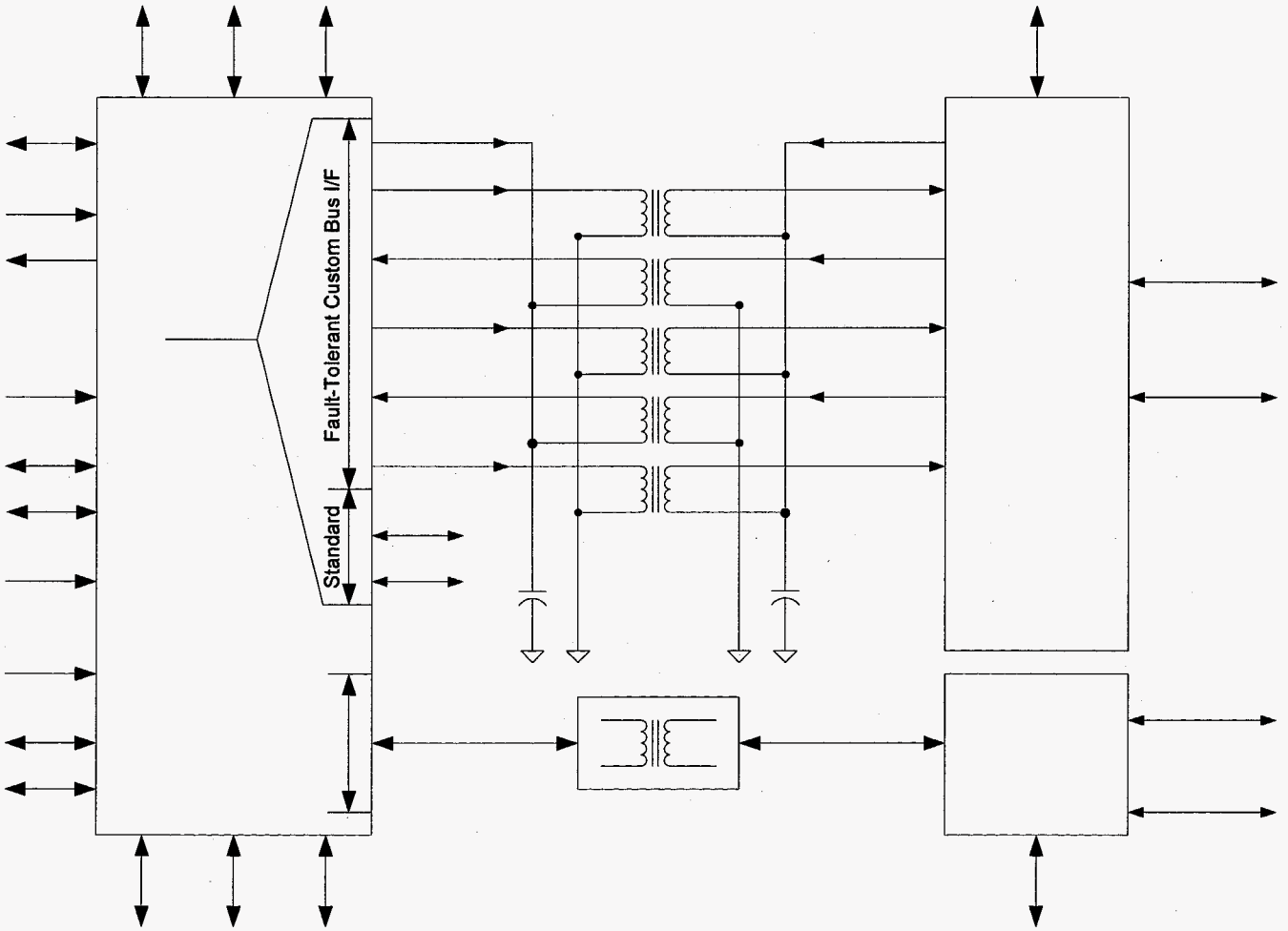
Introduction

- CIA-AIA chip-set:
  - Is a set of mixed-signal ASICs that provide a flexible high level interface between the spacecraft's command and data handling (C&DH) electronics and lower level functions in other spacecraft sub-systems.
  - Due to the open-systems architecture of the chip-set including an embedded microcontroller a variety of applications are possible.
- Developed By:
  - The Jet Propulsion Laboratory as part of the Deep Space Avionics (DSA) Project for Outer Planets Missions.
- Developed To Provide:
  - A single solution for both the switching and regulation of a spacecraft power bus.
- Fabricated Using:
  - Honeywell Solid State Electronic Center's (SSEC) SOI-IV Process.

Applications of CIA-AIA Chip-Set

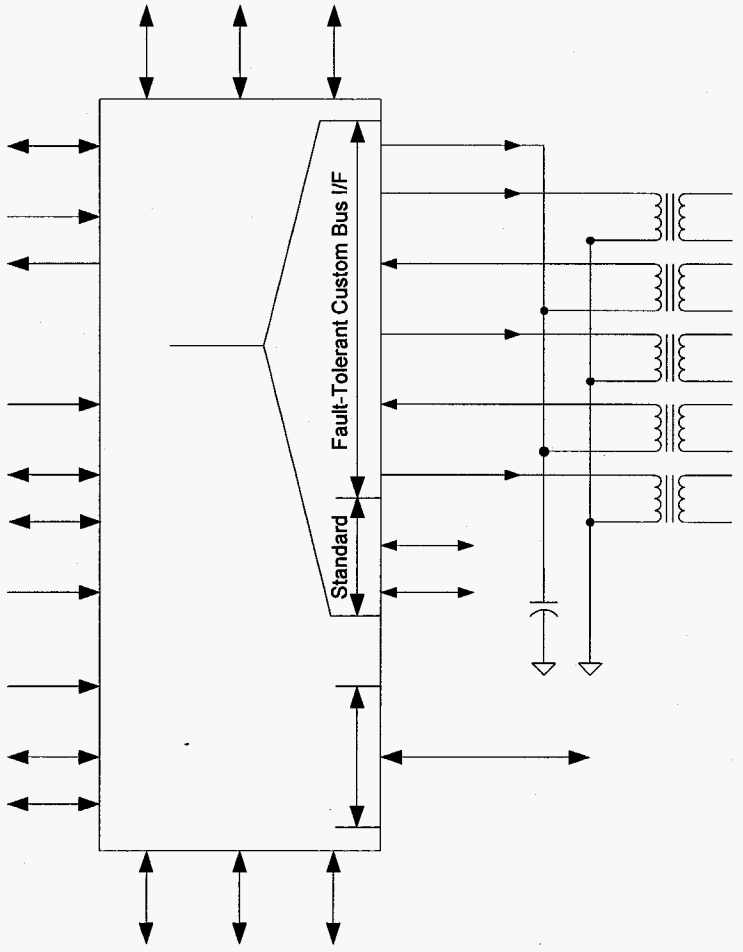
- **Power Switch Slice (PSS) – DSA Power System Electronics**
  - **Spacecraft Responsibilities**
    - Enabling/Disabling of Valves
    - Switching of all Loads
    - Firing of all Pyrotechnics
- **Power Control Slice (PCS) – DSA Power System Electronics**
  - **Spacecraft Responsibilities**
    - Power Bus Regulation
    - Power Bus Fault Protection
    - Control Charge/Discharge of the Battery
- **Other**
  - **Suitable for many other embedded applications such as remote data collection and instrument interface**

CIA-AIA Chip-Set Overview



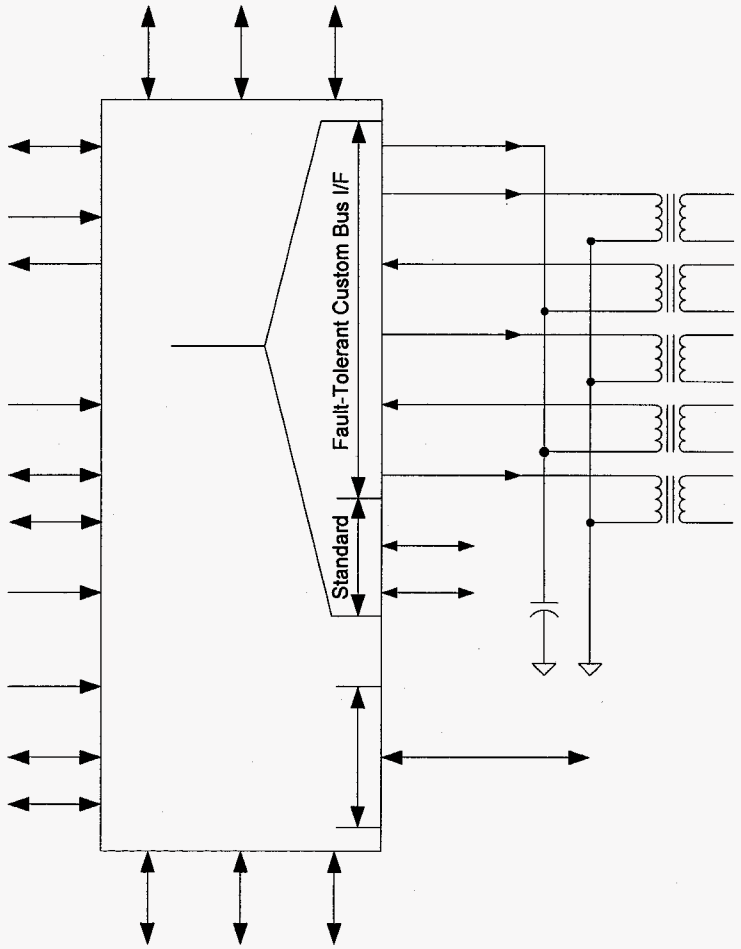
CIA External Interfaces

- **Power Cross-Strap**
  - **Input: Two 3.3 V Supplies**
  - **Output: One 3.3V Supply used internally and available externally**
  - **Input: Two 5 V Supplies**
  - **Output: One 5V Supply used internally and available externally**
- **Switch Interface (Digital I/O)**
  - **Control**
    - Switch Control
      - Software Controlled
      - Used to Engage/Disengage a single switch
      - One Line per Switch (16 Discrete Outputs)
    - Switch Enable
      - Hardware Controlled
      - Used to Enable/Disable a switch group (4)
    - Switch Default
      - Hardware Controlled
      - 16 Power-on-Reset (POR) Default Inputs (1 per Switch)



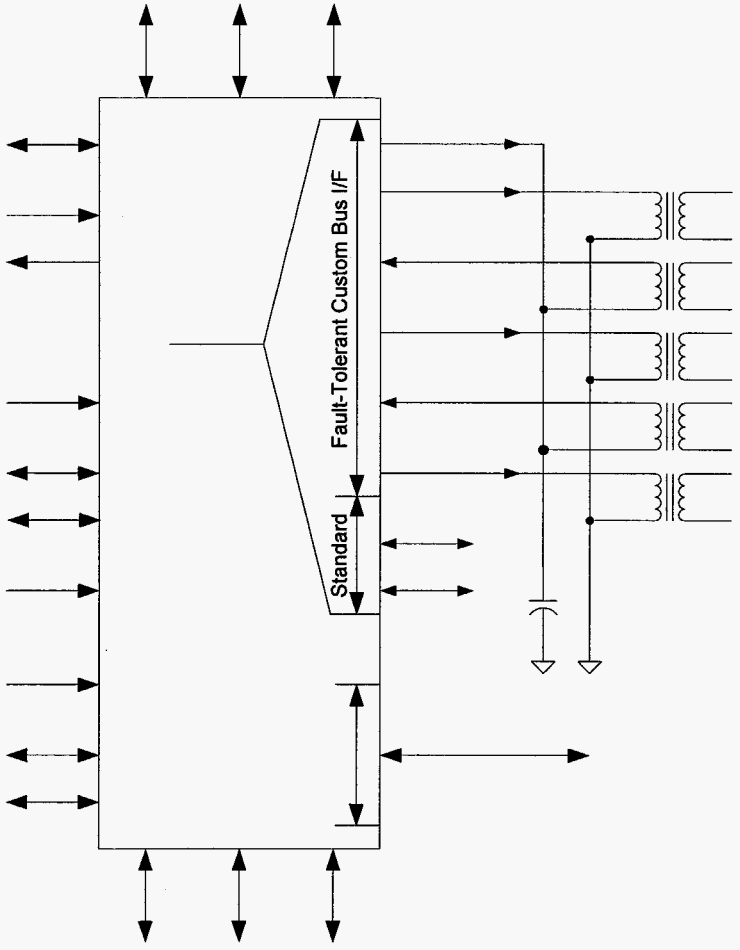
CIA External Interfaces

- **Telemetry**
  - Telemetry Select
    - Output from CIA
    - 1-bit select – In PSS Application used to determine which analog measurement is desired (Voltage or Current)
  - 4-Analog Unconditioned Input Channels
    - Switch current & voltage measurement
  - Digital Switch Status
    - A logic level output by the switch indicating if the associated switch tripped.
    - One Line per Switch.
- **Conditioned Analog Inputs**
  - Two Current Monitor Circuits
  - One Voltage Monitor Circuit
    - Produces Under Voltage Signal
- **Discrete Input/Output Signals**
  - Used to close battery charge control loop in PCS application
  - Can be configured for multiple other uses



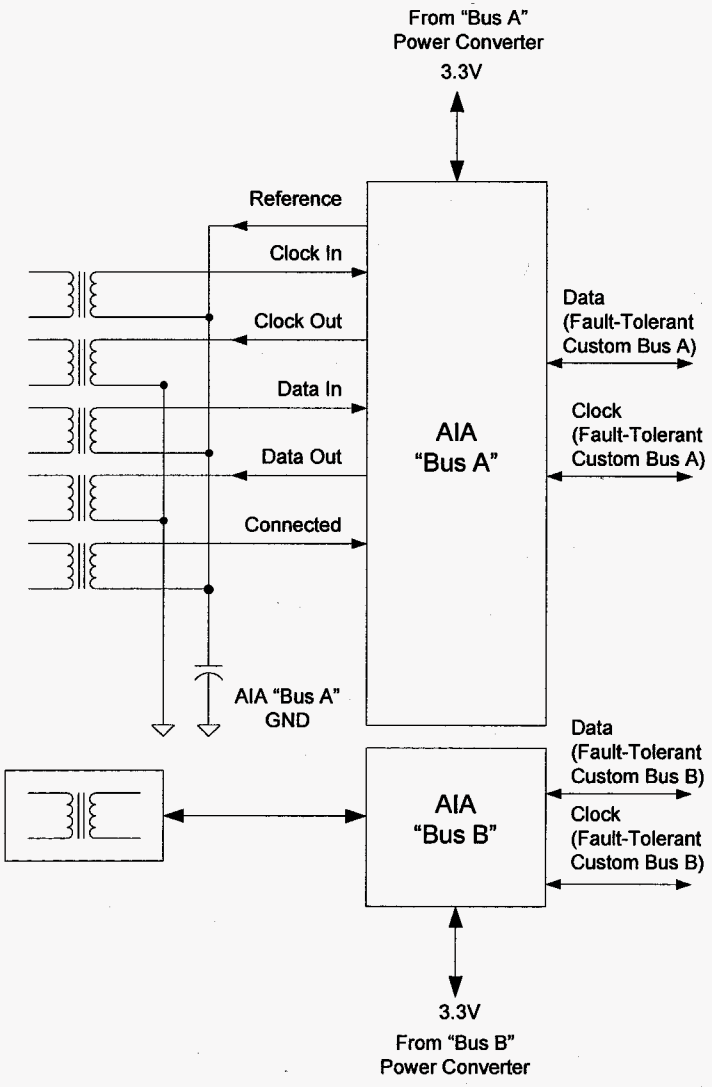
CIA External Interfaces

- **External RAM/ROM port**
  - **External ROM is Pin Selectable**
    - Default of Internal ROM (PSS Application)
  - **External ROM/PROM/EEPROM**
    - Provides for Reprogram Ability
    - 32Kx8 Maximum Allowable Size
  - **External RAM/Memory Mapped I/O**
    - 8-bit Data bus with 1-bit parity
    - 15-bit Address Bus
    - Up to 32KB of External RAM
    - Other Memory Mapped I/O may be connected to the CIA
- **Bus Interface (Phillips I2C)**
  - **Redundant Standard & Custom I2C Bus interfaces**
  - **Custom is transformer Isolated**
  - **One AIA per custom bus connection required.**



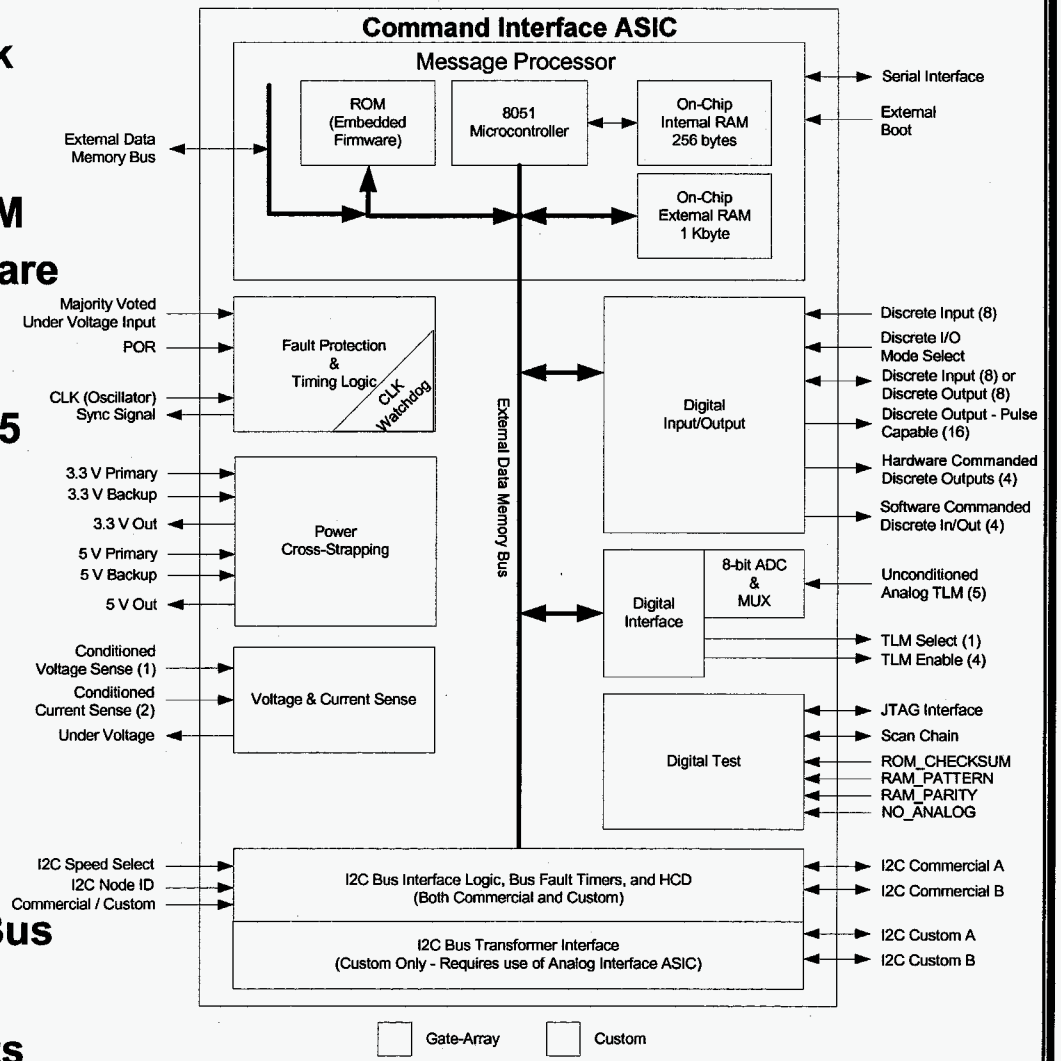
AIA External Interfaces

- **Power**
  - **Intended to draw power from the same converter supplying power to the bus which it is connected**
- **I2C Custom Bus Interface**
  - **Data and Clock connections**
    - 30 mA Sink Capability
    - Slew Rate Controlled
    - Long Bus Lengths Possible
- **I2C Transformer Interface**
  - **5 Transformer cores required per bus interface**
  - **Packaged in a single pack**



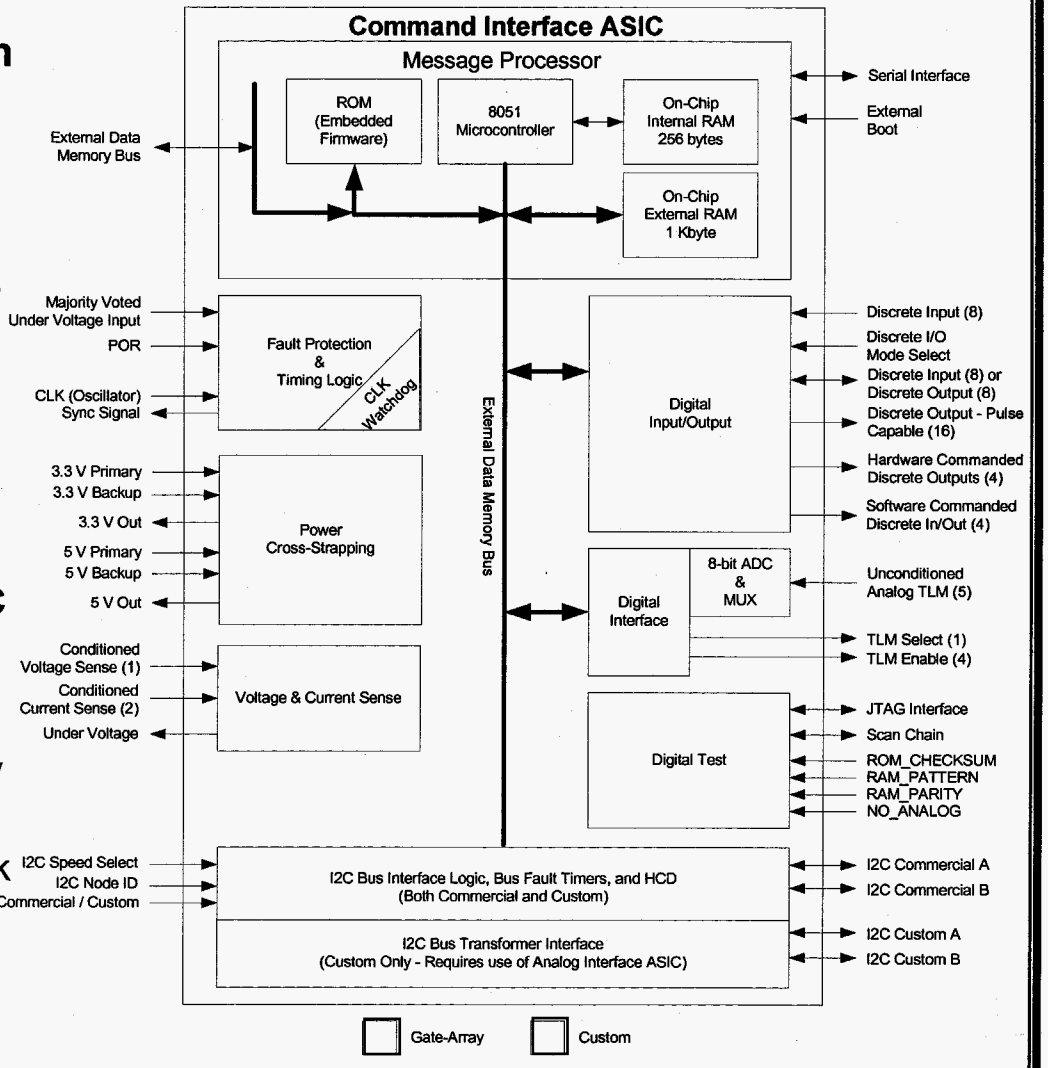
CIA HW Functional Description

- **Message Processor**
  - 8051 Microcontroller Core (2 clock cycles/instruction)
  - 256 Bytes of Internal RAM
  - 1K Byte of External (On-Chip) RAM
  - 8K x 8 On-Chip Boot ROM (Firmware for PSS Application)
  - External RAM/ROM Port
  - 2 Operating Speeds (16.5 MHz/8.25 MHz)
  - Serial Interface
- **Digital Input/Output**
  - Functions as Switch Control and Digital Status
- **On-Chip ADC**
  - 8-bit ADC Honeywell Macrocell
  - 8:1 Analog Mux
  - Digital Interface to 8051 Internal Bus
- **Digital Test**
  - JTAG & Custom Digital Test Inputs



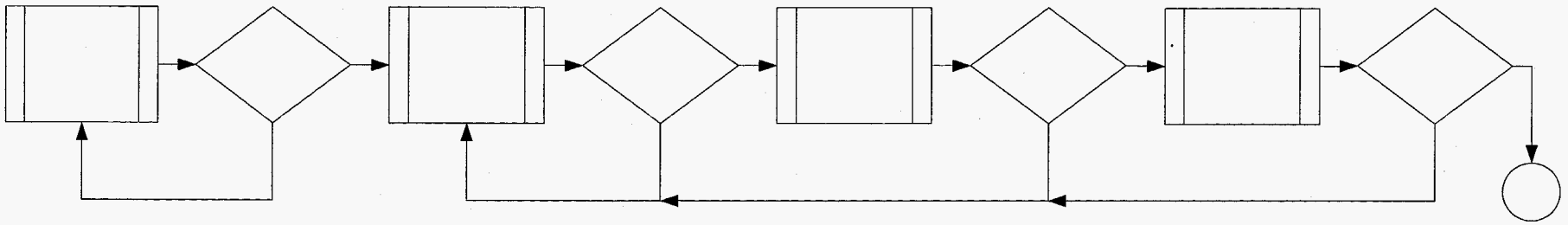
CIA HW Functional Description

- **I2C Bus Interface Logic**
  - **Simultaneous Communication with Two Independent I2C Busses**
    - Two I2C Link Layers with One I2C Hardware Address
    - Custom bus Interfaces to Analog Drivers through Transformer Isolators.
  - **Fault Protection Timers**
    - Fail Silent (1 per bus)
    - Auto-Turn-On (1 per chip)
    - Byte Timers (1 per bus)
  - **Standard I2C Bus Connection**
- **Fault Protection and Timing Logic**
  - **Produce CIA's Internal Resets**
  - **Maintain Local Time**
  - **Divide 33 MHz XTAL into internally needed frequencies**
    - Watchdog on 16.5 MHz. Internal Clock
- **Conditioned Analog Inputs**

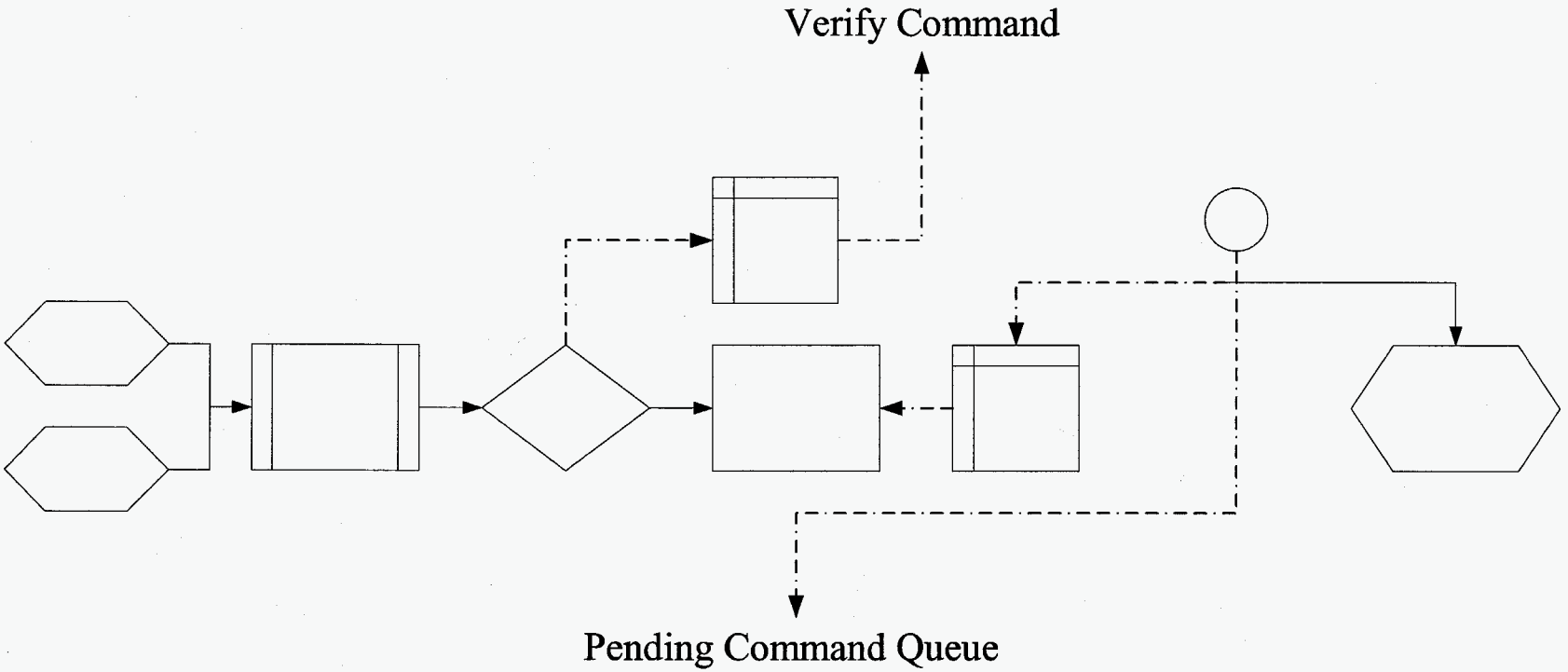


CIA FW Functional Description

- **Embedded Firmware**
  - provides for reliable startup
  - switch command and telemetry request receipt and verification
  - command execution
  - telemetry gathering
  - periodic health monitoring
- **Startup Code (Assembler)**
  - Performs ROM checksum
  - Pattern tests internal registers and internal RAM
  - Pattern tests external RAM but maintain any Critical Data.
- **Main Processing Loop (C)**
  - Determines Reset Type and Proceeds Accordingly
  - Enables Interrupts
  - Checks for the arrival of both switch and telemetry request commands over the I2C bus.
  - Allows processing of both established interrupts (I2C and 1.6ms)
  - Performs ongoing checksumming of ROM.

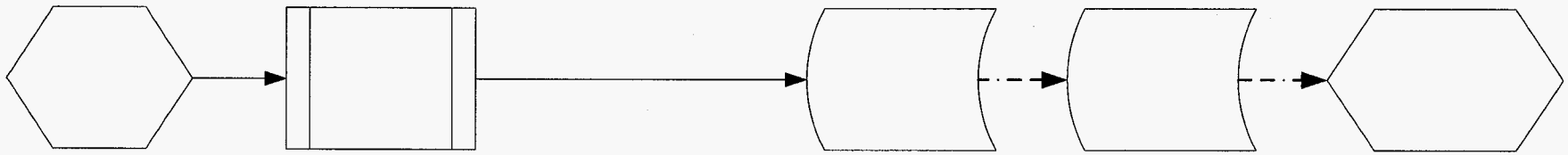


CIA FW Functional Description



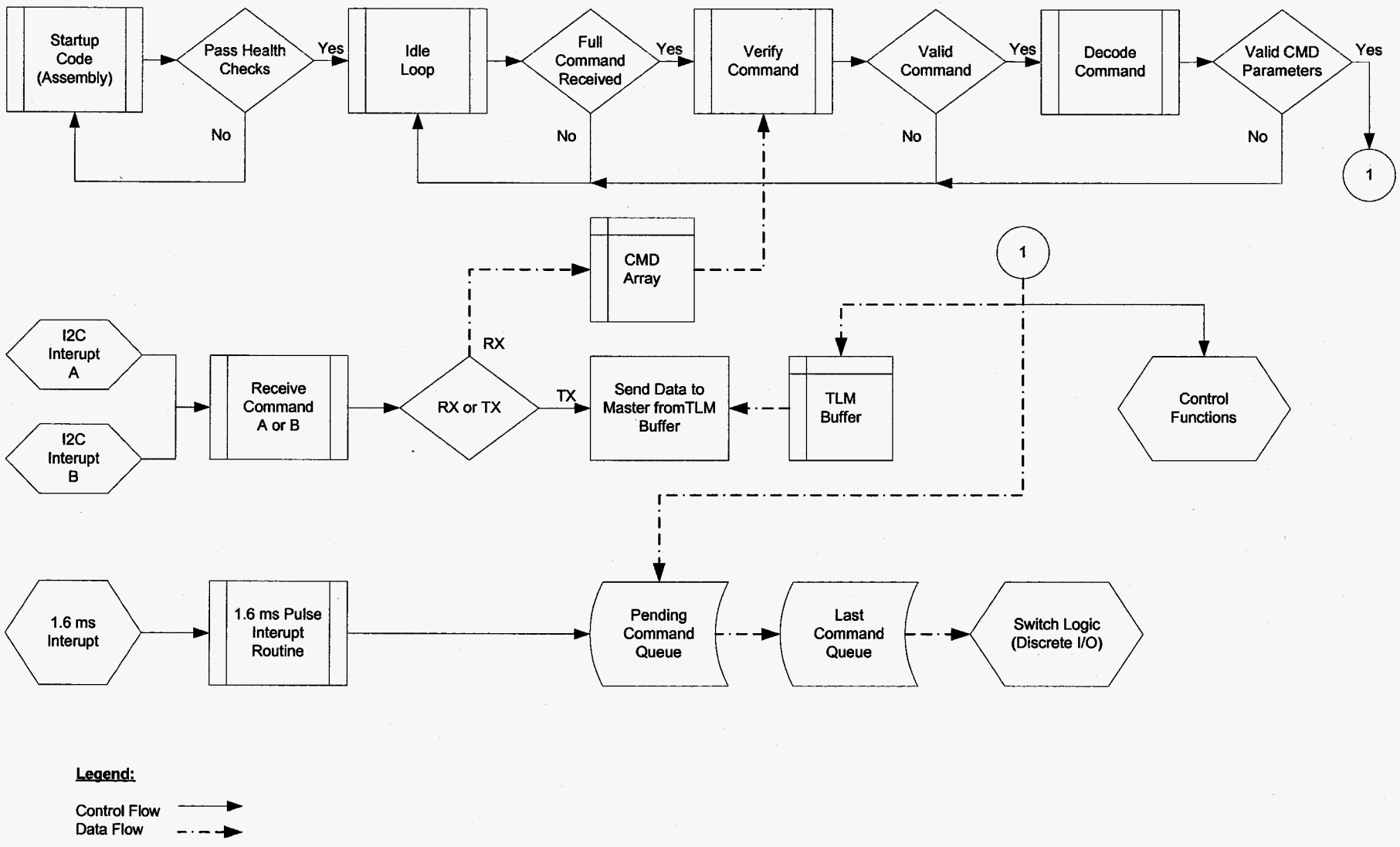
- **I2C Interrupt**
  - **Collect incoming data bytes and form commands that are passed to the main processing loop.**
  - **Load telemetry packets into the I2C hardware buffer that are then clocked out to the I2C bus master**

CIA FW Functional Description



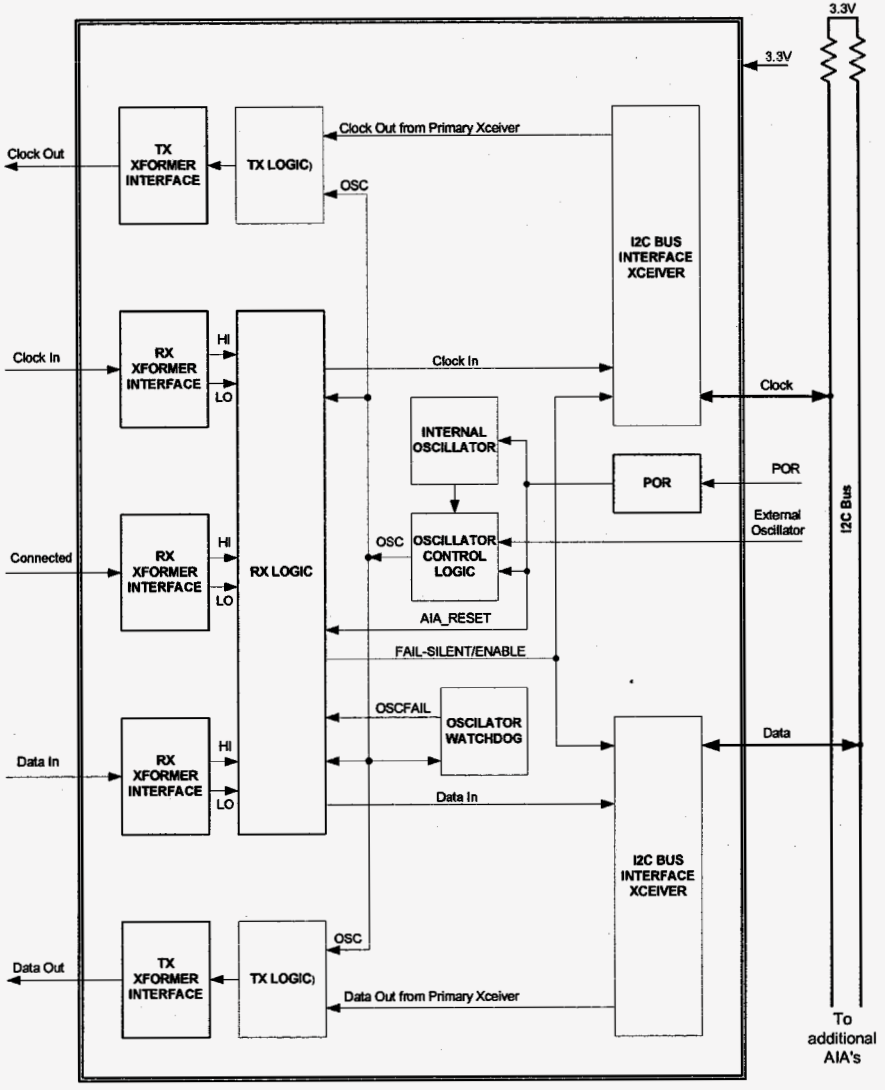
- **1.6 ms Interrupt**
  - **Used to actuate the on/off state of the digital I/O lines (switches)**
  - **Used to determine duration of pulsed commands.**

CIA FW Functional Description



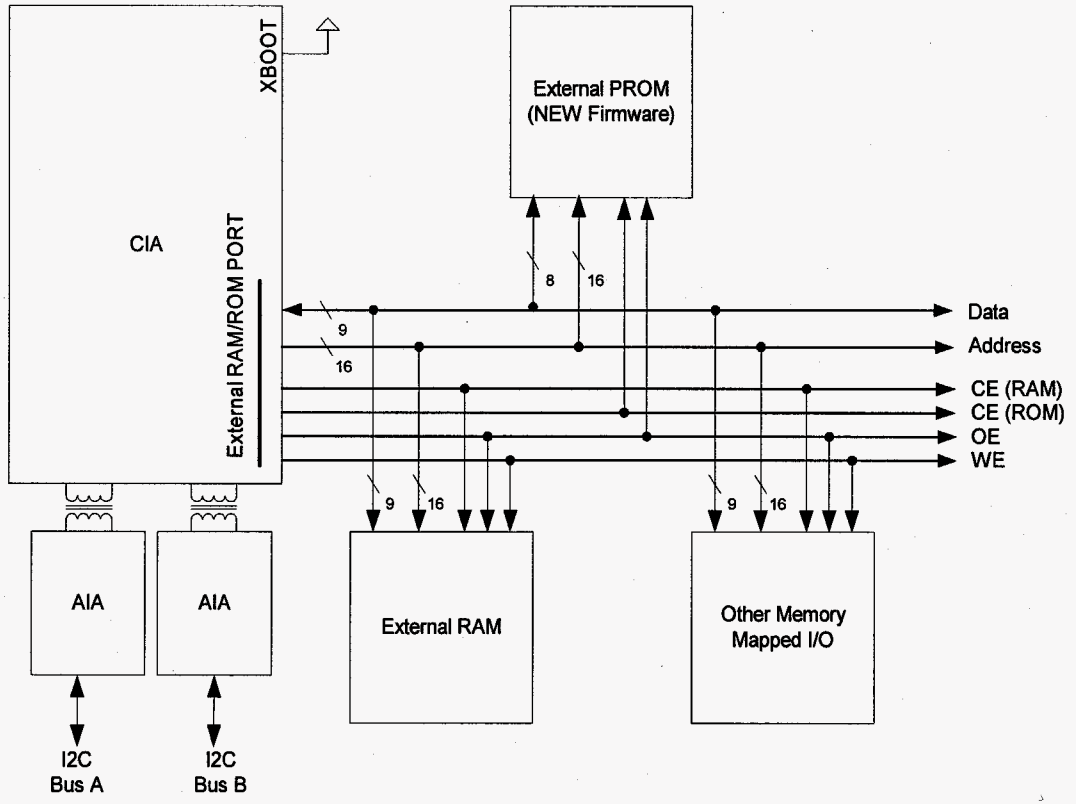
AIA Functional Description

- Power
- I2C Bus Interface
- I2C Transformer Interface
- Power-On-Reset Circuitry
  - Generates sequenced resets used within the ASIC to reset all internal logic.
- Fail-Silent Timer
  - Disables the chip-set's ability to communicate on the I2C Bus
  - Requires active connect signal from CIA.
  - Chip reset will disable communications as well.
- Internal Oscillator and Support Circuitry
  - Used to modulate and demodulate the signals to and from the CIA over the transformers.
  - Oscillator Watchdog will result in Fail-Silent timeout.



Other Applications - Connection

- Pull XBOOT High for External BOOT ROM/PROM
- Connect both RAM and ROM Modules to same bus
- Flexible Read Access Time Requirement for External PROM (Adjustable)
- Connect up to:
  - 32 KB of Additional RAM
  - 32 KB of Additional ROM
- External Bus Connectivity
  - 8-bit Data and 1-bit Parity
  - 16-bit Address
  - 1 Chip Enable (RAM)
  - 1 Chip Enable (ROM)
  - 1 Output Enable (Both)
  - 1 Write Enable (RAM)



Other Applications - Possibilities

- Instrument Interface
  - Provide reliable Isolated bus interface to low data rate instrument (Science or GNC) such as reaction wheels.
- Remote Engineering Unit
  - Typically remote from C&DH Chassis, thus requiring a convenient, yet reliable bus interface.
  - Responsible for remote data collection and minimal discrete commanding.
- In-Flight Reprogram-ability
  - Use of an EEPROM with this chip-set would allow for a modification to the code while in flight, thus providing a measure of reconfigurability.

Summary

- **Designed to provide a flexible solution to power switching and power bus regulation.**
  - **Power Switch Slice**
  - **Power Control Slice**
- **Open-Systems Architecture allows for other powerful applications**
  - **Robust Infrastructure**
    - Embedded Microcontroller (8051 – 2 clock cycles/instruction)
    - Fault Protection Logic and Timers
    - Embedded 8-bit ADC
    - Redundant and Fault Tolerant Custom and Standard I2C bus connection
  - **Adaptable Architecture**
    - Firmware Completely Replaceable
    - Additional RAM can be added.
    - Other Memory Mapped I/O can be added

Acknowledgements

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