

Frequency Dependence of Single-Event Upset in Advanced Commercial PowerPC Microprocessors

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35-WORD ABSTRACT:

Single-event upset from heavy ions is measured for advanced commercial microprocessors in a dynamic mode with clock frequency up to 1GHz. Frequency and core voltage dependence of single-event upsets in registers is discussed.

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I. Introduction

Typically Single-Event Upset (SEU) testing involves writing a test pattern into the storage elements (such as registers and Cache), irradiating the part with heavy ions, and then reading the storage element states to determine the number of SEUs. Obviously, clock frequency has no effect on static measurements of this kind. However, in dynamic measurements, if the memory is continuously written to and read during irradiation, clock frequency is expected to affect the cross section because there is a larger probability that transients from logic operator will overlap clock edge transitions.

Clock frequency is important when measuring dynamic SEUs in an integrated circuit (IC) along with the extent of using various regions of the processor. Recent experiments have demonstrated that the occurrence of SEUs in IC's increases with increasing clock frequency [1, 2, 3]. With clock frequencies constantly increasing, the concern about dynamic SEUs is becoming an important factor. Therefore, it is important to understand the mechanisms responsible for dynamic SEUs in IC's, as well as their dependence on clock frequency. These dynamic measurements are difficult to do, primarily because of the difficulty of isolating dynamic SEUs in IC's exposed to ion beams at accelerators.

Previously, we reported SEU measurements for SOI commercial PowerPCs with feature size of 0.18 and 0.13 μm [4, 5]. These results show an order of magnitude improvement in saturated cross section compare to CMOS bulk counterparts. Those measurements were done while the processor was in a static mode.

Recently, we have extended our SEU studies to dynamic conditions; varying the clock frequency. Only limited data is available in the literature for clock frequency dependence of the SEU of microprocessors. In Ref. [6, 7] the clock frequency dependence of the SEU of the Alpha microprocessor under use conditions has been investigated. Their measurements were limited to a clock frequency of 400 MHz and focused on the different failure trends for random core logic and the cache. Also, in Ref. [8] a direct comparison of SEU

sensitivities of the same generation SOI and CMOS bulk microprocessor was made. They performed their measurements in dynamic mode for clock frequency of 133 MHz.

This paper examines single-event upsets in advanced commercial SOI microprocessors in a dynamic mode, studying SEU sensitivity of General Purpose Registers (GPRs) with clock frequency. Results are presented for SOI processors with feature sizes of 0.18 μm and two different core voltages.

II. EXPERIMENTAL PROCEDURE

A. Device Descriptions

The Motorola 7455 is the first generation of the PowerPC family to be fabricated with SOI technology. They use a partially depleted technology without body ties. The 7455 has a feature size of 0.18 μm with a silicon film thickness of 110 nm and internal core voltage of 1.6 V. A low power version of this processor operates with an internal core voltage of 1.3 V. These devices are packaged with "bump bonding" in flip-chip BGA packages.

Table I show how the recent SOI generations of the PowerPC family compare with previous bulk generations. The feature size of the SOI Motorola PowerPC is reduced from 0.29 to 0.13 μm , with the core voltage reduced from 2.5 to 1.3 V. The larger die sizes of the SOI PowerPCs are due to the more advanced design. The processors tested are highlighted in gray in table I.

Table I. Summary of Motorola's PowerPC Family of Advanced Processors.

Device	Feature Size (μm)	Die Size (mm^2)	Core Voltage (V)	Maximum Operating Frequency (MHz)
750 (G3)	0.29	67	2.5	266
7400 (G4)	0.20	83	1.8	400
7455 (SOI)	0.18	106	1.6	1000
7455* (SOI)	0.18	106	1.3	800
7457 (SOI)	0.13	98	1.3	1000

* This is a special low power version of the Motorola SOI PowerPC 7455.

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B. Experimental Methods

Radiation testing was done at the Texas A&M cyclotron. Because of the "flip-chip" design of the Motorola PowerPC irradiations were done from the

back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. The thickness of die is about 850 μm . Irradiations were done in air utilizing 40 MeV/amu ^{20}Ne and ^{49}Ar ions. Both ions have enough range to penetrate the die. The LET range of 1.7 to 15 MeV-cm²/mg was covered in the measurements.

Radiation testing was done using the "Sandpoint" development board. This eliminated the large engineering effort required to design a custom test board for the processor. It also provided a basic PROM-based system monitor instead of a complex operating system. This provides better diagnostics and control of processor information during SEU testing compared to more advanced operating systems. The external communication channel on this board is a simple serial connection used as a "dumb" terminal and a JTAG port. An Agilent Technology 5900B JTAG probe was used for our tests. This probe made it possible to interrogate the processor even after unexpected events occurred (such as operational errors during irradiation).

Register tests were done with special "loop" software. The loop performed the following steps:

- 1- Load a GPR with the operand 0x55555555 (multiplicand).
- 2- Load the next GPR with operand 0x2 (multiplier).
- 3- Multiply the registers together and write the result into the first register.
- 4- Increment the register pointer (now the second becomes the multiplicand and a third GPR is the multiplier) and repeat the step 1 to 3, until all the GPR hold multiplication results.
- 5- Read the entire GPR and check that the result agrees with expected value of 0xaaaaaaaa.
- 6- If not, then log the result to external memory as a strip chart (for later read out after the current irradiation is complete).

There were three outcomes;

- 1- The test passes and no upset is recorded.
- 2- The result does not match the expected value, but only one or two bits are wrong so this is counted as a *register* upset.
- 3- The result does not match the expected value, but many bits are erroneous which is counted as *processing unit* upset because it occurred, for example, in the Arithmetic Logical Unit (ALU) or in the register addressing logic.

In this method the registers are continuously being read and written and the ALUs are kept busy. These

upset results and discussions of their implications are the focus of the present paper. In particular, the results at two frequencies (350 and 1000 MHz) and two operating voltage (1.6 and 1.3 Volts) are compared. Additional data were taken on functionality of the test program under irradiation and results follow on failures due to processor malfunctions (hangs) at both frequencies and voltages.

Future dynamic testing is planned that will exercise heavily the data cache which is likely to make the largest contribution to upset rates for most real applications.

III. TEST RESULTS

A Clock Dependence

Fig.1 shows results of the SEU cross section measurements for the Motorola SOI PowerPC 7455 in a dynamic mode. The clock frequency for this measurement is 350 MHz and the operating voltage is 1.6 V. In this figure we display the upsets from Registers, ALU and total upsets (sum of upsets from Registers and ALU). Clearly, the main contribution to the SEU is from the upsets in the registers. However, there is also some contribution from the ALU unit to the SEUs at higher LETs.

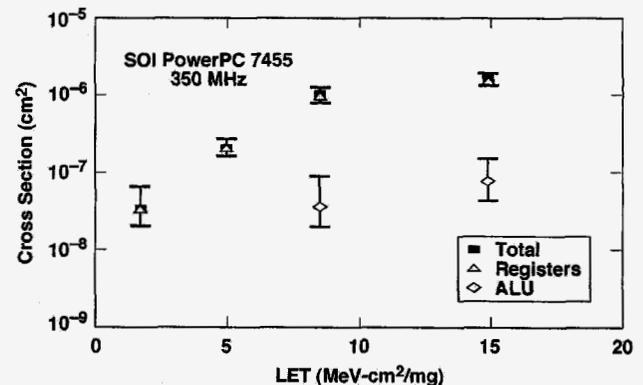


Fig. 1 Heavy-ion cross-sections register of the Motorola SOI PowerPC 7455 for dynamic mode.

Static measurement reveal that the SEU cross section increases with increasing LET, eventually reaching a saturation level at high LETs [4,5]. The same behavior is seen in the dynamic measurements.

In Fig. 2, we compare the SEU measurements for the Motorola PowerPC 7455 at two clock frequencies; 350 and 1000 MHz. At very low LET counting statistics prevent conclusive interpretation. However, for the higher LETs the results with 1000 MHz clock frequency are systematically larger by almost a factor of 2 compared with the results for a clock frequency of 350 MHz. This indicates that

there is a clock dependency in SEU measurement of the registers.

Fig. 3 compares the SEU measurements for ALU unit at clock frequencies of 350 and 1000 MHz. Although, the counting statistics are low, data shows a slight clock dependency in the SEU measurements of the ALU. The results with clock speed of 1000 MHz are systematically larger compare with the results for clock speed of 350 MHz.

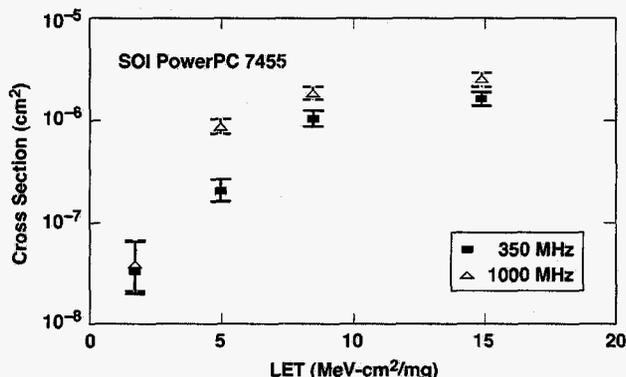


Fig. 2. Comparison of SEU cross-sections for registers with clock speed of 350 and 1000 MHz.

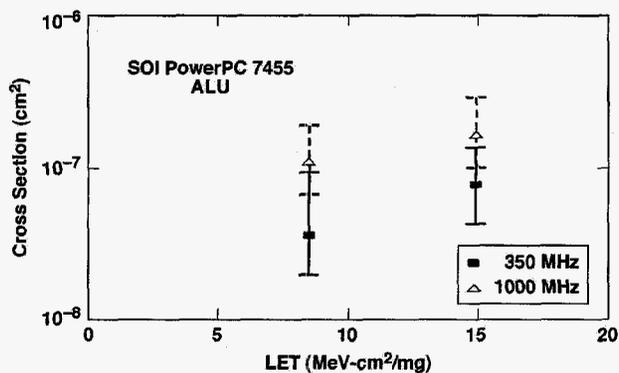


Fig. 3. Comparison of SEU cross-sections for ALU with clock speed of 350 and 1000 MHz.

We also repeated SEU measurements on a special version of the Motorola PowerPC 7455 that operates with lower internal core voltage specification; of 1.3 V. Similar clock frequency dependence was observed for the ALU contribution.

B Core Voltage Dependence

Fig. 4 compares the result of the dynamic SEU measurements on the Motorola PowerPC 7455 with core voltage of 1.6 V with the results of the Motorola PowerPC 7455 with a core voltage of 1.3 V. The SEU cross section with lower operating voltage, 1.3 V, is larger than the SEU for operating voltage of 1.6 V.

C Functional Errors (“Hangs”)

We also examined complex functional errors (“hangs”) where the processor operation is severely disrupted during irradiation. We detected “hangs” by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, it was still operational to the point where normal software means could likely restore operation.

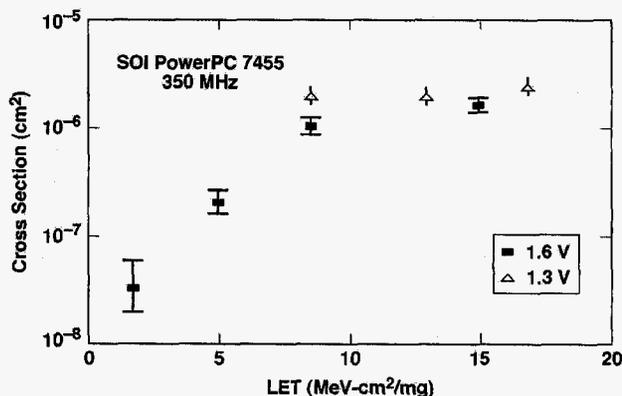


Fig. 4. Comparison of SEU cross-sections for internal core voltage specifications of 1.3 and 1.6 V at clock speed of 350 MHz.

If the interrupt could not restore operation, then the status was categorized as a “hang.” In nearly all cases, it was necessary to temporarily remove power from the device in order to recover, and reboot the device.

In order to evaluate “hangs,” we calculated the “hang” cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed, including runs with no observed “hangs.” This was done for each LET. Figure 5 compares estimated cross section for “hangs” for two internal core voltage specifications during heavy-ion SEU measurements of the PowerPC 7455. The threshold LET appears comparable to that obtained for register and errors. The SEU cross section for two measured clock speed is statistically the same and there is no clock dependence in the estimated cross section for “hang”.

Although the *threshold* LET for “hangs” is low, the cross section is small enough so that the expected incidence of “hangs” is not very high in typical space environments.

IV. DISCUSSION

Seifert *et al.*, measured the frequency dependence of alpha-particle induced SEU in the 21164 Alpha microprocessor [6]. They found that the SEUs of the cache (which has no dynamic latch nodes) increase with frequency. However, their results suggest that SEUs in the Alpha core logic decrease with increasing

clock rate and are dominated by the contribution from dynamic latch nodes. This is consistent with our results for the General Purpose Registers (GPR). It is also consistent with the expectations and explanation of Buchner *et al.* [2], that errors are caused by single event transients in coincidence with vulnerability

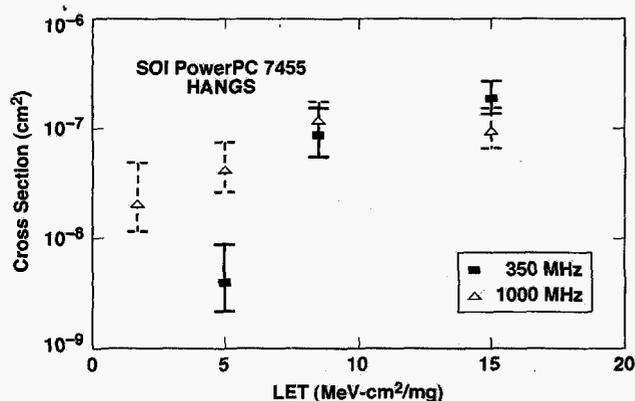


Fig. 5. Comparison of SEU cross-sections for "hangs" with clock speed of 350 and 1000 MHz.

windows associated with clock edges and that increase proportionally with frequency. The latter, more surprising, observation (an increase in SEUs for higher frequencies) appears to be the result of the lowering of the critical charge for upset for storage elements implemented in dynamic logic, at least as implemented by the Alpha design.

Consider what dynamic upset testing of a processor really measures. Typical use of the term "dynamic" implies running a program and comparing the expected result with the actual result, counting an error when they are not the same. In practice, such a test measures both the static cross sections of the bits that it uses (i.e., clock independent errors) and the dynamic cross sections of logic units (i.e., clock-dependent errors). Note, however, that not all bits within a microprocessor are used in typical programs. Further, the bits are actually storing data only for a portion of the time that the program takes to run. Thus a dynamic test is an admixture of static and dynamic contributions.

Our previous static SEU cross sections for GPR [4] were measured by a test program designed to yield near the ideal case of 100% register duty cycle. Results from our new dynamic test program provide per bit cross sections that are only about 40% of the "full" static results reported previously. This is consistent with our estimated register duty cycle of the dynamic test program.

It is important to evaluate single-event upset for different types of internal and storage elements because the overall upset rate of an operational

program in real live application depends how the various types of storage elements are used as well as their cross sections.

V. CONCLUSION

This paper has evaluated SEU cross section at different clock speed using a dynamic test program at clock frequencies up to 1 GHz. The cross section increases by as much as a factor of two at maximum clock frequency. Similar results were obtained for two versions of the PowerPC with different core voltages. The upset cross section is dominated by the registers; the ALU contributes very little to the SEU.

These results have important implications as clock frequencies are increased to even higher levels. At this point the dependence on dynamic operation – at least for this particular processor – is relatively small, with little overall impact to system SEU rates. However, the frequency dependence may become larger for future generations or other specific circuits. Dynamic tests should be included in SEU tests of microprocessors or other complex circuits.

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