

Design of an auto-zeroed, differential, organic thin-film field-effect transistor amplifier for sensor applications

David M. Binkley^{*a}, Nikhil Verma^a, Robert L. Crawford^a, Erik Brandon^b, and Thomas N. Jackson^c

^aUniversity of North Carolina, Charlotte, NC 28223

^bNASA Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109

^cPennsylvania State University, University Park, PA 16802

ABSTRACT

Organic strain gauge and other sensors require high-gain, precision dc amplification to process their low-level output signals. Ideally, amplifiers would be fabricated using organic thin-film field-effect transistors (OTFT's) adjacent to the sensors. However, OTFT amplifiers exhibit low gain and high input-referred dc offsets that must be effectively managed. This paper presents a four-stage, cascaded differential OTFT amplifier utilizing switched capacitor auto-zeroing. Each stage provides a nominal voltage gain of four through a differential pair driving low-impedance active loads, which provide common-mode output voltage control. p-type pentacene OTFT's are used for the amplifier devices and auto-zero switches. Simulations indicate the amplifier provides a nominal voltage gain of 280 V/V and effectively amplifies a 1-mV dc signal in the presence of 500-mV amplifier input-referred dc offset voltages. Future work could include the addition of digital gain calibration and offset correction of residual offsets associated with charge injection imbalance in the differential circuits.

Keywords: Organic thin-film field-effect (OTFT) amplifiers, large-area electronics, organic sensors, dc offset cancellation, auto-zero circuits, differential amplifiers, analog circuits, switched-capacitor circuits

1. INTRODUCTION

Organic thin-film field-effect transistors (OTFT's) have found application in recent years in low-cost, large-area electronics. OTFT's are flexible and can be fabricated at lower temperatures compared to other thin-film devices making them attractive for large-area applications. Pentacene has been the most promising organic semiconductor material and can be used for p-type semiconductor devices. Organic devices can also be used to fabricate sensors. These sensors have the potential of being integrated with OTFT amplifier and signal processing circuits on the same flexible, low-cost substrate.

Some reported sensors include chemical sensors¹, pH sensors², gas sensors^{3, 4, 5}, humidity sensors^{6, 7, 8}, bio sensors, and strain sensors⁹. When the active organic layer is exposed to the environment, changes in bulk conductivity, or OTFT field-induced conductivity or threshold voltage permit electrical readout. Another application of large-area organic devices is solar sails for potential space applications. These devices utilize a large, thin membrane to gain momentum from impinging photons of light from the sun to provide propulsion. Monitoring sensors can be integrated on the surface of the sail to monitor its temperature, strain, charge build up, radiation exposure, and other critical aspects of its health¹⁰.

This paper is organized as follows. *Section 2* describes analog amplification requirements for large area, organic strain-gauge sensor applications considered here. *Section 3* describes the technology and performance of OTFT's considered in amplifier circuits presented in this paper. *Section 4* describes an OTFT differential amplifier building block having deliberate low voltage gain and inherent output common-voltage control. This permits operation with OTFT's having large processing variations and large dc mismatches. *Section 5* presents a cascaded, four-stage amplifier utilizing the differential amplifier building block with switched capacitor output auto-zeroing. OTFT's are utilized in the amplifiers and switches. Simulations using OTFT models indicate the composite amplifier can accurately amplify a 1-mV dc sensor signal in the presence of 500-mV amplifier input-referred dc offsets. Finally, *Section 6* provides a concluding summary

* dmbinkle@uncc.edu; Phone: 704-687-4392; Fax: 704-687-2352.

and suggestions for future research. Future work includes possibilities of digital gain correction and correction of dc-offset errors associated with unbalanced charge injection in the differential circuits.

2. ANALOG CIRCUIT REQUIREMENTS

While signal processing requirements change as sensors are refined and system level specifications evolve, the following are target analog circuit requirements for the large area, strain-gauge sensor applications considered here.

- Operating Input Signal Level: as low as 1 mV (dc)
- DC Gain: 100 to 1000 V/V (sufficient to amplify the sensor signal for subsequent processing)
- DC Input-Referred Offset: $\ll 1$ mV (including OTFT offsets of 500 mV)
- Bandwidth: < 1 kHz (the physical measurement is sufficiently slow to permit OTFT's)
- Controllability: $< 1\%$ variation in gain over the operating environment (this anticipates system-level digital calibration)

3. ORGANIC THIN-FILM FIELD-EFFECT TRANSISTORS FOR ANALOG APPLICATIONS

3.1 Fabrication

OTFT's are three terminal devices consisting of a source, drain, and gate contact. An organic semiconductor material extends between the source and drain providing a semiconductor channel. A gate, separated by an insulator, extends above or below the organic semiconductor to set up a vertical electric field between the gate and the semiconductor channel. Here, bottom gate pentacene p-type OTFT's are considered with the construction shown in Fig. 1.

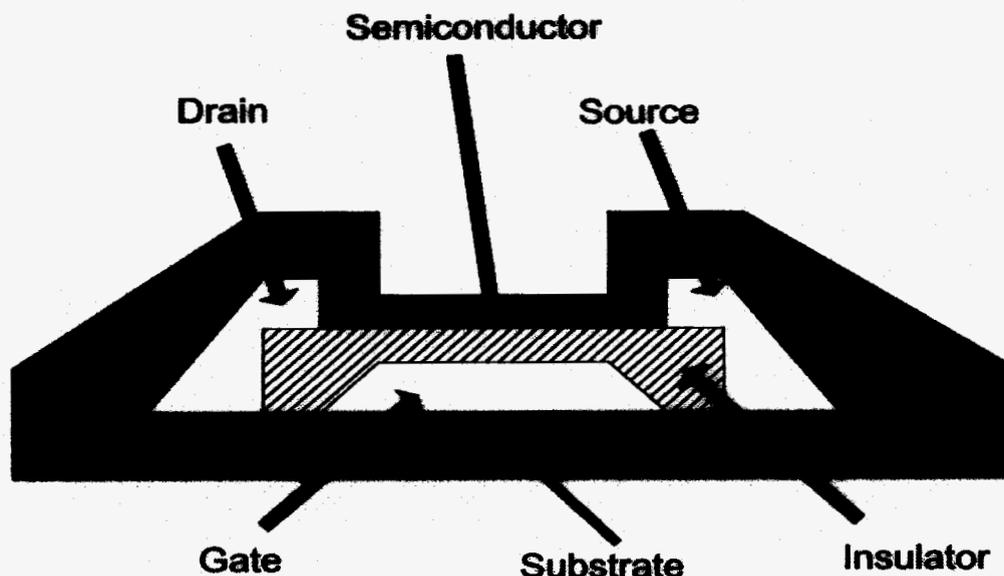


Fig. 1. Cross-sectional diagram of bottom gate OTFT¹¹.

The p-type pentacene OTFT's considered here have the same characteristics as those fabricated by Kane et al¹². The substrate material was a 75- μm thick transparent, flexible polyethylene naphthalate (PEN) film mounted on a removable glass support. The gate dielectric was SiO_2 with thickness of 190 nm. Nickel gate and palladium source-drain metallization was used. The gate dielectric surface was vapor-treated with octyldecyltrichlorosilane and then followed by thermal evaporation of the pentacene channel at a substrate temperature of about 60°C. The maximum processing temperature was 110°C following a two-hour heat treatment at 150°C to improve thermal dimensional stability. Further details of the pentacene OTFT process can be found elsewhere^{12, 13}.

3.2 Operation

OTFT devices operate in a similar manner to metal oxide semiconductor field-effect transistors (MOSFET's) where current flows between the drain and source under field-effect control established by the gate electrode. In a MOSFET, however, electrons (n-type MOSFET's) or holes (p-type MOSFET's) are drawn into the channel from the substrate to supply a source of mobile charge carriers. In OTFTs, charge is accumulated in the doped organic semiconductor channel under gate electrode control¹⁴.

OTFT drain current¹⁴ can be expressed like MOSFET strong-inversion drain current in saturation ($V_{DS} > V_{DSAT}$) as

$$I_D = \frac{1}{2} \mu C'_{OX} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad (1)$$

where μ is the channel carrier mobility, C'_{OX} is the gate-oxide capacitance per unit area, λ is a parameter describing the increase of drain current with drain voltage, W is the channel width, and L is the channel length.

3.3 Analog design considerations

Equation (1), identical in form to MOSFET strong-inversion drain current in saturation, suggests OTFT's may be readily used for analog and digital circuit design. However, the mobility of OTFT's is almost 1,000 times smaller than MOSFET's¹⁴. p-type pentacene OTFT's have reported mobilities¹⁵ around $1 \text{ cm}^2/\text{Vs}$, but operating mobilities, especially at lower supply voltages, are typically below this level. n-type OTFT's using channel materials such as crystalline sexithiophene have mobilities that are even an order-of-magnitude lower. The low mobility of OTFT's results in low small-signal transconductance, $g_m = \partial I_D / \partial V_{GS}$, giving low gain and bandwidth compared to MOSFET's. p-type OTFT's are typically used for active circuit elements because of their higher mobilities compared to n-type devices. n-type devices, however, might be usable as active loads where high small-signal load resistance associated with low transconductance could provide higher voltage gain.

In digital circuits, the low mobility of OTFT's give circuit speeds well below those for MOSFET circuits. A five-stage ring oscillator¹ has been reported running at 1.7 kHz at a supply voltage of 20 V. A seven-stage ring oscillator¹⁶ has also been reported running at 106 kHz at a supply voltage of 80 V. Here, the OTFT devices utilize a top gate, a p-type soluble polymer (regio-regular poly, 3-alkylthiophen) semiconductor layer, and a soluble polymer gate insulator. Reported digital circuit speeds suggest analog circuit bandwidths in the 1 – 100 kHz range, as obtained in the differential amplifiers described later in this paper.

Mismatch in devices, long considered important in analog MOSFET design, results in dc errors between identically laid out devices. This causes input-referred dc offsets in the range of 2 – 10 mV for typical analog MOSFET circuits with the actual offset depending upon the process and size of the device used. Larger area devices, where local processing variations are averaged out, result in lower mismatch¹⁷. Mismatch, however, in OTFT's devices can be substantially higher than that of MOSFET devices¹⁸ approaching levels as high as 500 mV. As described later, analog circuits must operate without signal saturation caused by large device mismatches. Additionally, auto-zeroing or other techniques are required to manage the high levels of input-referred dc offset.

OTFT devices require substantially higher supply voltages compared to modern MOSFET circuits. p-type pentacene OTFT's use gate and drain voltages of 10 to 20 V or higher as illustrated in reported device dc characteristic curves^{12, 14, 16, 19}. The higher supply voltages, while clearly a disadvantage for miniature integrated systems, is less a disadvantage for large-area organic sensor and electronic systems.

Finally, while mobility, transconductance, bandwidth, dc mismatch, and operating voltages are much less favorable for OTFT devices compared to MOSFET's, OTFT's, like MOSFET's, have high on-off resistance ratios when used as switches in the deep linear, triode, or ohmic region ($V_{DS} \ll V_{DSAT}$). On-off ratios of pentacene channels have been reported near 10^8 when deposited on octyldecyltrichlorosilane treated silicon¹⁵. These OTFT's have a threshold voltage near 0 V and a sub-threshold swing less than 2 V/decade. The four-stage, auto-zeroed differential amplifier described later utilizes pentacene OTFT's as switches.

4. DIFFERENTIAL AMPLIFIER GAIN BLOCK

4.1 Device modeling

The four-stage, auto-zeroed differential amplifier described here was designed for the pentacene OTFT devices reported by Kane et al.¹² and described in Section 3.1. An AIM SPICE model²⁰ was developed to model these devices. The devices are depletion mode, p-type pentacene OTFT's having threshold voltages of +7 V and field-effect mobilities of approximately $0.6 \text{ cm}^2/\text{Vs}$. Fig. 2 shows simulated curves for a $W = 25 \text{ }\mu\text{m}$, $L = 20 \text{ }\mu\text{m}$ device, which closely match the measured device curves for the same size device¹².

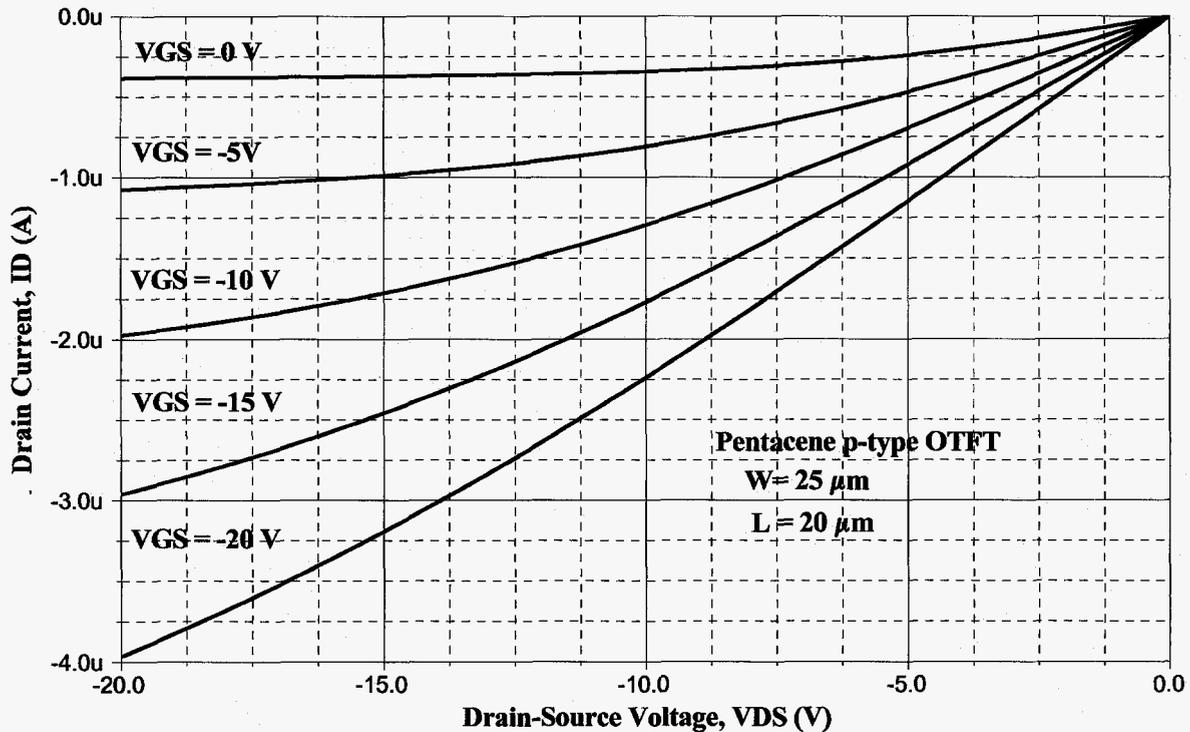


Fig. 2. Simulated device curves for a p-type pentacene OTFT having $W = 25 \text{ }\mu\text{m}$ and $L = 20 \text{ }\mu\text{m}$. These device curves closely match measured data¹².

4.2 Amplifier design

A differential amplifier using the p-type pentacene OTFT's considered here was reported by Kane et al.¹² This amplifier used a differential pair with active OTFT current-source loads to achieve a measured voltage gain of 8.5V/V at supply voltages of +10 V and -20 V. Additionally, a five-stage ring oscillator was reported having operating frequencies of 1.1 and 1.7 kHz.

In the differential amplifier gain block described here, we chose to use low-impedance active loads consisting of connections to the sources of grounded-gate OTFT devices. This ensures output common-mode voltage control since these loads operate at predictable gate-source voltages. Voltage gain is reduced to approximately 4 V/V, but is less sensitive to process variations as described later. Additionally, the lower voltage gain helps ensure the amplifier stage will not saturate on its own input-referred offset voltage, which is expected to approach 500 mV for OTFT devices. Four low gain stages are used to achieve a composite gain of approximately 260 V/V.

Fig. 3 shows a schematic diagram of the OTFT differential amplifier gain block. Devices $M1$ and $M2$ comprise a differential pair connected to grounded-gate, source-connected active loads, $M3$ and $M4$. $M5$ operates as a current source providing bias current to the differential pair. Supply voltages of +10 V and -35 V are used along with a bias voltage of -20 V for the grounded-gate, source-connected active loads. Input common-mode voltage is at ground (0 V), and the

output common-mode voltage is approximately -14.6 V. The output common-mode voltage will be level shifted back to ground through output auto-zeroing described later. Supply current for the amplifier is $0.37 \mu\text{A}$ for a total power consumption of $16.7 \mu\text{W}$.

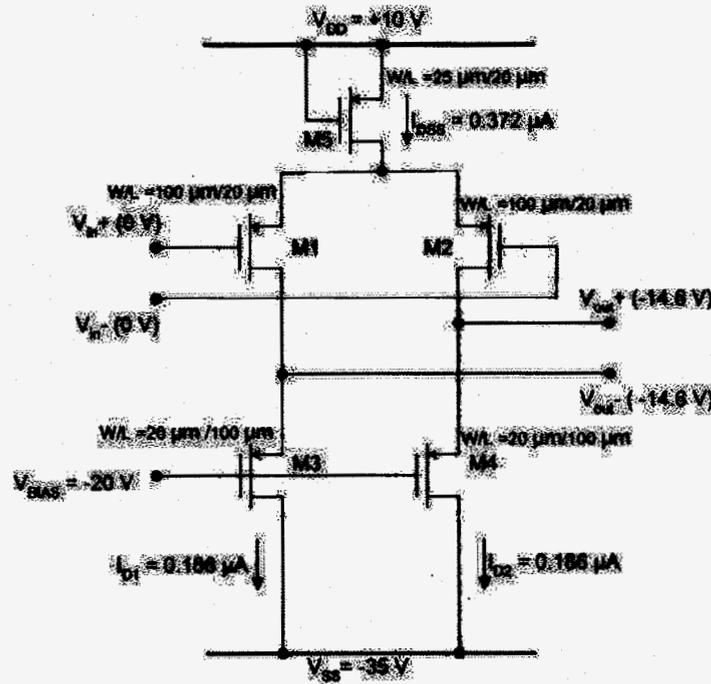


Fig. 3. Schematic diagram of OTFT differential amplifier gain block with dc bias voltages and currents.

Table 1 lists the sizing, W and L , drain current, I_D , effective gate-source voltage, $V_{EFF} = V_{GS} - V_T$, drain-source saturation voltage, V_{DSAT} , transconductance, g_m , and output conductance, g_{ds} , for the OTFT's in the differential amplifier. Active loads $M3$ and $M4$ are sized for g_m four times smaller than that of the differential pair devices, $M1$ and $M2$. This is required to obtain a voltage gain of four. V_{EFF} , V_{DSAT} , g_m , and g_{ds} were obtained from AIM SPICE simulations. Simulated V_{EFF} and g_m values are within 20% of square-law, hand calculated values.

Table 1. Sizing, bias current, effective gate-source voltage, drain-source saturation voltage, transconductance, and output conductance for OTFT's used in the differential amplifier.

Device	W (μm)	L (μm)	I_D (μA)	$V_{GS} - V_T$ (V)	V_{DSAT} (V)	g_m (μS)	g_{ds} (μS)
M1,M2	100	20	0.186	-2.303	-2.553	0.133	0.0006
M3,M4	20	100	0.186	-12.421	-12.463	0.027	0.002
M5	25	20	0.372	-7	-7.08	0.100	0.003

Small-signal voltage gain for the differential amplifier is given by

$$A_V = \frac{g_{m1}}{g_{m3} + g_{ds1} + g_{ds3}} = \frac{0.133 \mu\text{S}}{0.027 \mu\text{S} + 0.0006 \mu\text{S} + 0.002 \mu\text{S}} = 4.49 \text{ V/V} \quad (2)$$

where g_{m1} is the transconductance of the differential pair devices, $M1$ and $M2$, and g_{m3} is the transconductance of active load devices, $M3$ and $M4$. g_{ds1} and g_{ds3} are the output conductances of the differential pair and active load devices respectively. The small-signal voltage gain is predicted at 4.49 V/V and is dominated by the ratio of differential pair and load device transconductances. While the differential amplifier has relatively low voltage gain, a significant amount of

process variation compensation is expected since its gain is controlled by the ratio of differential pair and load device transconductances for similar (p-type) devices in the same process. Additionally, the gain is largely independent of device output conductances that vary widely with processing and temperature. As mentioned, low voltage gain has also been selected to ensure reliable output common-mode voltage levels and ensure high input-referred OTFT offset voltages will not saturate the amplifier.

Fig. 4 shows simulated signal voltages for the differential amplifier for a differential input swept from -5 V to 5 V at a common-mode input voltage level of ground. All devices are reliably in saturation, operating at drain source voltages above their drain-source saturation voltages ($V_{DS} > V_{DSAT}$). As mentioned, the operating gate-source voltages of load devices, $M3$ and $M4$, reliably establish the output common-mode voltage. This eliminates the need for complex common-mode feedback circuitry commonly used in high-gain, differential analog MOSFET circuits.

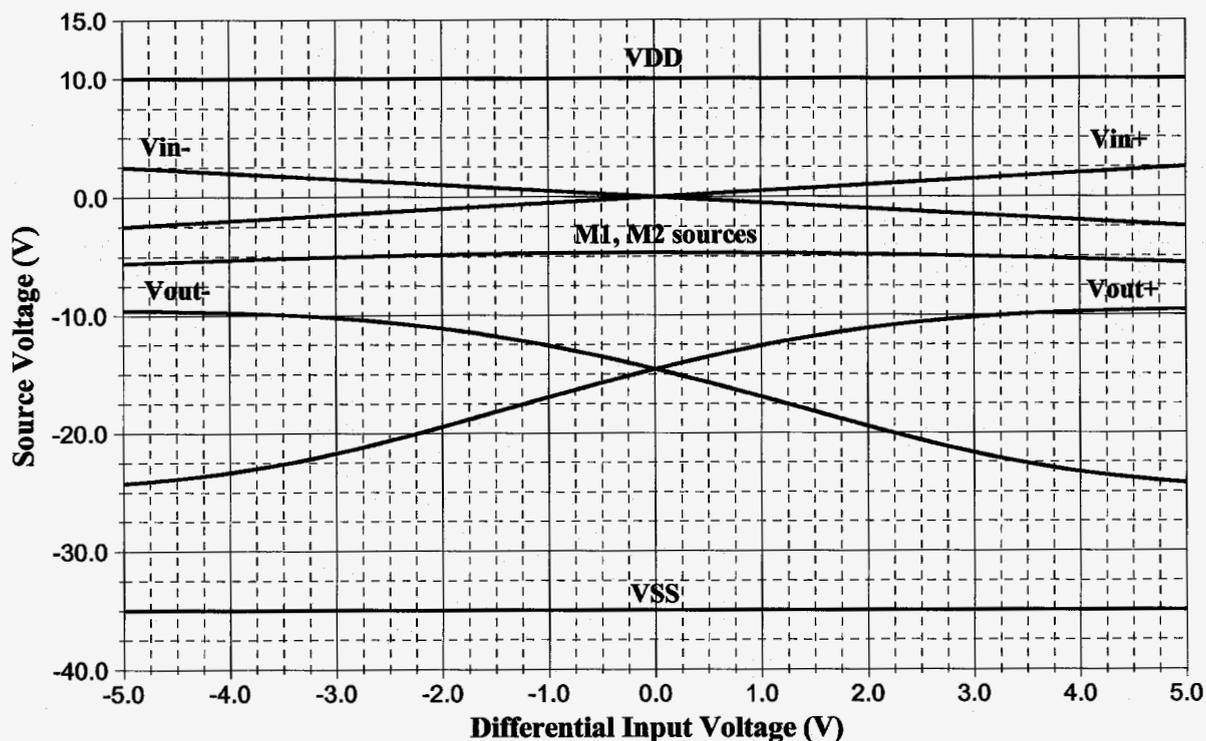


Fig. 4. Simulated signal voltages for the OTFT differential amplifier for a differential input of -5 V to 5 V at a common-mode input voltage of ground (0 V).

Fig. 5 shows the differential output voltage for a differential input swept again from -5 V to 5 V at a common-mode voltage level of ground. The amplifier has well behaved large signal characteristics and good linearity for inputs between -1 and 1 V. The simulated dc gain is 4.45 V/V, which closely matches the small-signal gain of 4.49 V/V predicted earlier.

Fig. 6 shows the simulated frequency response for the OTFT differential amplifier loaded by 0.5 -pF capacitors to emulate the capacitive loading of subsequent stages. Low-frequency voltage gain is 4.41 V/V, which closely matches the dc gain value (Fig. 5) of 4.45 V/V and small-signal gain calculation (Equation 2) of 4.49 V/V. The -3 dB frequency is 6.5 kHz, which is more than sufficient to support measurement of dc signals from organic sensors.

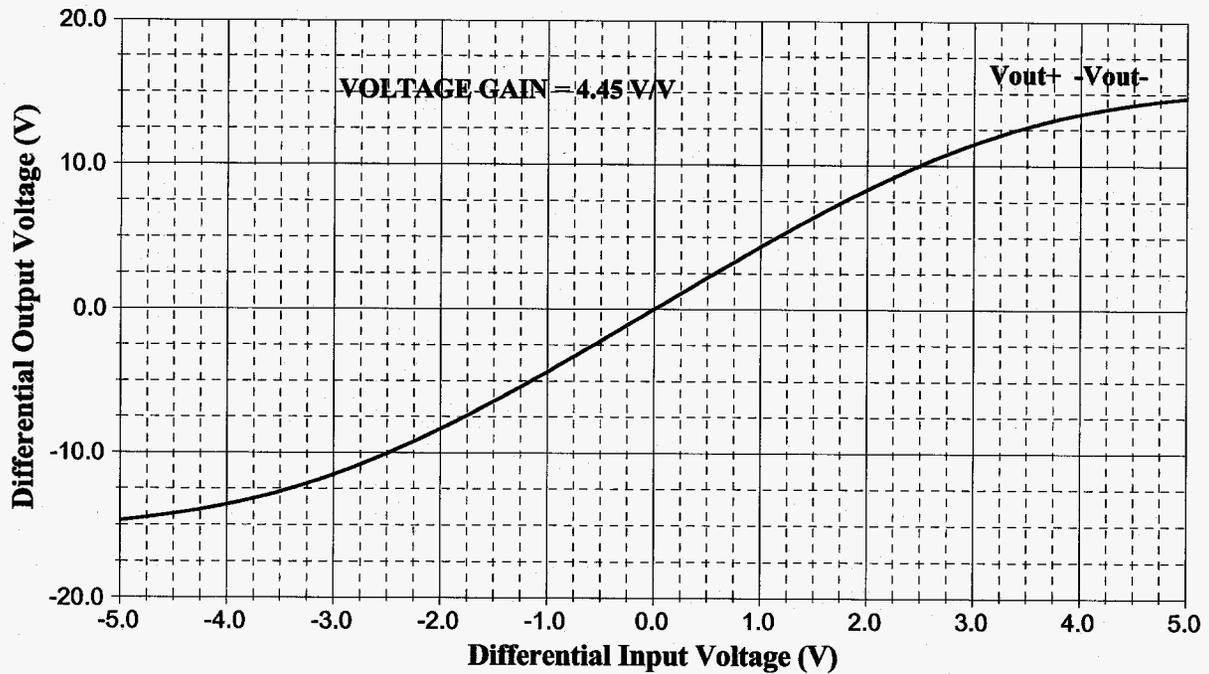


Fig. 5. Simulated dc transfer characteristics for the OTFT differential amplifier for a differential input of -5 to 5 V at a common-mode input voltage of ground (0 V).

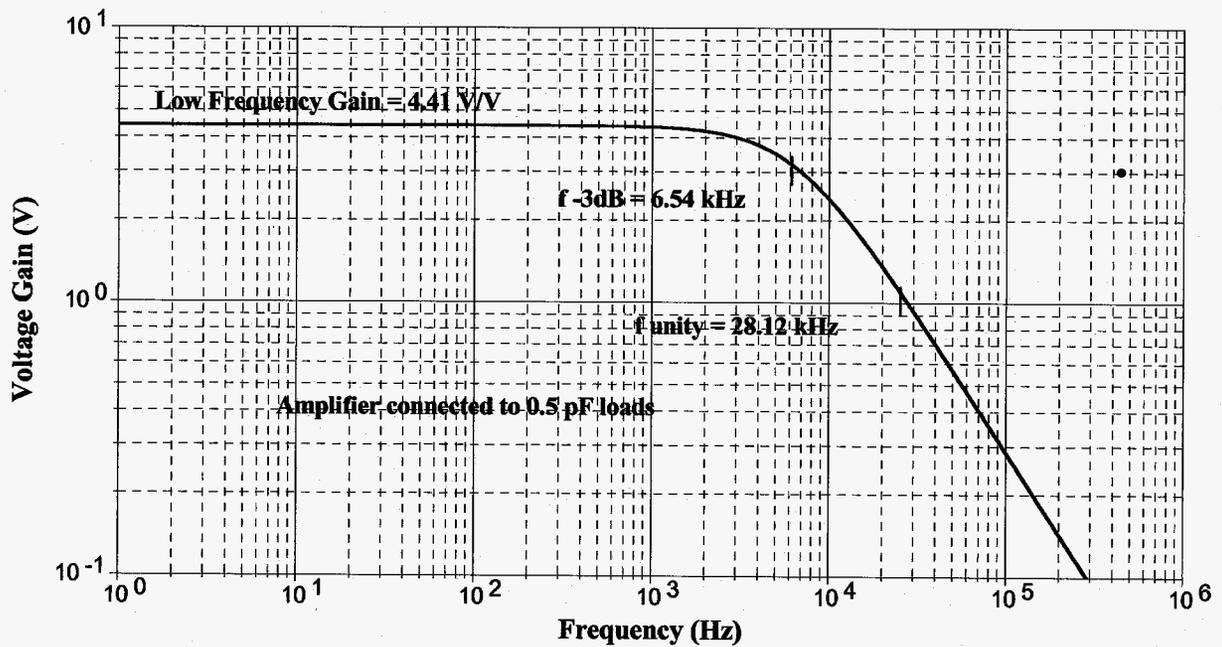


Fig. 6. Simulated frequency response for the OTFT differential amplifier.

5. FOUR-STAGE, AUTO-ZEROED DIFFERENTIAL AMPLIFIER

5.1 Single stage operation

OTFT differential amplifier input-referred dc offset is expected to approach 500 mV because of the large mismatch in OTFT devices. This offset will have to be effectively cancelled in order to amplify a sensor signal as small as 1 mV. In the design described here, we utilize output-offset cancellation that, in principal, permits complete cancellation of circuit offsets. This and other offset-cancellation methods used in MOSFET circuits are described in various books and papers^{21, 22}.

Fig. 7 shows a schematic diagram of output-offset cancellation applied to the OTFT differential amplifier. The circuit consists of the OTFT differential amplifier, six switches implemented using OTFT's, and two output-offset storage capacitors, which can be fabricated with the OTFT devices. The OTFT differential amplifier shows a 500-mV input referred offset voltage that is included in circuit simulations to verify its cancellation.

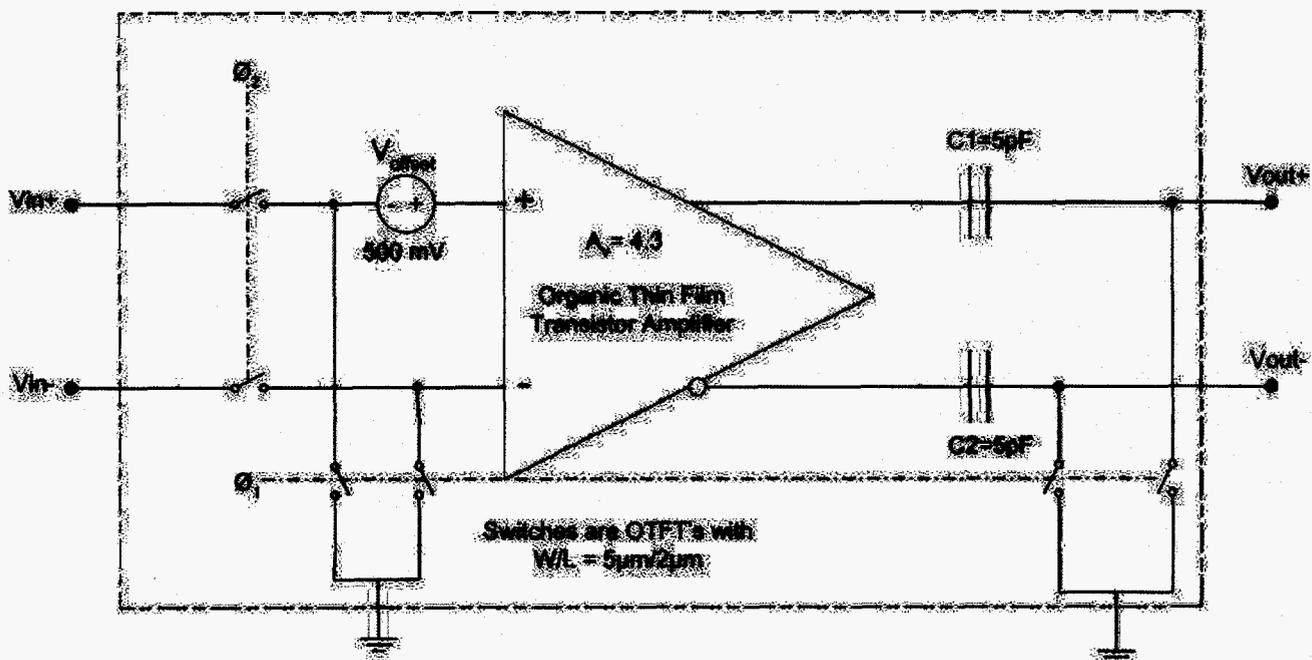


Fig. 7. Schematic diagram of output offset cancellation applied to the OTFT differential amplifier.

During the auto-zero phase, phase 1, the input signal is disconnected from the amplifier input by open series input switches while the amplifier input is grounded by closed input switches to ground. Series amplifier output capacitors, $C1$ and $C2$, are grounded at the main output signal by closed output switches to ground. During the auto-zero phase, the amplifier input-referred offset voltage is amplified by the amplifier and stored on the output capacitors along with the amplifier output common-mode voltage. For a 500-mV dc offset and a gain of 4 V/V, this corresponds to a differential output voltage of 2 V, well within the operating range of the amplifier as required.

During the signal phase, phase 2, the input signal is connected to the amplifier input by closed series input switches while the amplifier input is disconnected from ground by open input switches to ground. The main output signal on the right side of the output capacitors is released from ground by open output switches to ground. The amplifier now amplifies the desired input signal plus the undesired dc offset and presents this at its output on the left of the output capacitors. Since these capacitors were charged in the auto-zero phase to amplifier output voltages inclusive of the amplified offset voltage and the amplifier output common-mode voltage, both the amplifier offset and output common-mode voltage are removed in the final output signals. Unlike input-offset cancellation schemes, the offset is completely removed, in principal, using output-offset cancellation. Additionally, the output common-mode voltage is restored to

ground, which permits the auto-zeroed differential amplifier to directly drive a subsequent stage. Some output offset error, however, will exist because of unbalanced charge injection into the OTFT switches. If these switches are equal, charge injection on the positive side of the signal path will equal that on the negative side of the signal path and be cancelled when observing the differential output. Potential use of digital error correction for amplifier gain variations and removal of offset associated with non-ideal offset cancellation will be discussed later in the conclusions.

Fig. 8 shows the simulated differential output signal of the auto-zeroed OTFT differential amplifier for a 1-mV input signal in the presence of 500-mV input-referred dc offset. During the auto-zero phase, the output voltage is at 0 mV. During the signal phase, the output voltage is nearly 4 mV, four times the 1-mV input signal since the nominal differential amplifier voltage gain is four. The 1-mV input signal is clearly separated from the 500-mV input-referred offset voltage.

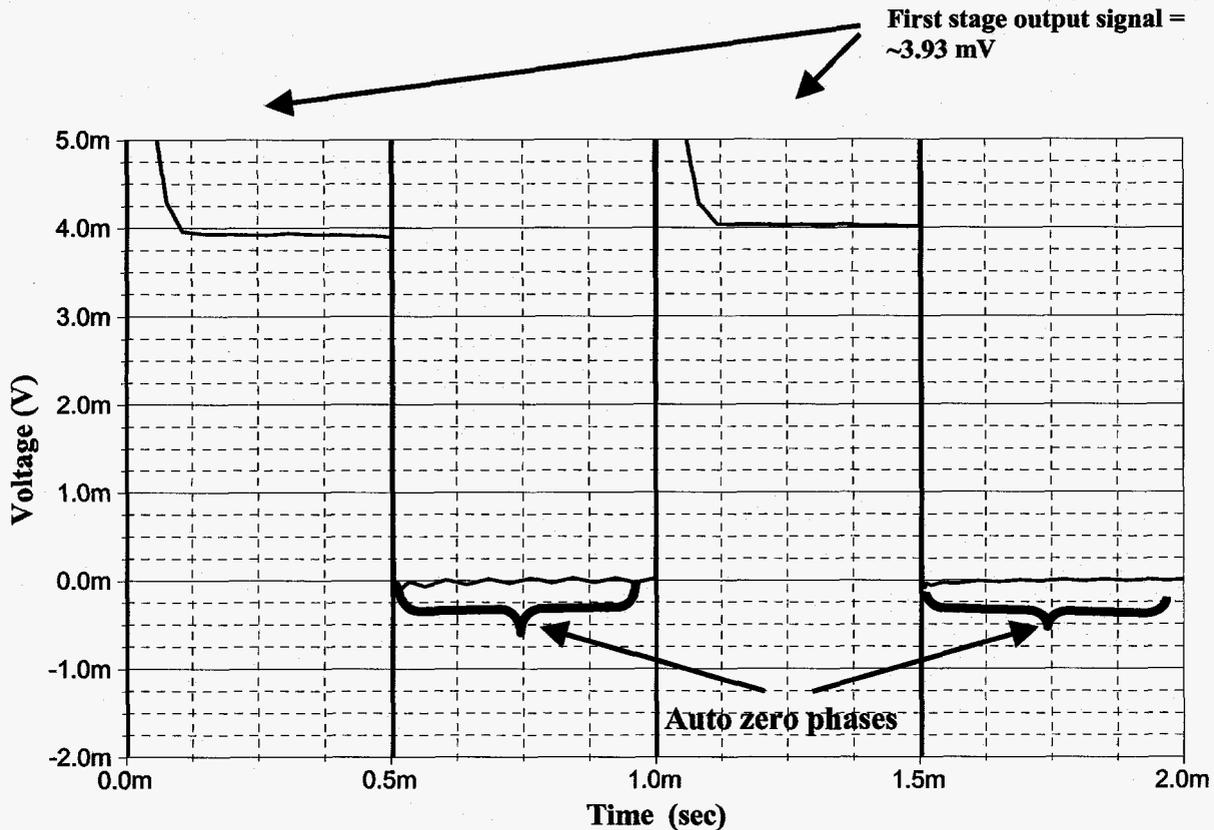


Fig. 8. Simulated differential output signal of auto-zeroed, differential OTFT amplifier for a 1-mV input signal in the presence of 500-mV input-referred dc offset.

5.2 Four stage operation

Four auto-zeroed, OTFT differential amplifier stages were cascaded to obtain a nominal voltage gain of 256 (4^4) V/V from nominal individual stage gains of 4 V/V. Each stage is simultaneously auto-zeroed (phase 1) and then placed into the signal mode (phase 2). As mentioned, output offset cancellation also level shifts the output common-mode voltage levels back to ground, which permits direct cascading of the auto-zeroed stages.

Fig. 9 shows the simulated differential output signals at each stage for a 1-mV input signal at the first stage. Individual stage input-referred offsets of 500 mV are included. During the auto-zero phase, the output voltages are at 0 mV. During the signal phase, the output voltages are 3.96, 16.57, 65.6, and 280 mV for stages 1 through 4 respectively. These levels follow the expected nominal stage gains of 4 V/V. As in the first stage illustrated in Fig. 8, the 1-mV input signal is accurately amplified in the presence of input-referred offsets a factor-of-five-hundred higher at 500 mV. The output signals also indicate that the -3-dB differential amplifier bandwidths of 6.5 kHz are sufficient for 500 μ s auto-zero and

signal phases. Output signal overshoots are due to charge injection in the OTFT switches. These transients are completely removed during the signal phase. The final output dc level can be captured and stored on external output capacitors using OTFT switches.

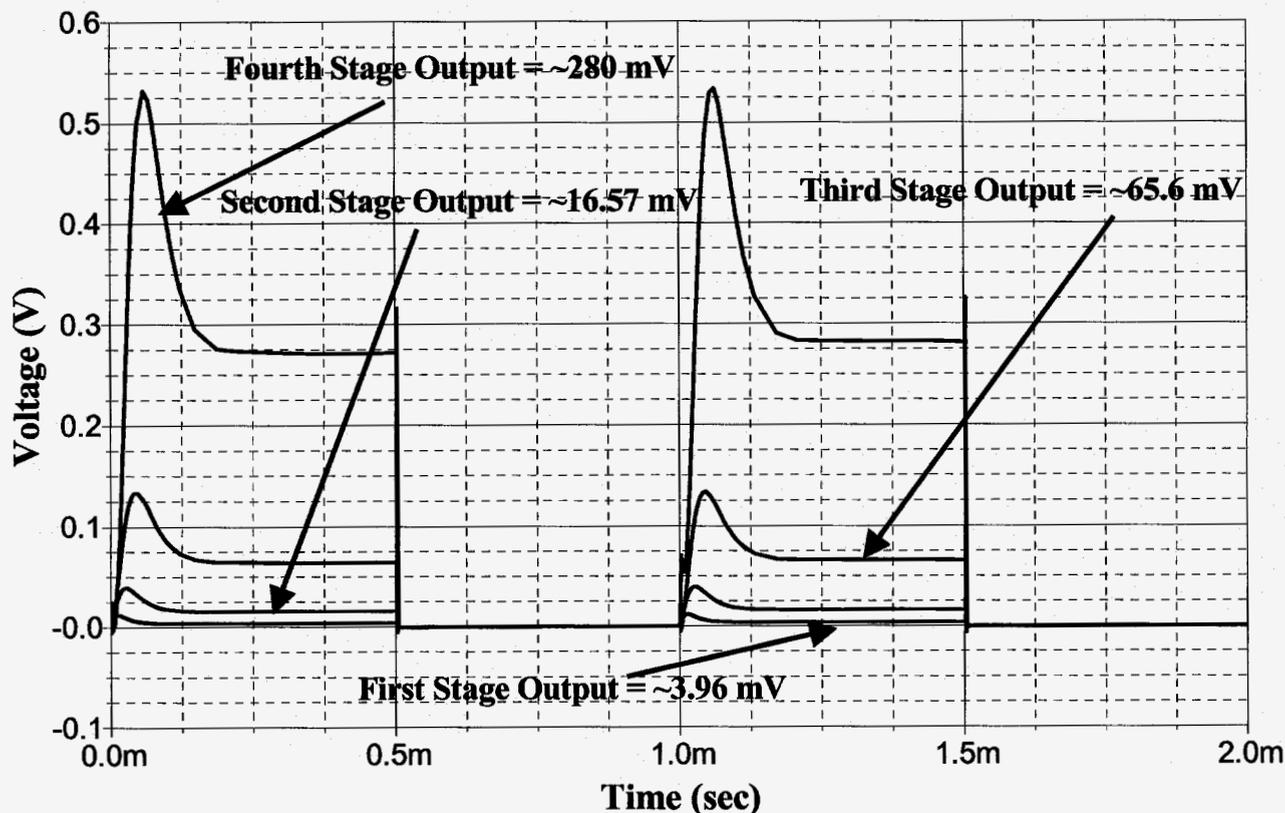


Fig. 9. Simulated differential output signals of four-stage, auto-zeroed, differential OTFT amplifier for a 1-mV input signal in the presence of 500-mV input-referred dc offsets at each stage.

5.3 Auto-zero clock and switches

Auto-zero (phase 1) and signal (phase 2) control is provided by two nonoverlapping digital clock signals operating between -35 and $+15$ V. A clock level above the positive supply voltage of $+10$ V ensures the p-type pentacene OTFT switches are off with minimal leakage. Clock rise and fall times of $0.5 \mu\text{s}$ are used with a clock frequency of 1 kHz. This is consistent with ring-oscillator performance¹² reported for the pentacene devices considered here and for other reported OTFT circuits²³.

The auto-zero OTFT switch devices are considerably smaller at $W = 5 \mu\text{m}$ and $L = 2 \mu\text{m}$ compared to devices used in the differential amplifier. As typical for MOSFET circuits, gate areas for these devices are minimized to minimize charge injection resulting from clock signals appearing at their gates. Since OTFT's have been reported with channel lengths¹⁶ as small as $0.75 \mu\text{m}$, it is believed the switch devices can be practically fabricated.

6. CONCLUSIONS

In this paper, we presented a pentacene OTFT differential amplifier building block designed for relatively low gain, 4 V/V, in exchange for well defined common-mode output voltage levels and minimal gain variations over OTFT processing. The voltage gain is controlled primarily by the ratio of differential pair and active load device

transconductances. Amplifier simulations were based on an AIM SPICE²⁰ device model that yielded simulated curves that closely matched those reported¹².

Since OTFT input-referred circuit offsets can approach 500 mV due to device mismatches, output auto-zeroing was utilized using OTFT switches. A 1-mV input signal level was considered for organic strain gauge and other sensor applications that require precision dc amplification. Simulations of both a single-stage and cascaded four-stage auto-zeroed amplifier show amplification of a 1-mV input signal with removal of 500-mV input-referred dc offsets. Output stage voltages correspond to nominal voltage gains of 4 V/V, with a final output signal of 260 mV corresponding to a composite voltage gain of 260 V/V. 1-kHz non-overlapping, auto-zero digital clock signals were used having rise and fall times of 0.5 μ s and an overlap time of 1 μ s. This frequency and rise and fall times are consistent with those available from pentacene OTFT digital ring oscillators.

While in principal ^{de} output offset cancellation gives complete offset voltage cancellation in fully differential circuits, charge injection resulting from mismatches in OTFT switches will result in residual dc offset errors. Additionally, differential amplifier voltage gains will vary with temperature, although considerable temperature compensation is expected since the gain is controlled by the ratio of device transconductances. System-level digital calibration should be considered where reference signals are applied to the four-stage, auto-zeroed OTFT differential amplifier. These can be used to measure the residual circuit dc offset and voltage gain. Both dc offset and gain errors can then be corrected digitally at the system level. Additional research could also include utilizing amorphous silicon devices in multi-stage, auto-zeroed, differential amplifier circuits.

7. ACKNOWLEDGMENTS

The authors would like to thank the Jet Propulsion Laboratory, managed by the California Institute of Technology, for partial support of this work. They would also like to thank Trond Ytterdal, one of the creators of AIM SPICE, for providing a special version of AIM-SPICE that would accommodate the simulation of four stages of differential, auto-zeroed amplifiers.

8. REFERENCES

1. L. Torsi, A. Tafuri, N. Cioffi, M. C. Gallazzi, A. Sasella, L. Sabbatini, and P. G. Zambonin, "Regioregular polythiophene field-effect transistors employed as chemical sensors", *Sensors and Actuators B*, 2003.
2. C. Bartic, B. Palan, A. Campitelli, and G. Borghs, "Monitoring pH with organic-based field-effect transistors", *Sensors and Actuators B*, **83**, pp. 115-122, 2002.
3. L. Torsi, "Novel applications of organic based thin film transistors", *Microelectronics Reliability*, **40**, pp. 779-782, 2002.
4. L. Torsi, N. Cioffi, C. Di Franco, L. Sabbatini, P. G. Zambonin, and T. Bleve-Zacheo, "Organic thin film transistors: from active materials to novel applications", *Solid-State Electronics*, **45**, pp. 1479-1485, 2001.
5. B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, and Z. Bao, "Electronic sensing of vapors with organic transistors", *Applied Physics Letters* **78**, no. 15, pp. 2229-2231, April 2001.
6. L. Torsi, A. Dodabalapur, N. Cioffi, L. Sabbatini, and P. G. Zambonin, "NTCDA organic thin-film transistors as humidity sensor: weaknesses and strengths", *Sensors and Actuators B*, **77**, pp. 7-11, 2001.
7. Y. Sakai, Y. Sadaoka, and M. Matsuguchi, "Humidity sensors based on polymer thin films", *Sensors and Actuators B*, **35-36**, pp. 85-90, 1996.
8. Z. -T. Zhu, J. T. Mason, R. Dieckmann, and G. Malliaras, "Humidity sensors based on pentacene thin-film transistors", *Applied Physics Letters*, **81**, no. 24, pp. 4643-4645, December 2002.
9. J. Thaysen, A. D. Yalcinkaya, P. Vettiger, and A. Menon, "Polymer-based stress sensor with integrated readout", *Journal of Applied Physics*, **35**, pp. 2698-2703, October 2002.
10. E. Brandon, W. West, L. Zhou, T. Jackson, G. Theriot, R. A. B. Devine, D. Binkley, N. Verma, and R. Crawford, "Flexible electronics for space applications", *Proc. Materials Research Society*, April 2004.
11. H. Klauk, D. J. Gundlach, and T. N. Jackson, "Fast organic thin-film transistor circuits", *IEEE Electron Device Letters*, **20**, number 6, pp. 289-291, June 1999.

12. M. G. Kane, J. Campi, M. S. Hammond, F. P. Cuomo, B. Greening, C. D. Sheraw, J. A. Nichols, D. J. Gundlach, J. R. Huang, C. C. Kuo, L. Jia, H. Klauk, and T. N. Jackson, "Analog and digital circuits using organic thin-film transistors on polyester substrates", *IEEE Electron Device Letters*, **21**, no. 11, November 2000.
13. H. Klauk, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, "Pentacene organic thin-film for circuit and display applications," *IEEE Trans. Electron Devices*, **46**, pp.1258-1263, 1999.
14. A. R. Brown, C. P. Jarrett, D. M. de Leeuw, and M. Matters, "Field-effect transistors made from solution-processed organic semiconductors", *Synthetic Metals*, **88**, pp. 37-55, January 1997.
15. T. N. Jackson, Y.- Y. Lin, D. J. Gundlach, and H. Klauk, "Organic thin-film transistors for organic light-emitting flat-panel display backplanes", *IEEE Journal of Selected Topics in Quantum Electronics*, **4**, no. 1, January/February 1998.
16. W. Fix, A. Ullmann, J. Ficker, and W. Clemens, "Fast polymer integrated circuits", *Applied Physics Letters*, **81**, no. 9, August 2002.
17. M.J. Pelgrom, C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors", *Journal of Solid-State Circuits*, **24**, no. 5, pp.1433-1440, October 1989.
18. Private conversations with T. N. Jackson, Penn. State University, June 17 and September 9, 2003.
19. P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson, "Modeling of organic thin-film transistors of different designs", *Journal of Applied Physic*, **88**, no. 11, December 2000.
20. AIM SPICE, available at website: <http://www.aimspice.com>.
21. C. C. Enz, and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling and chopper stabilization", *Proceedings of IEEE*, **84**, no. 11, November 1996.
22. B. Razavi, "Design of analog CMOS integrated circuits", *Mc-Graw Hill*, New York, 2001.
23. H. Klauk, D. J. Gundlach, J. A. Nichols, C. D. Sheraw, M. Bonse, and T. N. Jackson, "Pentacene organic thin film transistors and IC's", *Solid State Electronics*, **43**, no. 3, pp. 63-77, March 2000.