

New Generation Power System for Space Applications

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Abstract—

The Deep Space Avionics (DSA) Project is developing a new generation of power system building blocks. Using application specific integrated circuits (ASICs) and power switching modules a scalable power system can be constructed for use on multiple deep space missions including future missions to Mars, comets, Jupiter and its moons. The key developments of the DSA power system effort are five power ASICs and a module for power switching. These components enable a modular and scalable design approach, which can result in a wide variety of power system architectures to meet diverse mission requirements and environments. Each component is radiation hardened to one megarad total dose. The power switching module can be used for power distribution to regular spacecraft loads, to propulsion valves and actuation of pyrotechnic devices. The number of switching elements per load, pyrotechnic firings and valve drivers can be scaled depending on mission needs. Telemetry data is available from the switch module via an I²C data bus. The DSA power system components enable power management and distribution for a variety of power buses and power system architectures employing different types of energy storage and power sources. This paper will describe each power ASIC's key performance characteristics as well as recent prototype test results. The power switching module test results will be discussed and will demonstrate its versatility as a multipurpose switch. Finally, the combination of these components will illustrate some of the possible power system architectures achievable from small single string systems to large fully redundant systems.

I. Introduction

The Deep Space Avionics (DSA) Project is a Jet Propulsion Laboratory project developing a new generation of power system building blocks for use on future deep space missions. The effort includes the development of electronic components and modules, which can be used as building blocks in the design of generic spacecraft avionics systems. All avionics components and modules are designed for use in centralized or distributed spacecraft architectures. Specifically the power system components are being developed for a low voltage (30V) power management and distribution system. The power system components may be included on missions such as the recently proposed mission to Jupiter and its three planet sized icy moons, Callisto, Ganymede and Europa (Jupiter Icy Moons Orbiter – JIMO). Deep space missions beyond Mars orbit demand reliable long life circuitry (usually greater than 10 years). Missions to Jupiter and its moons demand high radiation tolerant components. These two combined challenges force the research to improve the lifetime and radiation tolerance of electronic components and parts used in the design and fabrication of power system modules. The current state of the art low voltage power system components are limited to environments less than 300 Krad total ionizing dose. To create a power system

capable of performing in an extreme radiation environment the Deep Space Avionics project has taken the approach of developing a set of Application Specific Integrated Circuits (ASICs), which are radiation tolerant to >1 Mrad. The current DSA effort is leveraging off previously sponsored work by the Jet Propulsion Laboratory (JPL) and is currently sponsored by the JIMO project. JPL had teamed with Boeing (ASIC Design) and Honeywell (ASIC foundry) under the X2000 Integrated First Delivery Project. During this past effort the team developed an analog ASIC cell library to be used for future ASIC designs. By combining the analog cell library developed by Boeing and the digital circuit cells developed by Honeywell, mixed signal ASICs for power applications, which are 1 Mrad hard, can be designed and fabricated. Using mixed signal ASICs for power system design can reduce the number of components necessary for a system. By using components that are inherently radiation hard, less shielding is required and higher reliability is achieved, resulting in overall mass and volume reduction. This result is beneficial to power system architects who are constrained by spacecraft volume and mass requirements.

Power system functions have been broken up into five ASIC designs and one switching module.

The following four ASICs have been developed:

1. Switch Control ASIC – High Side (SCAH)
2. Switch Control ASIC – Low Side (SCAL)
3. Analog Interface ASIC (AIA)
4. Command Interface ASIC (CIA)

The fifth ASIC is currently in development

5. Pulse Width Modulator ASIC (PWMA)

One switching module has been developed:

1. Power Actuation and Switching Module (PASM)

All ASICs are inherently 1 Mrad hard as a result of the Honeywell fabrication process. The two switch control ASICs (SCAH – SCAL) are used in the PASM design. The PASM is fabricated using High Density Interconnect (HDI) technology developed by General Electric. This packaging technology allows more power switches per circuit card than chip on board, hybrid or discrete component designs. The PASM can be used along with the AIA and the CIA to create a general purpose switch board. The PWMA can be used in the design of dc/dc power converter units. By scaling the circuitry surrounding the PWMA, various output voltages and power levels may be achieved.

II. Power System Building Blocks

A. Switch Control ASICs (SCAH and SCAL)

The SCA-High and SCA-Low are designed as a chipset to control one solid-state switch (such as a MOSFET) for general switching purposes. Figure 1 illustrates both ASICs connected to a power switch. The chipset is fabricated on the Honeywell foundry HX2000, 0.8µm, Silicon on Insulator (SOI) process and the first ASICs were completed in June 2003. The chipset has the capability to be powered by redundant 5V power supplies. Power-on-Reset (POR) circuitry was designed to keep the circuit in a known state during power on and power cycling. The ASICs have the capability of providing analog telemetry for switch current and switch voltage. Logic command inputs are compatible with 3.3V & 5.0V standard CMOS logic levels. Currently the chipset is designed to interface with a 100V MOSFET appropriate for use in

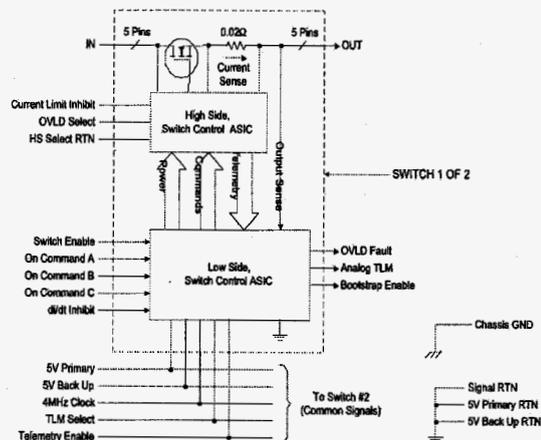


Figure 1 SCAs in Power Switch Diagram

most low voltage applications. However, with adequate isolation between the interfaces of the two chips it can be used in higher switch voltage applications.

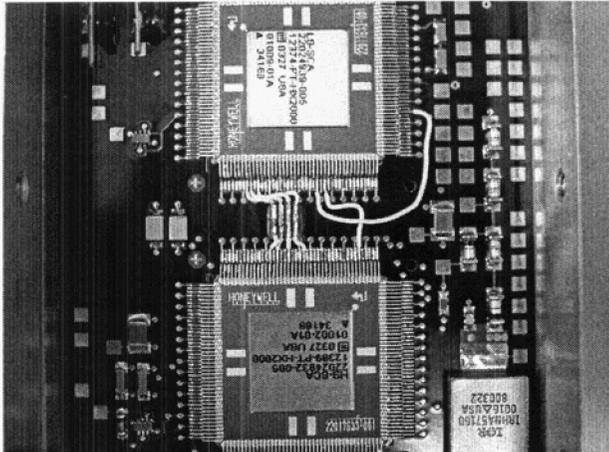


Figure 2 Test Card for Packaged SCAs

One wafer lot of SCAs was fabricated and the first wafer was packaged and shipped to JPL as proof of design components. Low side and high side SCAs were individually packaged into quad flat packs and assembled on to a test card. The SCA chip set was designed for the close proximity packaging afforded by the HDI process so, when tested on a card in separate quad flat packs the performance was expected to degrade. The test results showed that the package lead length and capacitance affected the SCA signals adding noise and decreasing output voltages. These parasitic effects were added to the circuit simulation model and resulted in waveforms similar to those seen on the test card. This gave us enough confidence in the ASICs to proceed with the fabrication of the PASM.

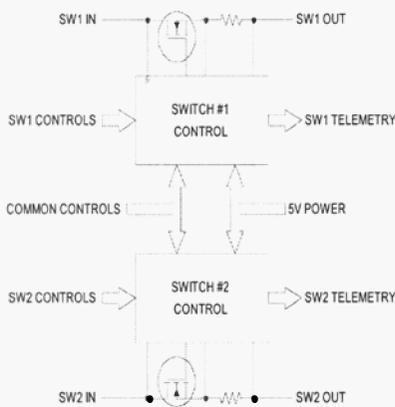


Figure 3 PASM Block Diagram

being used to fabricate the PASM. Some of the key features of the PASM are over-current trip, current limiting, soft start (closed loop di/dt control), switch current and voltage telemetry and back EMF suppression for inductive loads. The over-current trip and current limit capability of the PASM have high and low settings. Current will be limited to a maximum of 6.5A on the high setting and 2.5A on the low setting. The individual switches are command reset able once tripped. In addition switch status (on/off) and overload fault telemetry output is available. Nominal limit for di/dt control is 7.5 A/ms. The PASM is capable of driving regular loads (heaters, traveling wave tube amplifiers, spacecraft computers), pyro devices and inductive loads (thruster valves, motors). The SCA control circuitry allows each switch to be configured appropriately to match the needs of the load. For example, to configure a PASM switch to drive a pyro device one would disable the di/dt, set the current limit to 5.0A and enable the over current trip so that when switched on the pyro initiator is given a 6.5A pulse for a maximum of 31ms before the switch trips off.

B. Power Actuation and Switching Module (PASM)

The PASM is a solid state general purpose switching module. Each PASM has two independent MOSFET power switches that can be used in various configurations. Figure 3 exhibits the PASM block diagram. These switches can be used in a series or parallel configuration and as high side or low side connection to the load, thus, providing greater flexibility to the system architect when designing the power system. The PASM package design is based on a new technology that enables higher density packaging of electronic components when compared to chip on board or hybrid packaging techniques. JPL's industry partner Lockheed Martin – Commercial Space Systems (LM-CSS in Newtown, PA) has designed the PASM. The Power High Density Interconnect (Power HDI) packaging technique developed by General Electric is

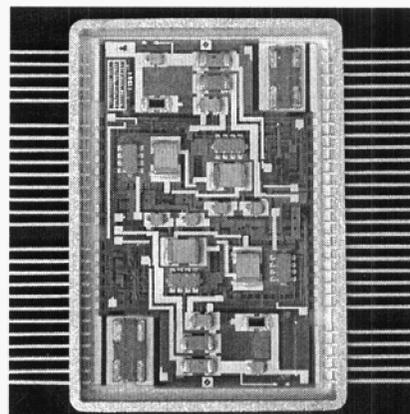


Figure 4 HDI PASM

Prototype HDI PASM s were fabricated and tested the first half of 2004. The PASM package is 1.0 by 1.6 inches, as shown in figure 4, and contains two independent power switches. The tight package significantly reduced the noise sensitivity found during packaged SCA testing. The switches were tested with resistive loads at various bus voltage levels and various load values. Switched voltage and current waveforms were clean and followed the di/dt ramp as expected. Testing was performed with the switch configured as a high side and low side switch. When driven into a load greater than the current limit, the output current was held at the current limit value until the switch tripped off. Pyro initiator switch testing with di/dt disabled performed perfectly. Switching into inductive or capacitive loads with di/dt control enabled performed as expected for the representative values that have been tested to date. Testing is ongoing at LM-CSS. Testing of the switch commands and telemetry performed as expected. The PASM current limit levels and shut down response times were as expected. Combining the PASM with the AIA and CIA on a single card is planned for early 2005.

C. Analog Interface ASIC (AIA)

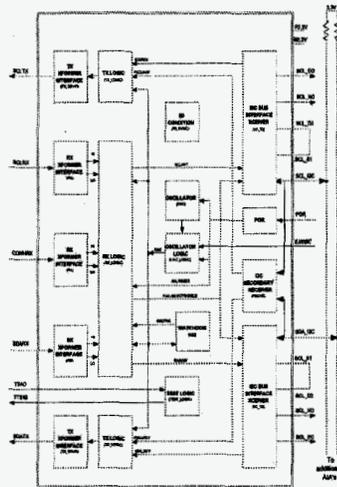


Figure 5 AIA Block Diagram

The AIA provides power return isolation between the data buses and the power system electronics. The AIA receives and transmits commands to the CIA via two I²C transceivers. Figure 5 exhibits the block diagram of the AIA. Transformers are used to isolate the signals between the AIA and the CIA. An internal 6.29Mhz clock is designed on chip with the capability of interfacing with an optional external clock. An on-chip oscillator watchdog forces the AIA into a fail-silent mode in the event of an oscillator failure. This chip is powered by redundant 3.3V power sources. A power-on-reset signal must be provided by an external source such as a power converter. Like the SCA, it is fabricated on the Honeywell HX2000 process, which makes the chip 1Mrad hard. The first ASICs were produced June 2003. Prototype ASICs were packaged and have been tested individually and with the Command Interface ASIC. The AIA passed all functional verification tests.

D. Command Interface ASIC (CIA)

The CIA is a micro-controller that is based on a M8051 core processor with multi-frequency operation. A block diagram of the CIA is shown in figure 6. The CIA has been fabricated on the Honeywell HX3000 0.3μm, SOI process line. The CIA has two modes of operation, one at 16.5 MHz and another at 8.25 MHz. In addition it has a sleep mode for low power consumption. It can interface with the spacecraft computer via an I²C standard data bus. The design provides two I²C ports, which allow communication on primary and redundant data busses. There is 8KB and 12KB of program and data memory respectively available on chip. The CIA also has the capability to boot up from an external ROM and store data to a larger external memory device. The external ROM feature allows user specific programming of the micro-controller. The chip can be powered by two 5.0V sources for the analog circuitry and

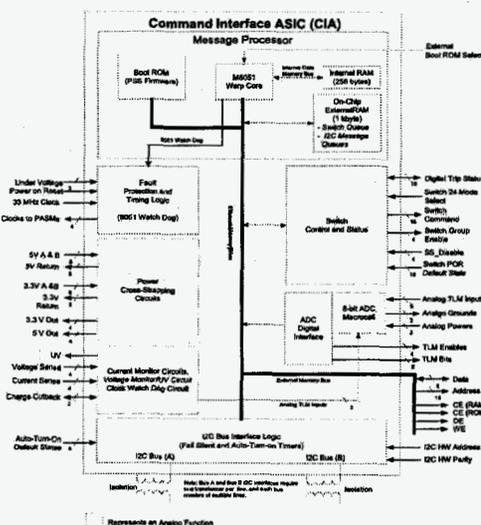


Figure 6 CIA Block Diagram

two 3.3V sources for the digital circuitry. Both voltages are then cross-strapped internally for redundancy. At least one of each voltage is needed for proper CIA functionality. Internal power-on-reset (POR) circuits are also designed to hold the circuit in a known state during initial power on and power cycling. The CIA is designed to work with the other building blocks of the power system, and as such contains a multiplexed 8-bit analog to digital converter, which processes the analog telemetry from the PASM. The CIA has the ability to measure bus voltage and current directly across an external resistor network and report this telemetry on the I²C bus. An internal watchdog timer in the design forces a fail silent state on the I²C bus in the event of a failure.

Prototype versions of the AIA and CIA have been tested at JPL. Functionality of each block has been targeted by a series of tests. All blocks have successfully passed performance testing at ambient temperature. A simulated spacecraft computer was used to send I²C commands and receive telemetry back from the test card containing two AIAs and one CIA. Each time the automated test is run approximately 2.3 million I²C commands are sent and a telemetry status response is received for each command. Tests were run using primary and redundant I²C busses; all commands resulted in the expected telemetry and power switch status indication. The fail silent and power cross-strap functions of both ASICs performed as expected. Overall, this chip set has met or exceeded our expectations. A photo of the test card is shown in figure 7.



Figure 7 AIA-CIA Test Card

E. Pulse Width Modulator ASIC (PWMA)

The PWMA is currently in design. The goal of this effort is to design a single ASIC that can be used as the PWM for a family of radiation hardened power converters. Taking advantage of the analog cell library used in the design of the other ASICs along with the same design team and modeling tools the PWMA design has a high likelihood for first pass success. The ASIC will contain necessary functions for power conversion such as pulse width modulation, synchronous rectification, voltage references and FET drivers. As a DC/DC converter building block, the PWMA will accommodate isolated and non-isolated converter designs using spacecraft input bus voltages as large as 130V. The design of the ASIC is currently being performed by JPL and fabrication is planned for early 2005.

III. Sample Power System

Figure 8 exhibits a block diagram of a fault tolerant power system configured using Deep Space Avionics ASICs and PASMAs assembled into slices. A number of Power Switch Slices (PSS) are used for switching regular spacecraft loads, pyros and propulsion valves. Three power control slices are controlling the power source to its peak power point and also regulating the battery charge current.

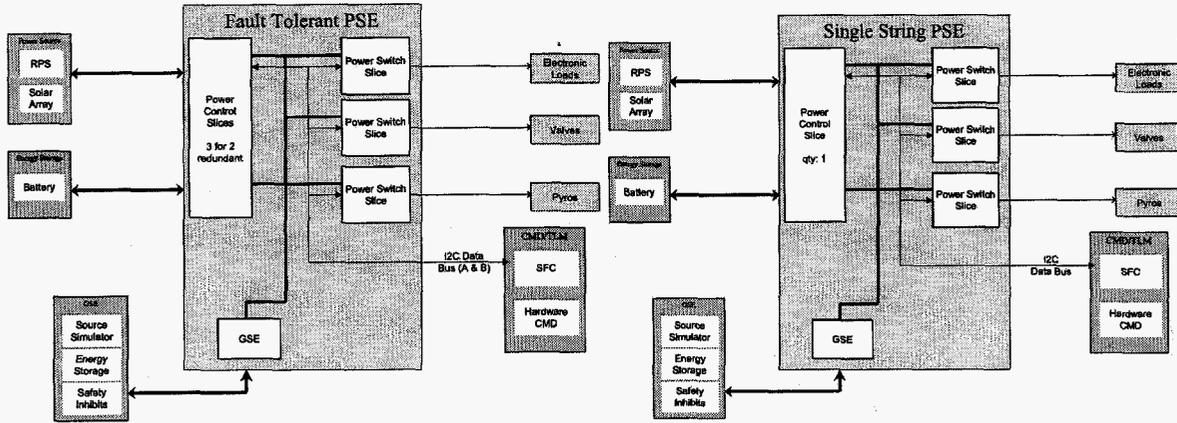


Figure 8 Fault Tolerant Sample Power System

Figure 9 Single String Sample Power System

Figure 9 exhibits a block diagram of a single string power system using Deep Space Avionics ASICs and PASM. Eliminating redundancy and power return isolation is achieved by simply removing the appropriate building blocks. Figure 10 and figure 11 illustrate one possible Power Switch Slice configuration for the fault tolerant power system and the single string power system, respectively. The single string system does not require the data bus protection of the AIAs and the isolation transformers so the spacecraft computer may communicate directly with the CIA. The fault tolerant power switch slice uses multiple power and ground trees and multiple PASM across several cards would be wired to spacecraft loads to provide redundant power switching. These simple building blocks can be integrated into small power systems and at the same time are flexible enough to handle large, complex power systems.

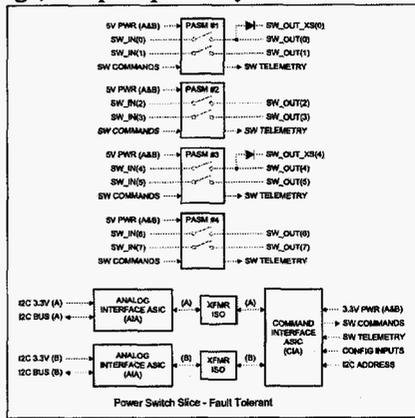


Figure 10 Fault Tolerant PSS

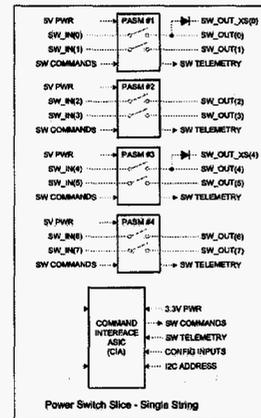


Figure 11 Single String PSS

IV. Summary

The Deep Space Avionics project is developing electronic components that are high reliability and radiation hard for future spacecraft power systems. These components can be used to architect a centralized or distributed power system for future long life deep space missions such as missions to Jupiter. Using these components a power system can be designed to have a regulated or non-regulated power bus. In addition, a power system designer is not limited in the types of power sources and energy storage devices that can be selected. These components have the flexibility to meet the needs of many power system architectures. Commanding of the power system is achieved through an I²C data bus. Power distribution to a variety of loads such as heaters, pyros and propulsion valves can be achieved by using the same generic building blocks being developed. The basis of the building blocks being developed is a set of five mixed-signal ASICs (AIA, CIA, SCAH, SCAL and PWMA) and one power switching module (PASM). To date four ASICs and a switching module have been designed, fabricated and preliminary test results have been gathered.

V. Acknowledgments

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