National Aeronautics and Space Administration
Jet Propulsion Laboratory
California Institute of Technology

Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

***RadioNet Engineering Forum Workshop*:**

Next Generation Correlators for Radio Astronomy and Geodesy

Robert Navarro

June 27, 2006

Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

DSN Large Array Background

Array Project Overview

- **DSN Large Array will replace/augment 34 and 70 meter antenna assets.**
- **Mainly used for to support NASA's deep space telemetry, radio science and navigation requirements.**
- **The Array Project will deploy**
  - **Three Complexes (Western US, Australia, European Longitude), each with:**
    - **400 12m downlink antennas (x40 the data rate of the 70m antenna subnet at X-band)**
  - **DSN Central facility at JPL**
    - **Remotely conduct all real-time monitor and control for the network**

Signal Processing Requirements

- Number of Antennas in a cluster ~ 400.
  - Design needs to accommodate growth but is not infinitely scalable
- Number of IF inputs per antenna = 2.
  - RCP & LCP or X and Ka
- IF signal bandwidth = 500 MHz 1dB
  - Main driver for sample rate of 1280 Ms/sec.
- Signals of interest can come from anywhere in input passband
- Provide up to 16 simultaneous phased array outputs
- Provide a wideband correlator (500 MHz) which can process a significant number of the antenna signals
  - Required to support the array for phase and antenna position calibration and searching for lost spacecraft

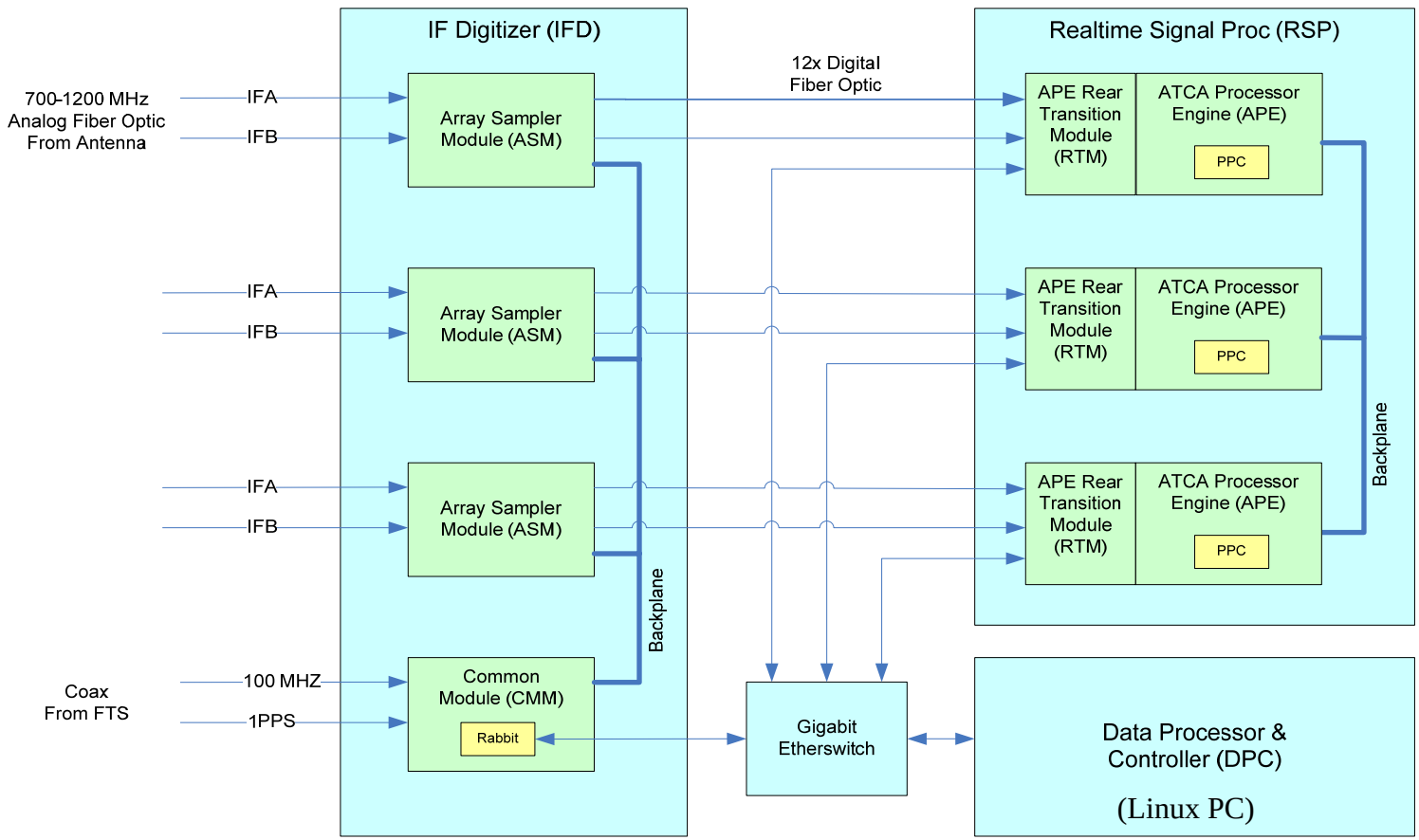
Breadboard Array Signal Processing Objectives

- Provide a means to evaluate the performance of the Breadboard Array's antenna subsystem (the antenna, feed and RF-IF downconversion) for one 12 meter and two 6 meter antennas.
- Design and build prototype hardware
  - High density IF digitizer, current design supports 6 Antennas (12 IF inputs) in one chassis
  - High speed FPGA digital signal processing board for AdvancedTCA chassis
- Demonstrate and evaluate proposed signal processing techniques
  - Implement an architecture similar to an FX correlator but includes synthesis processing at the output to reconstruct a time domain signal for beamforming applications
  - Provides both beamformer and wideband correlation functions
  - Supports Order N and Order N^2 complexity combining algorithms
  - Polyphase FIR filter and a FFT for Analysis filterbank
  - Synthesis filterbank for reconstruction of beamformer output
- Gain experience with various technologies that may be used in the Large Array
  - High speed serial digital signal interconnects (Xilinx RocketIO 3-10Gbit/s)
  - High speed analog to digital converters (1280 Ms/s, 8 bit, Atmel)
  - AdvancedTCA Chassis with high speed serial backplane
  - Field Programmable Gate Arrays for digital signal processing (Xilinx)
  - Linux OS for use in embedded processors (MontaVista)

Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

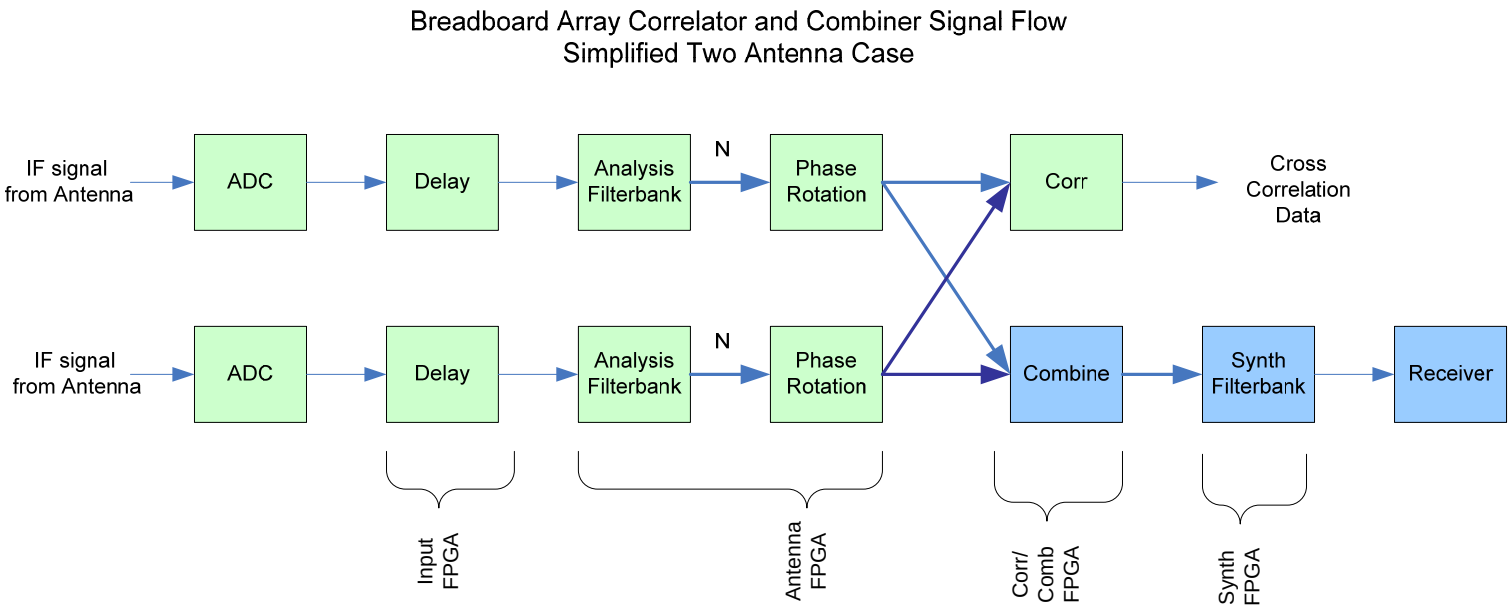
Breadboard Hardware

Breadboard Array Signal Processing



Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

Breadboard Signal Processing Flow

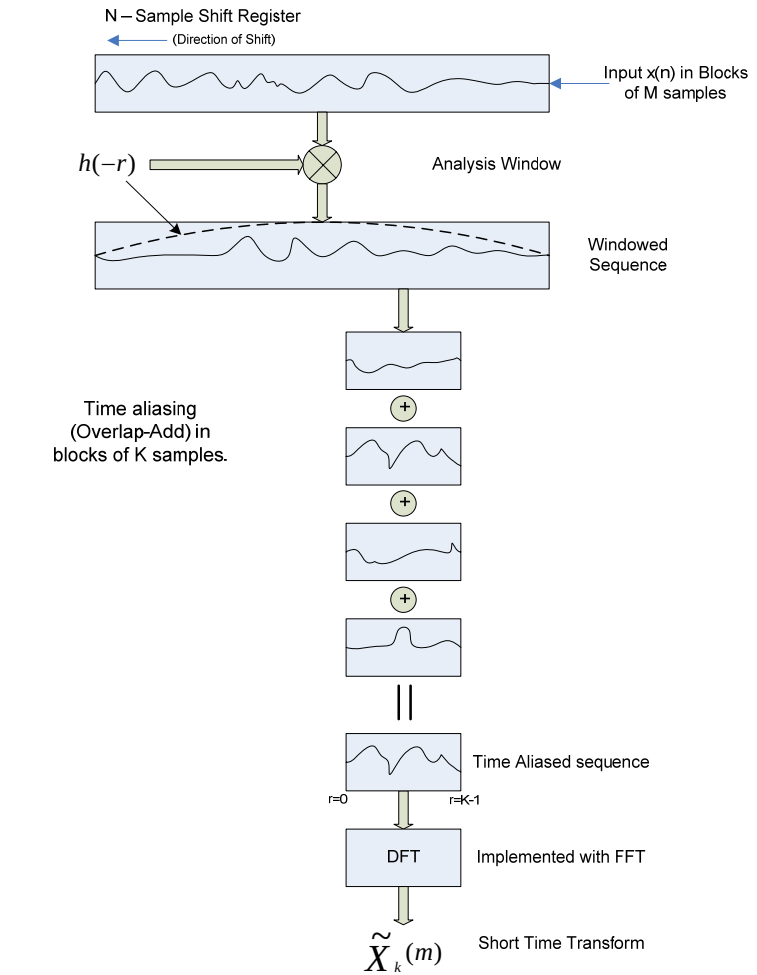


- Functional Blocks in green are implemented.
- Functional Blocks in blue are in development

Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

Detail – Analysis Filterbank

- **Block Diagram of Analysis Filterbank in Antenna FPGA**
- **This structure allows for oversampling of the DFT to obtain overlap in the bandwidth of the frequency channels.**
- **The extra bandwidth in each frequency channel allows for fringe rate (frequency) corrections to be made to each channel.**
- **Also, it allows for the analysis/synthesis filterbank combination to give near perfect reconstruction with a simple square root raised cosine prototype filter.**

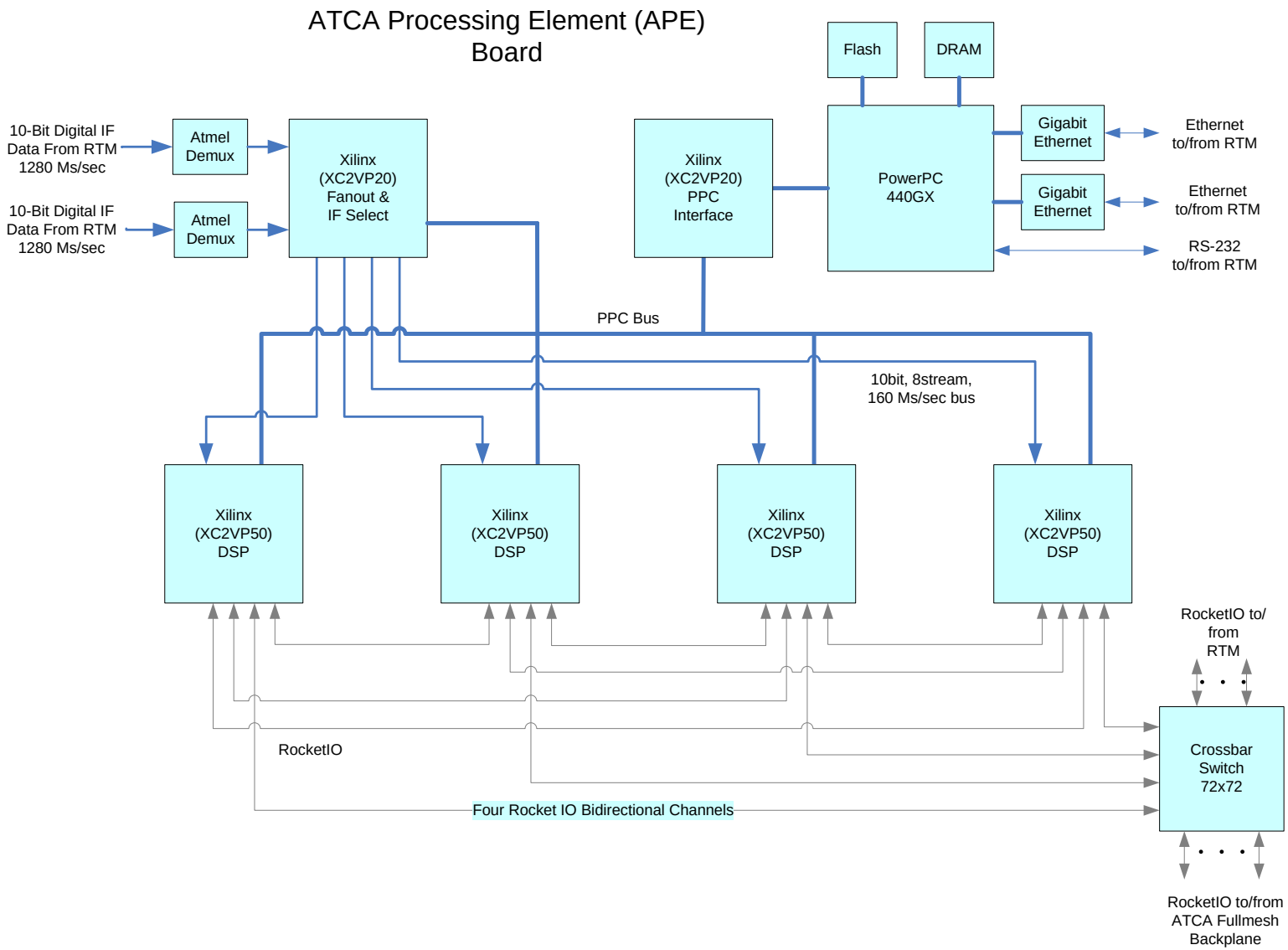


Sequence of Operations for weighted overlap-add spectral analyzer

(From Multirate Digital Signal Processing, Crochiere and Rabiner, page 318)

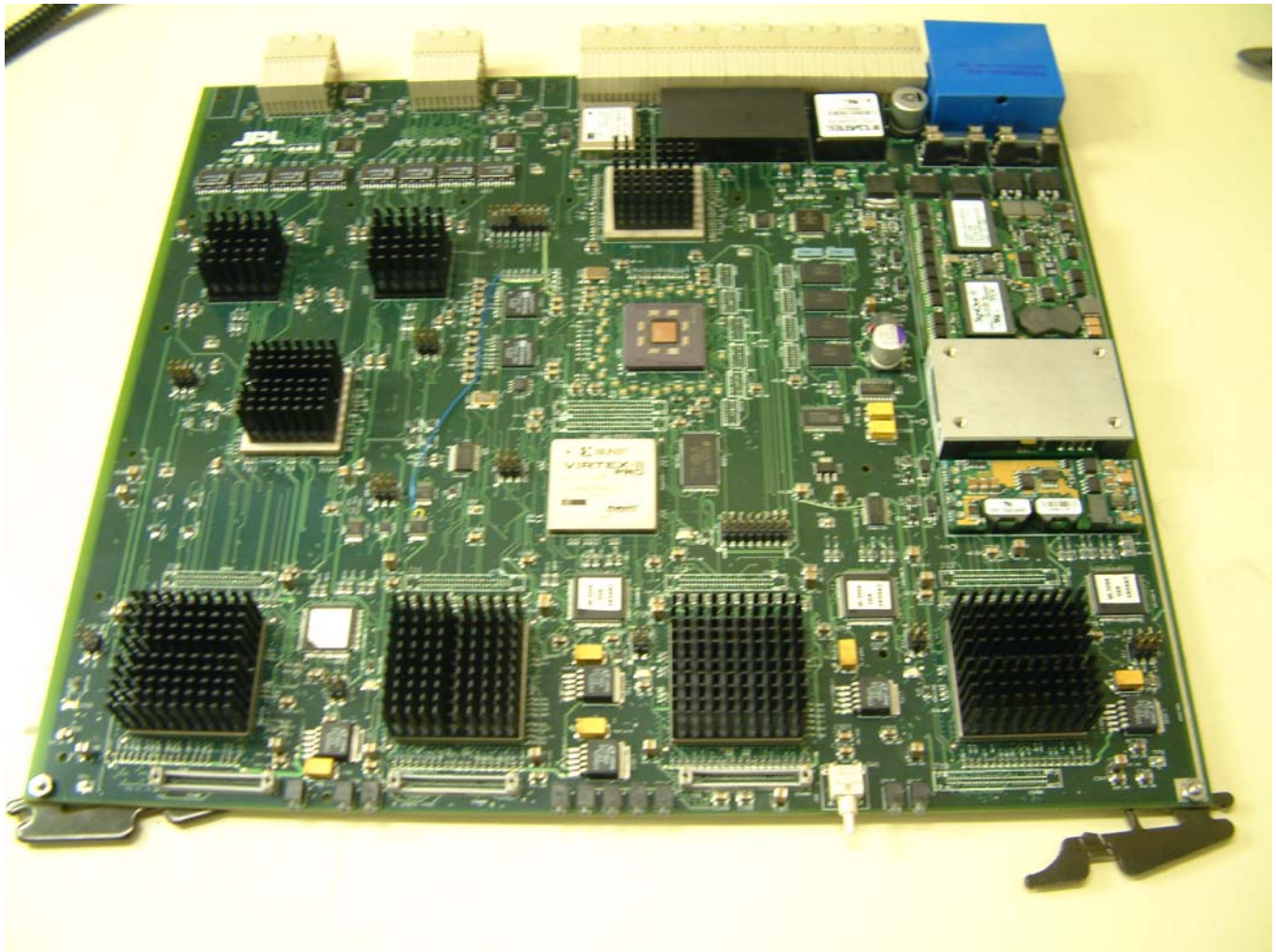
Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

APE Board in Real-time Signal Processor



Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

APE Board Picture



BBA Signal Processing Results Summary

- **Built and Tested Hardware: 3 Array Sampler Modules (ASM) for the IF Digitizer (IFD) and 3 AdvancedTCA Processor Engine (APE) boards for the Real Time Signal Processor (RSP).**
- **Software and Signal Processing Firmware (FPGA code) for the wideband correlator completed and tested.**
- **Successfully demonstrated these technologies for BBA:**
  - **High Speed A/D (1280 Ms/sec, 10 bit digitizer)**
  - **Analog Fiber link from Antenna to IFD, Optical Fiber link from IFD to RSP.**
  - **High Speed Serial links (3.2 Gb/sec) between Filterbanks and Correlator blocks.**
  - **Real-time Linux OS for Embedded PowerPC processors.**
  - **Wideband (640 MHz) Discrete Fourier Transform Analysis Filterbank implemented in FPGA.**

Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

Experimental Results

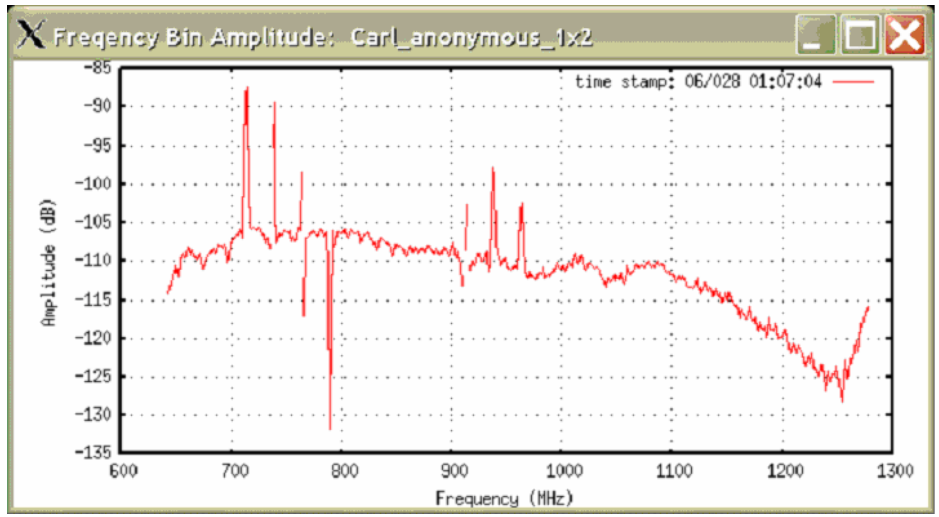
- **Successfully detected interferometric fringes from two 6 meter antennas using Venus as the source in Dec 2005.**
- **Successfully stopped interferometric fringes using Geometric models while viewing Venus, Cygnus A, and Cassiopeia A with the two 6 meter antennas on the mesa in January 2006.**
- **Signal Processing Monitor plots give visibility to confirm correlation and measure delay offsets but not to do detailed analysis of data.**
- **Correlation Data is archived for later processing using AIPS software to determine more accurate antenna position.**

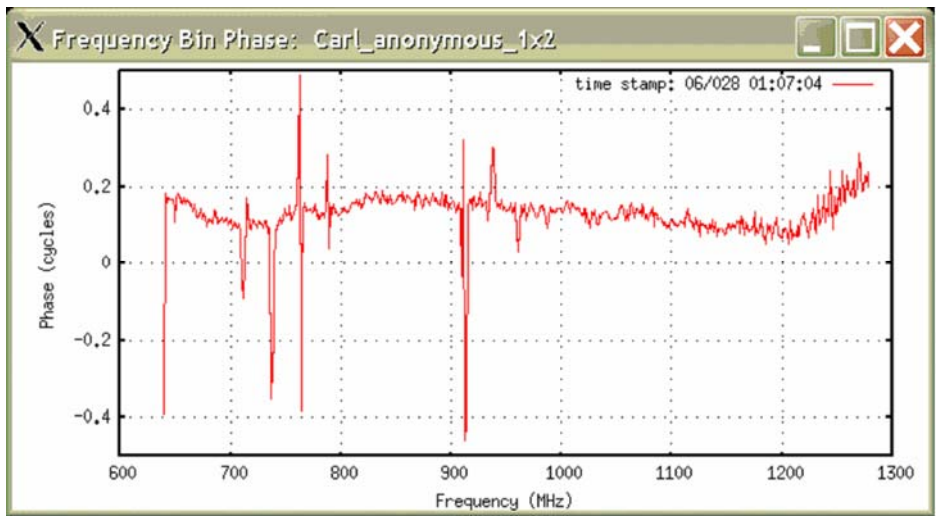
Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

Experiment Results: Phase and Amplitude

Results from two 6 meter antennas looking at Cygnus A:

- Amplitude and Phase shown over 640 MHz complex sampling band.
- Large spikes in Amplitude and Phase from RF interference at X-band
- Geometric models and offsets for path delay applied to bring delay to zero.
- For zero delay, the plot of phase versus frequency should have a slope of zero across the band.



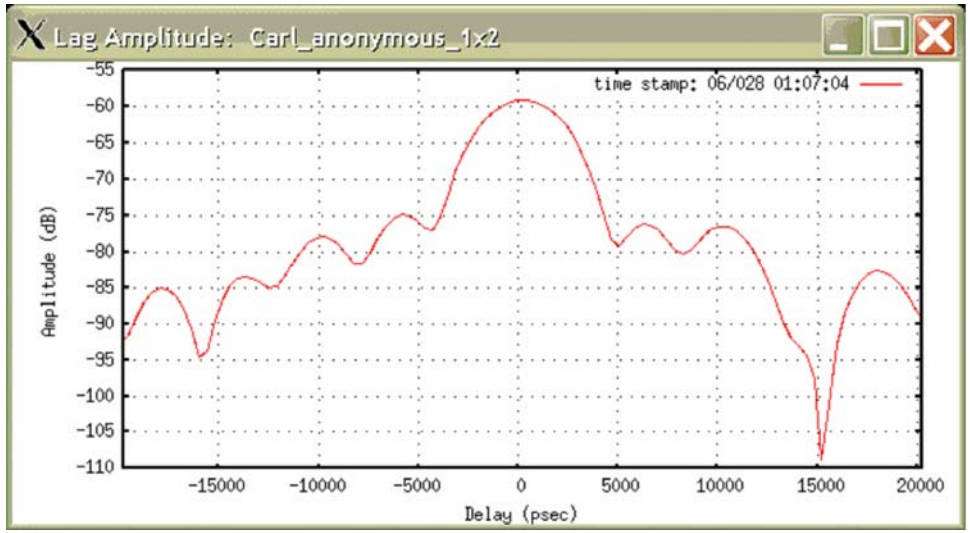


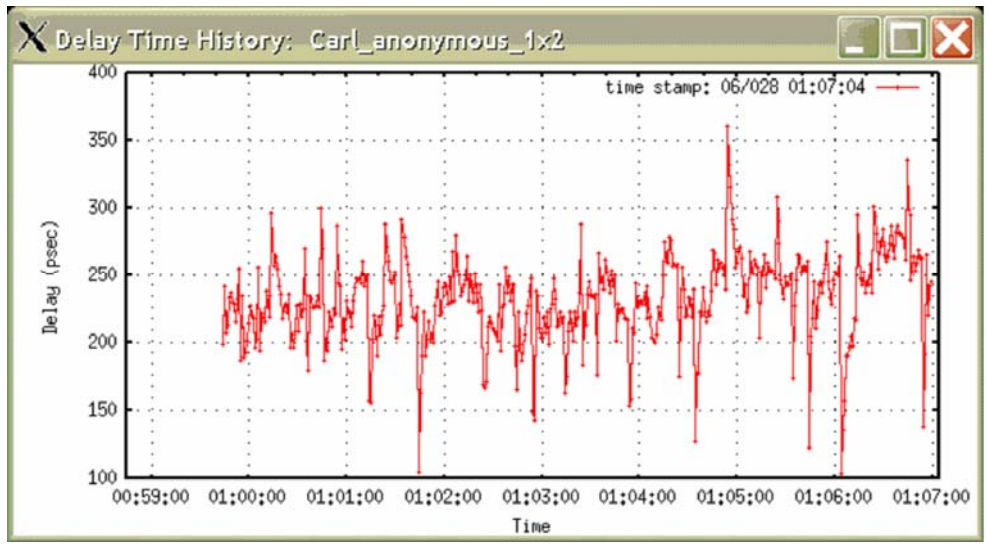
Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

Experiment Results: Lag and Time Delay Plots

Results from two 6 meter antennas looking at Cygnus A:

- Plot of Lag Amplitude made by taking inverse FFT of frequency channel data.
- Main Lobe of lag plot centered at delay of Antenna2 to Antenna1.
- Frequency channels with RF interference excluded in calculating these plots.
- Delay Time History plot tracks peak of Lag Amplitude plot.





Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

Scaling to 400 Antennas

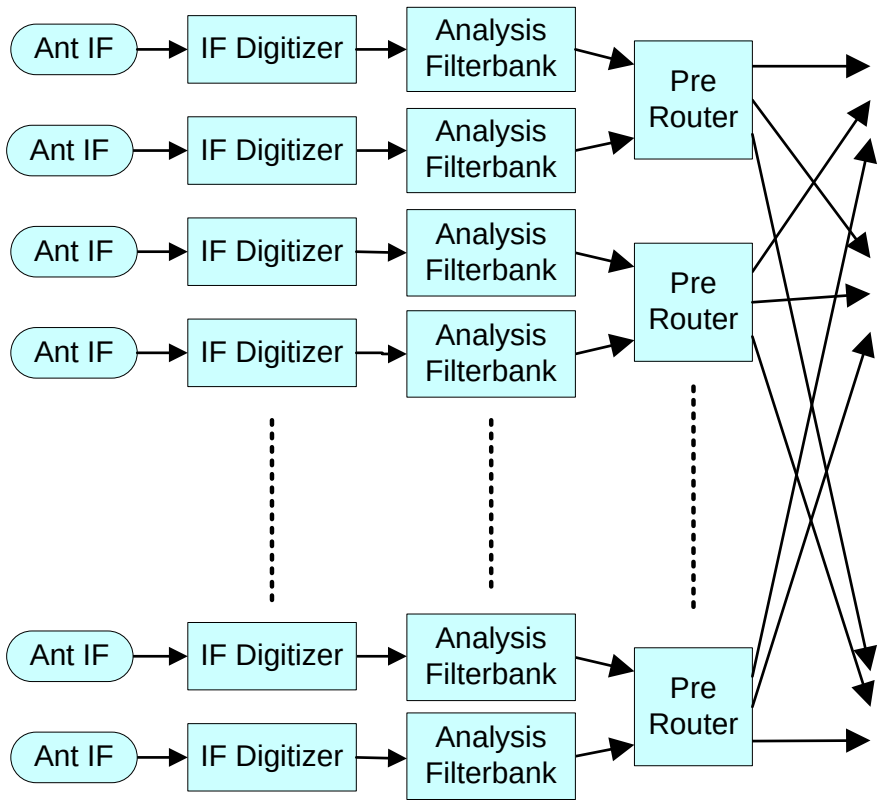
- Revise current ATCA APE board into 3 or 4 ATCA boards optimized to the various functions of the Array Signal Processing using latest FPGA technology available.
  - Input analysis filterbank (Frequency Channelizer) Board
  - Data Routing/Corner Turner Board (may be spread amount Channelizer and Correlate/Combine boards).
  - Correlate/Combine Board
  - Synthesis Board
- Research interconnect strategies for Advanced TCA to Advanced TCA chassis interconnection.
- Architecture must provide features to increase system reliability
  - Redundant power supplies & hard drives to avoid the most common failures
  - Hot swap capability to allow hardware repair without shutting down systems
  - Avoid single points of failure by distributed functions across multiple boards and chassis
  - Automatic diagnostics identify hardware to be swapped
  - Mostly provided by attributes of Advanced TCA shelf technology.

Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

400 Antenna Array Architecture

FX Beamformer & Correlator

- Digitize entire antenna IF bandwidth
- Apply course delay and phase corrections in time domain
- Analysis filterbank uses polyphase FIR filter and a FFT to break the time domain signal up into evenly spaced frequency channels
- Apply fine delay and phase corrections in the frequency domain
- Multiple correction profiles required to support multiple beams per antenna
- Multiple resolutions required to support wideband correlation and spacecraft signals
- Pre-Router receives frequency channel data from multiple antennas and rearranges the data so that each output carries data for all input antennas over a subset of the frequency channels
- Failure of one block does not cause failure of entire signal processing system

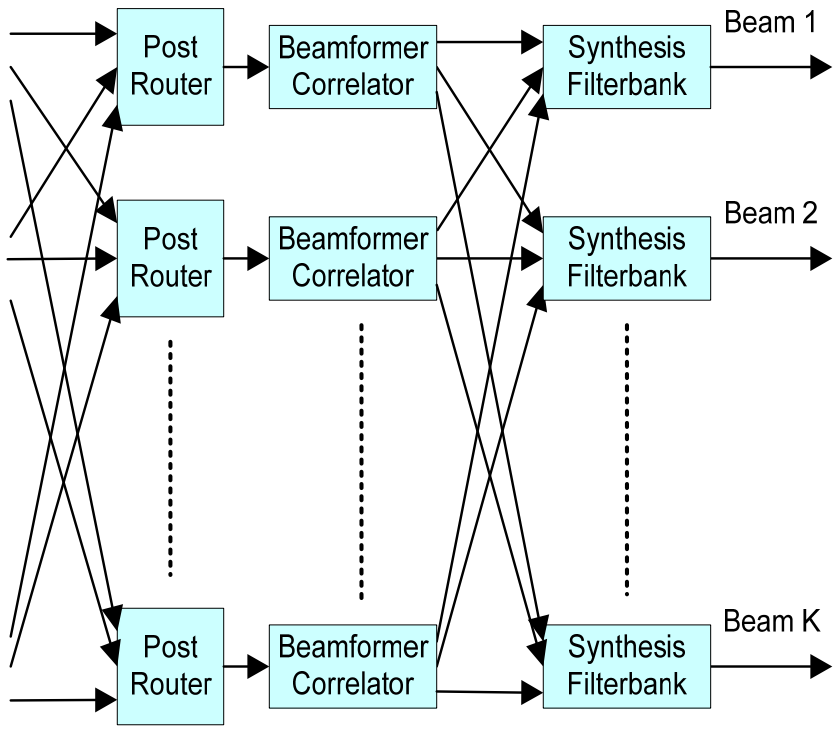


Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

400 Antenna Array Architecture

FX Beamformer & Correlator

- Post-Router receives input from each Pre-Router and completes the corner turning process
- Beamformers receive data from Post-Routers and process data from all antennas for a subset of the frequency channels
- Beamformers provides both a wideband correlation function and narrower band spacecraft processing
- Synthesis filterbanks receive data from multiple beamformers and transforms them into a wider bandwidth time-domain signal
- Multiple Synthesis filterbanks provide multiple phased array outputs
- Output rate of Synthesis filterbanks can be scaled to meet required output bandwidth



Implementation of an Antenna Array Signal Processing Breadboard for the Deep Space Network

400 Antenna Array Architecture

Signal Processing Hardware for 400 Antenna Array

23 Digitizer Racks

- 1 Antenna (2 bands) per Sampler module
- 6 Sampler & 1 Common module per chassis
- 67 Dig chassis per 400 Antenna Cluster
- Each Dig chassis requires 100MHz, 1PPS, & 10Base-T

10 Antenna Signal Proc Racks

- 2 Antenna (2 bands) per Ant board
- 10 Ant & 4 Pre-Rtr boards per chassis
- 20 Ant chassis per 400 Antenna Cluster
- Each Ant chassis requires 100MHz, & 1000Base-T

8 Beam Former Signal Proc Racks

- 1 Beam per Beam Former chassis
- 5 Post-Rtr, 8 Beam Former & 1 Synthesis board per BF chassis
- 16 Beamformer chassis per 400 Antenna Cluster
- Each BF chassis requires 100MHz, & 1000Base-T