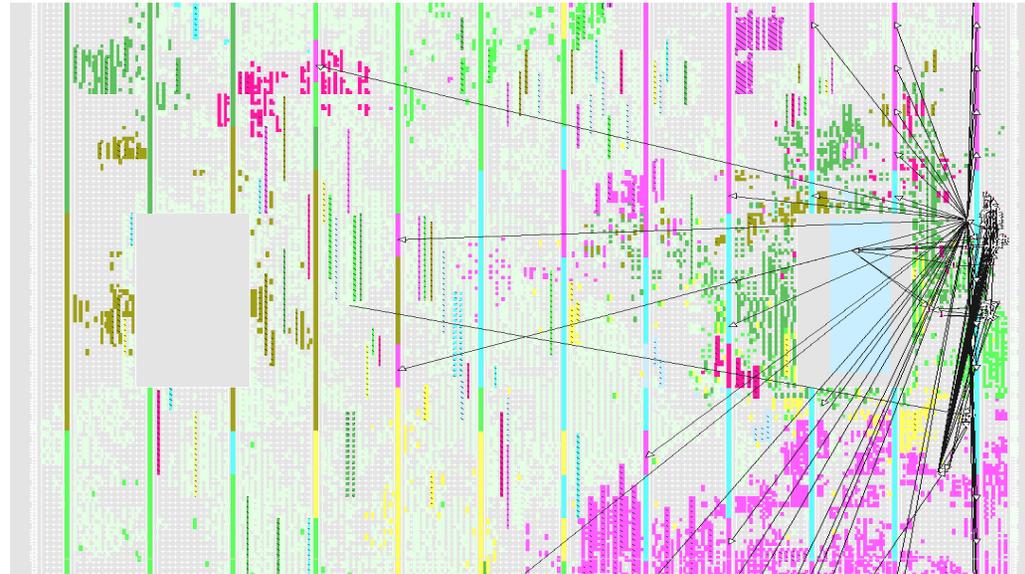




# TRIGA – CFDP Protocol Accelerator



Telecommunications Protocol Processing Subsystem Using  
Reconfigurable  
Interoperable  
Gate  
Arrays



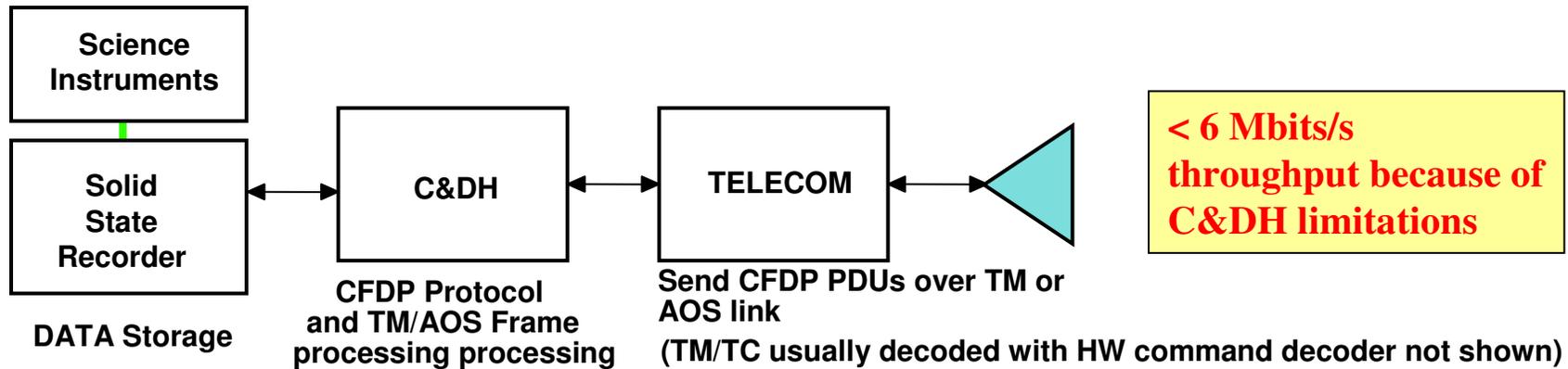
**Jackson Pang, Paula Pingree and J. Leigh Torgerson  
Jet Propulsion Laboratory  
California Institute of Technology**

**Second IEEE International Conference on  
Space Mission Challenges for Information Technology 2006  
Pasadena**

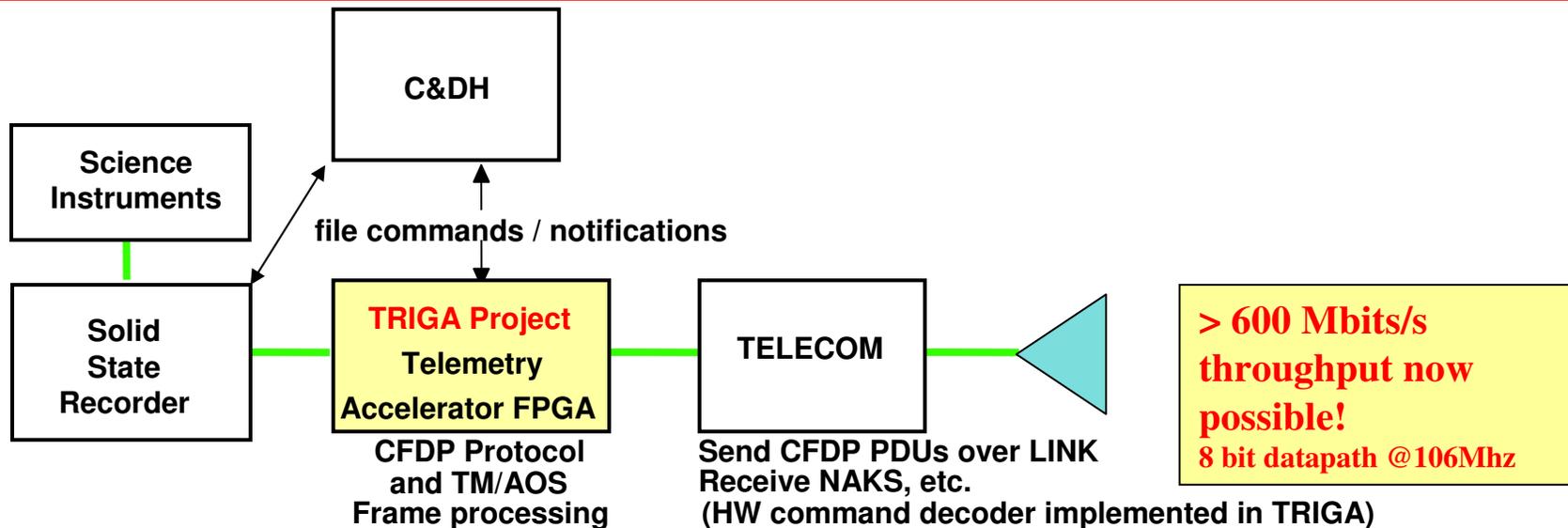
# Spacecraft Telecom Architecture



TRIGA



- **New approach - use FPGA hardware for protocol processing**



# Deep Space Telecommunications



TRIGA

- **Deep Space Telecommunications Requirements**
  - **Automated file transfer across inter-planetary distances**
  - **Limited communication periods**
  - **Reliable transport**
  - **Delay and Disruption Tolerant**
  - **Asymmetric Data Channels**



# CFDP Protocol



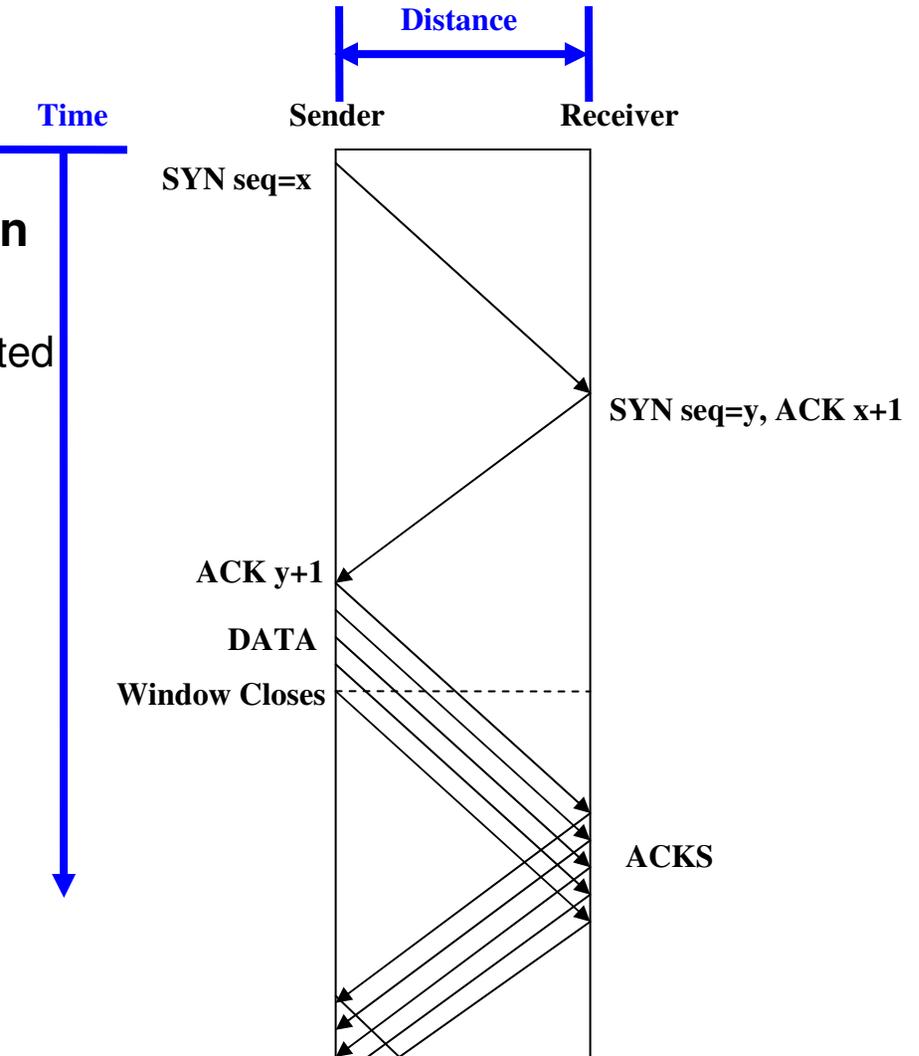
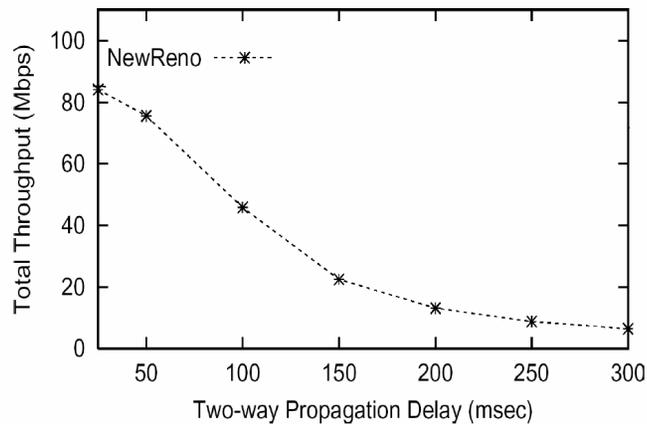
TRIGA

- **An international standard for automatic, duplex reliable file transfer between spacecraft and ground, built on top of familiar CCSDS protocols**
  - **CCSDS - Consultative Committee for Space Data Systems comprised of 30 International space agencies**
- **Able to route data across multiple relay points, some of which may be separated by interplanetary distances**
- **Combines transport layer and file management capabilities**
- **Handles out-of-order Protocol Data Unit delivery**
- **Supports acknowledged and unacknowledged mode**
- **Provides several data integrity measures including file checksum and optional CRC for each PDU**
- **Connectionless transport protocol using Deferred NAK ARQ allows high throughput for interplanetary distances**



# Why Not TCP/IP?

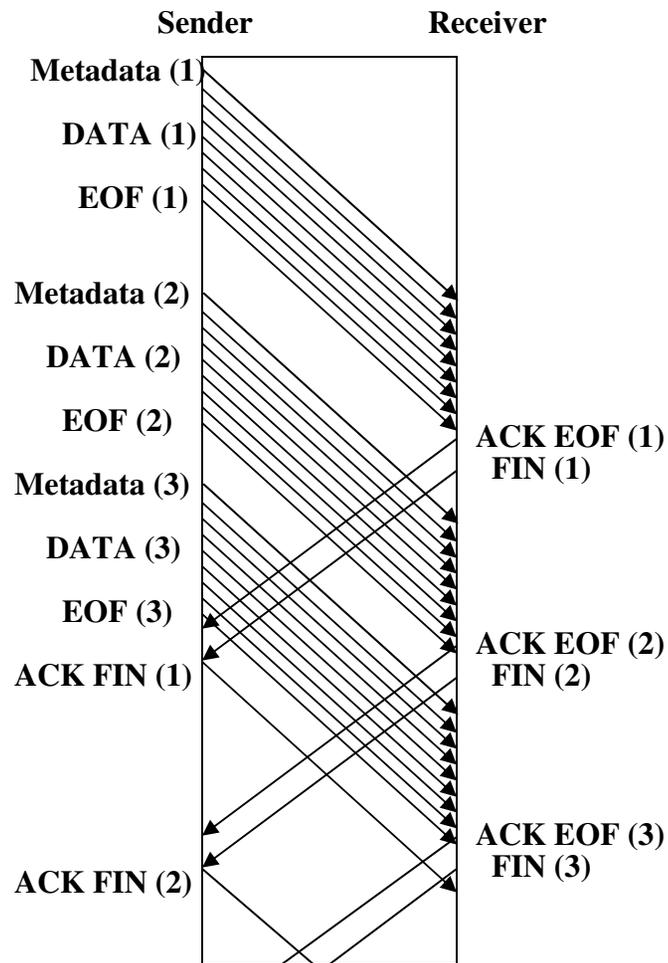
- **Establishing a TCP connection typically requires at least one round-trip delay.**
- **TCP receives data in transmission order only.**
  - Requiring lost data to be retransmitted and received before continuing
- **Throughput diminishes with increasing round-trip time**



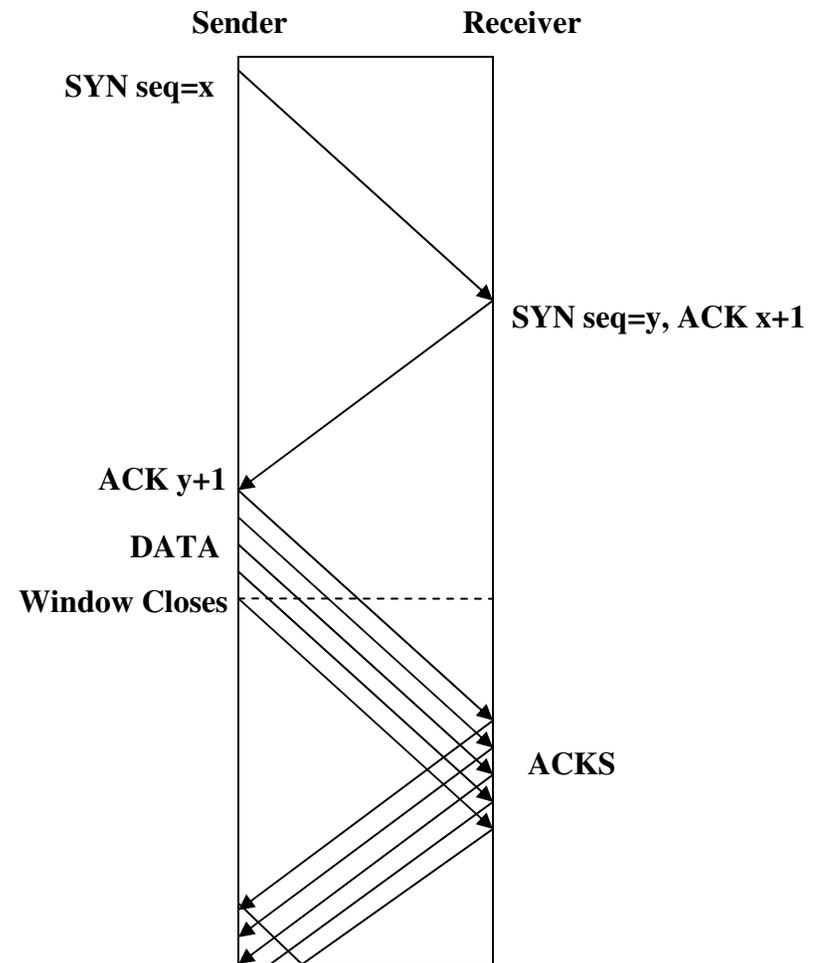
# CFDP with Deferred NAK vs. TCP



TRIGA

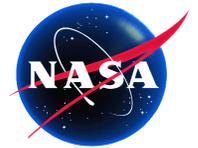


CFDP - High Delay Environment



TCP - High Delay Environment

# Recent Implementations



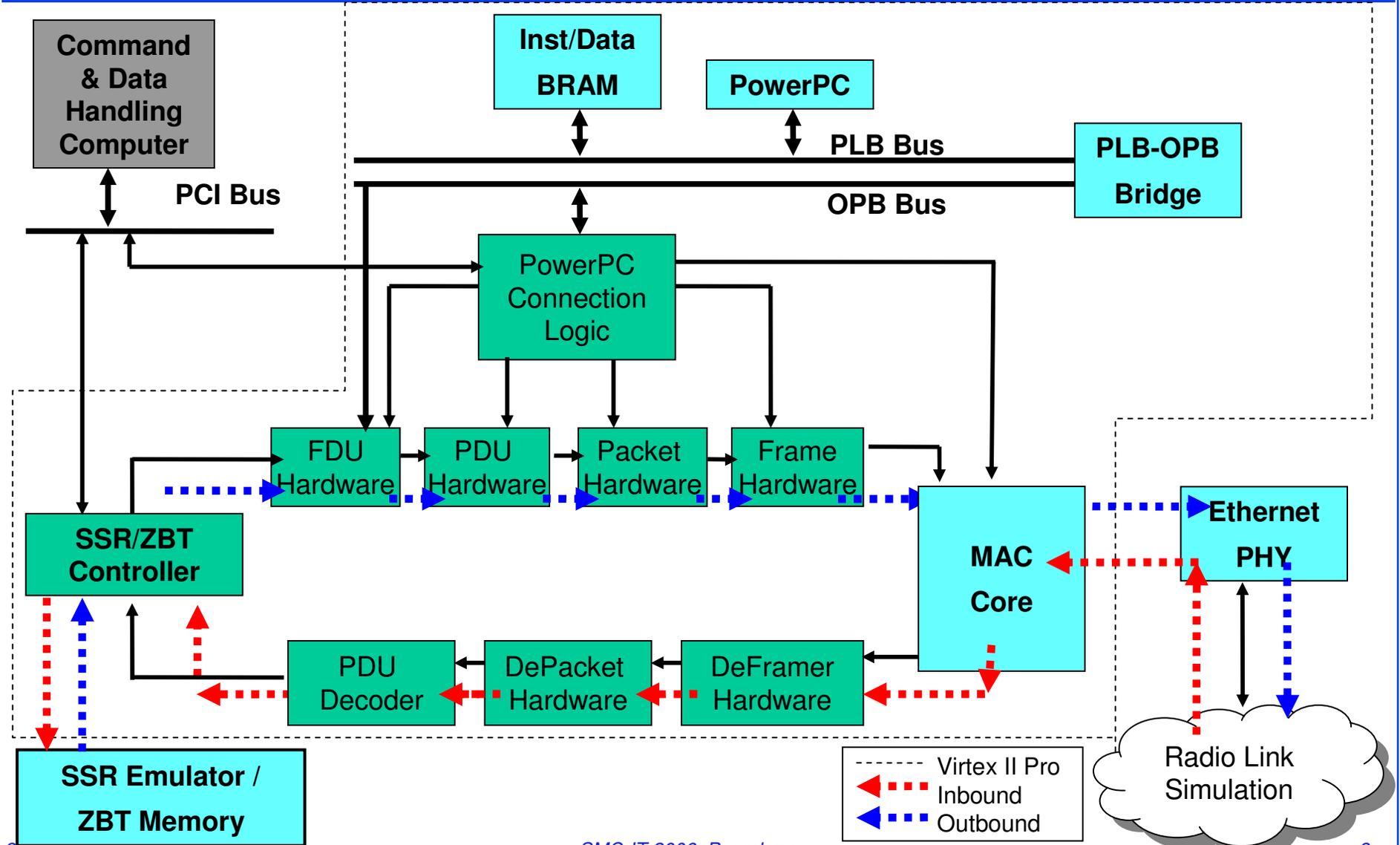
TRIGA

CCSDS Protocol		CCSDS	TRIGA	Deep Impact	MRO	OSI
Uplink to S/C	Downlink from S/C					
CFDP	CFDP	Flight SW	C&DH App	SW	SW	Application
		Transport	SW Stateful HW PDU			Transport
Space Packet	Space Packet	Logical Data Path	HW Packet			Network
Telecommand Space Data Link	Telemetry Space Data Link	Link Sublayer	HW TM/TC	Hardware	SW	Data Link
Telecommand Synchronization and Channel Coding	Telemetry Synchronization and Channel Coding	Channel Coding Sublayer				
R-S /LDPC/Turbo	R-S /LDPC/Turbo	R-S /LDPC/Turbo	N/A	R-S /LDPC/Turbo	R-S /LDPC/Turbo	Physical
RF	RF	Modulation	Ethernet	RF	RF	

# TRIGA System Architecture



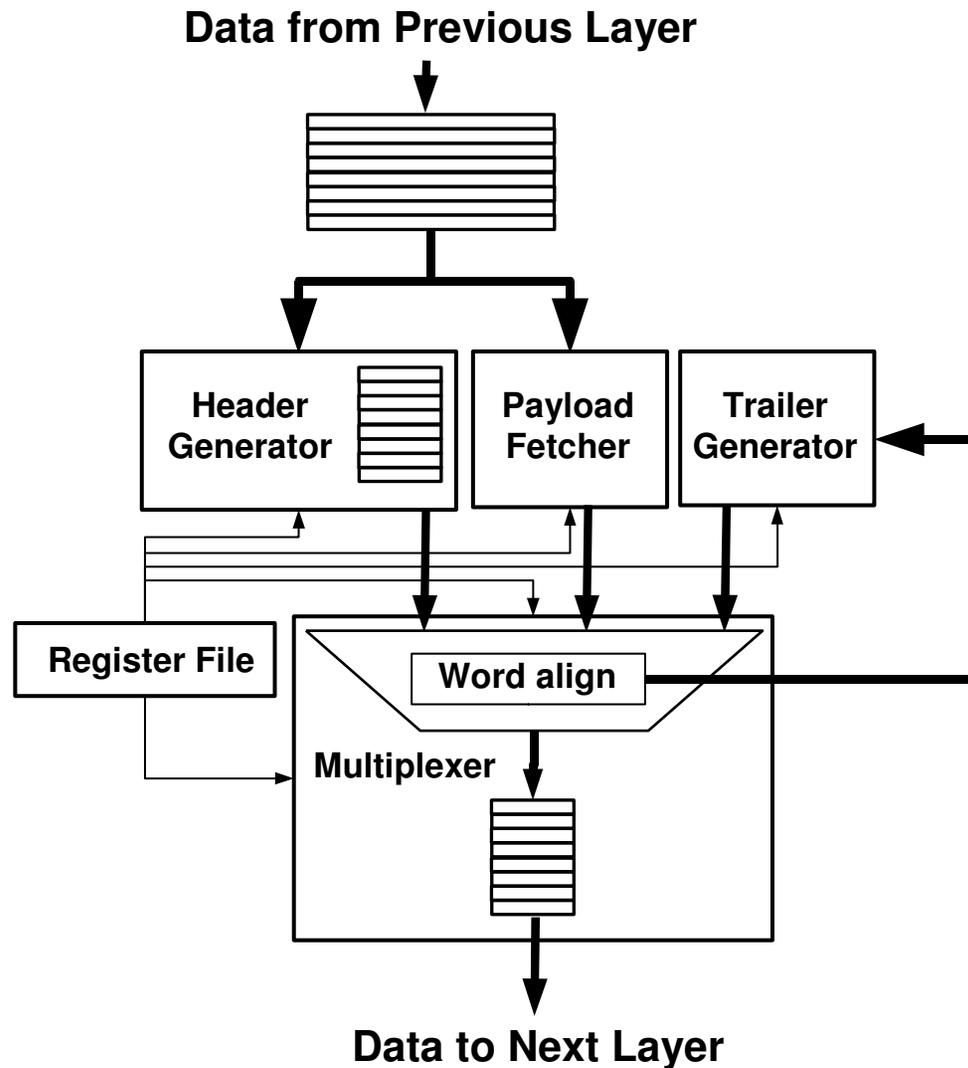
TRIGA



# Generic Outbound Processing Layer



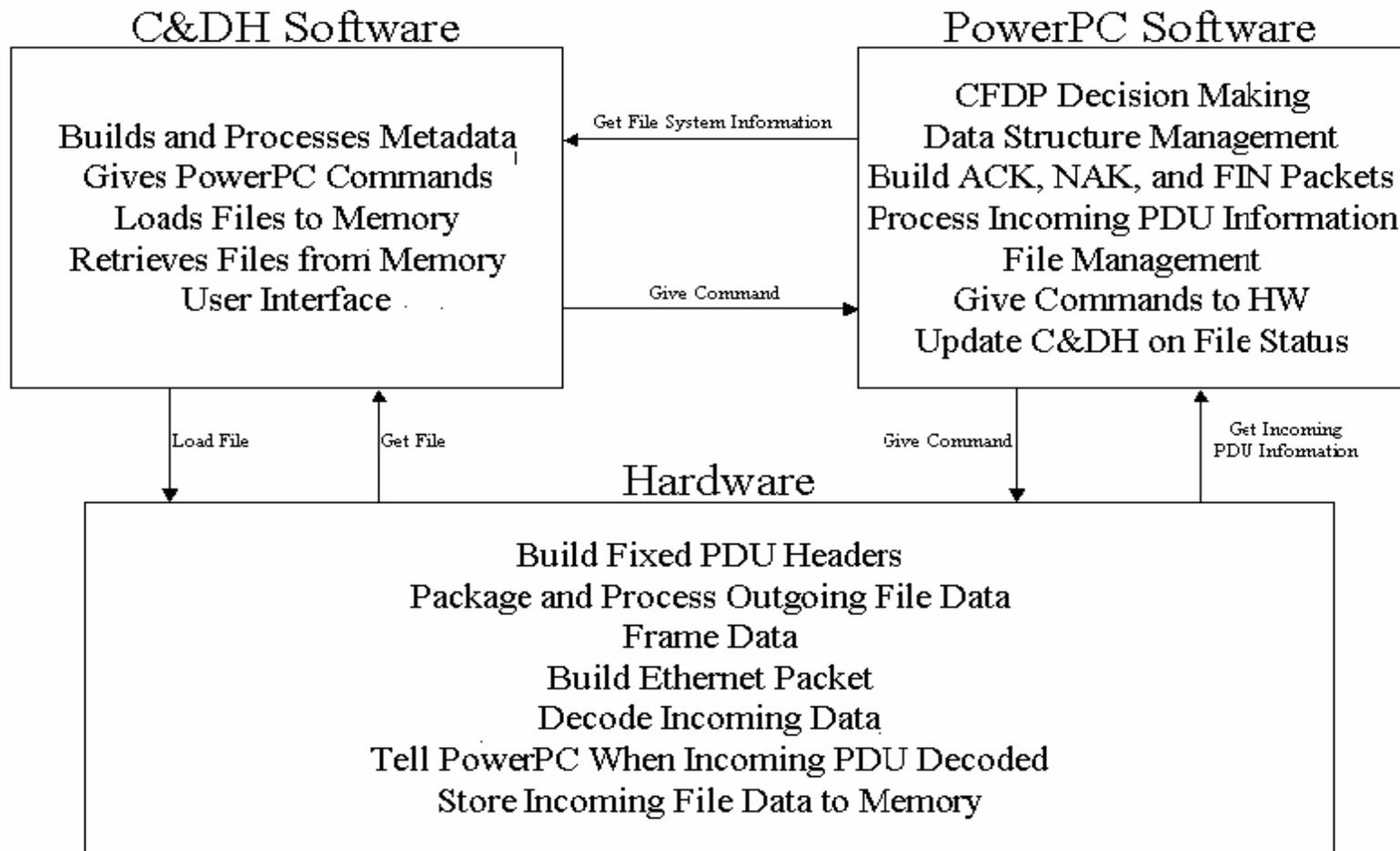
TRIGA



# Software Architecture



TRIGA



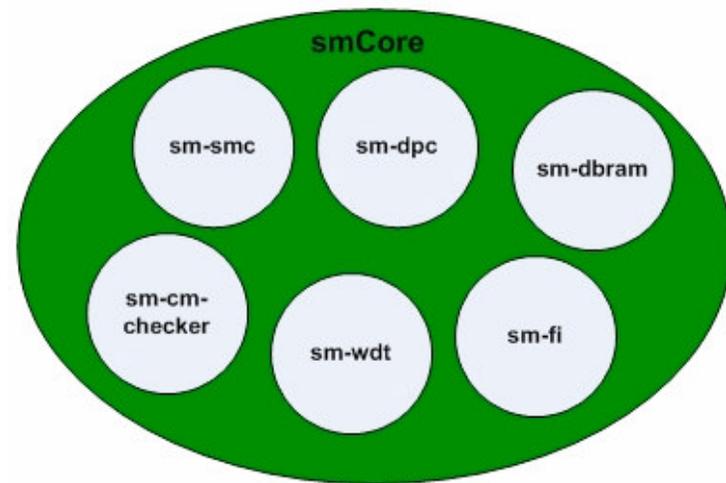
# Preliminary SEU Mitigation Design



TRIGA

- **Adapted from Mobility Avionics Project's SEU Mitigation Design *smCore***

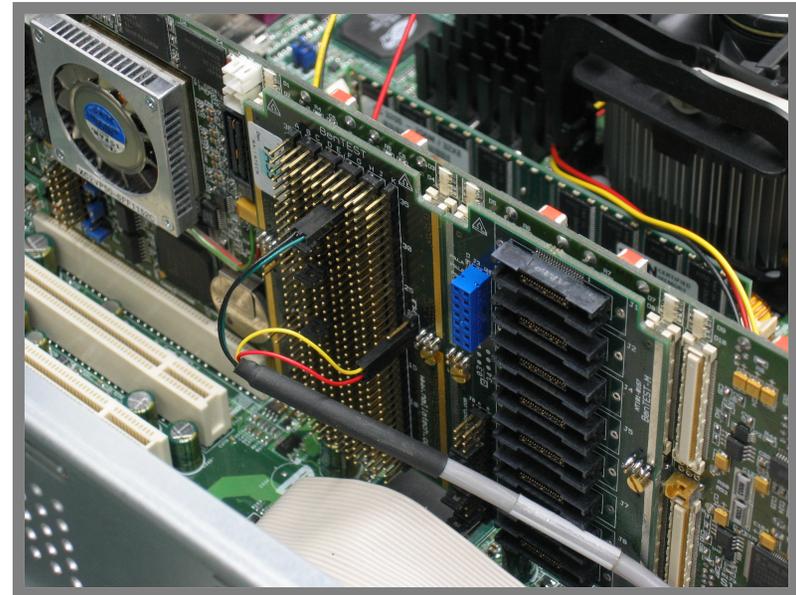
- SEU management core (*sm-smc*)
- Duplicate-and-compare for PPC405 (*sm-dpc*)
- CRC and readback-based configuration memory checker (*sm-cm-checker*)
- Duplicate-and-compare for Block RAM (*sm-dbram*)
- Watchdog timer for deadlocks (*sm-wdt*)
- Built-in fault injection for verification (*sm-fi*)



# Development Platform



TRIGA



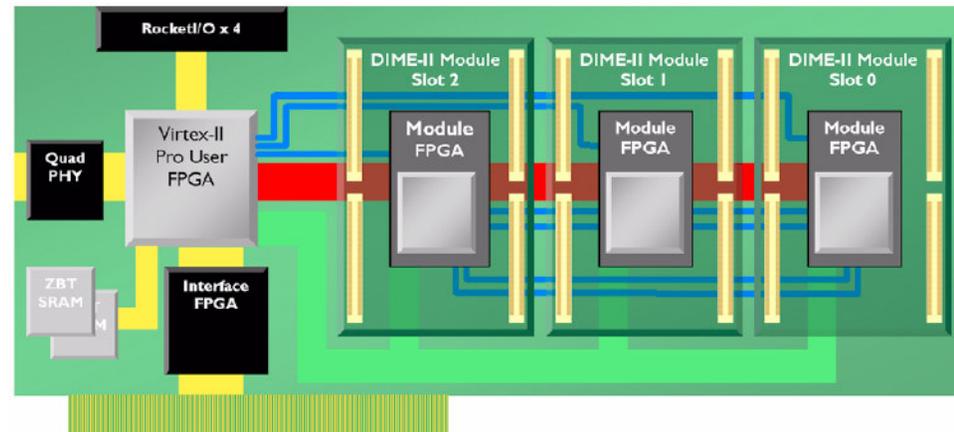
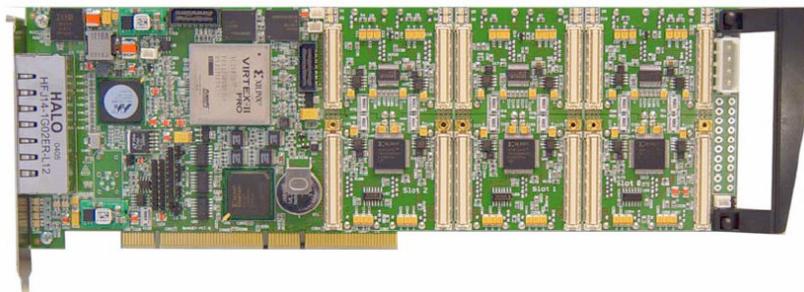
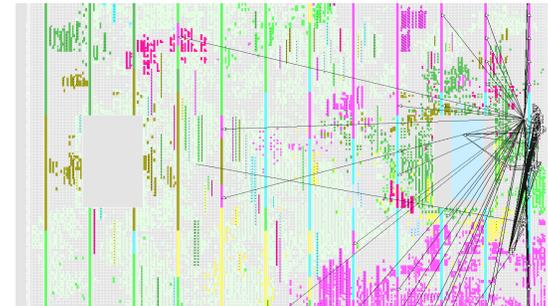
- **Nallatech BenNUEY-PCI-4E™**
- **BenTest Daughter Test Probe Card**
- **Fedora Core Linux with 2.6.9 Kernel**
- **Xilinx ISE and EDK for hardware synthesis**

# Development Platform



TRIGA

- **BenNUEY-PCI-4E™**
  - 4 Gigabit Ethernet ports
  - Virtex2Pro with 2 embedded PPC
  - PCI Interface
  - 2 banks of 512K x 32-bit ZBT memory (4MB each)
  - Add-on cards for LVDS communication
- Radiation hardened Virtex2Pro available now
- Allows for consolidation with other hardware in a single chip

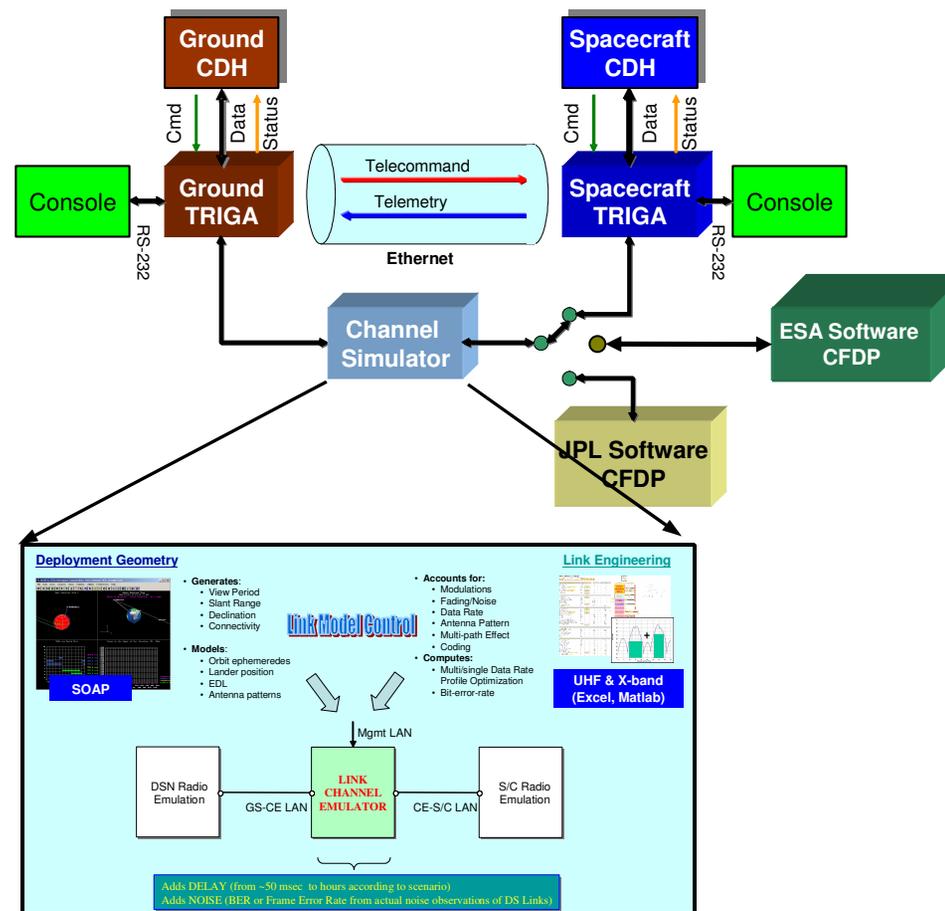




# System Verification

TRIGA

- Interoperable with ESA and JPL CFDP software reference implementations both Acknowledged and Unacknowledged modes



# Flight CFDP Stack Implementations



TRIGA

Deep Impact		Mars Reconnaissance Orbiter	
Hardware (Power)	Function (Data Copies)	Hardware (Power)	Function (Data Copies)
Rad 750,DRAM, cPCI Cntrl (8.6 W @ 132 Mhz)	Core CFDP (1)	Rad 750,DRAM, cPCI Cntrl (8.6 W @ 132 Mhz)	Core CFDP(1)
	Packetizing (1)		Packetizing (1)
			Framing (1)
Power PCI (1.5W @ 33Mhz)	Data Transport (1)	Power PCI (1.5W @ 33Mhz)	Data Transport (1)
Telecom HW (7.5 W @ 24Mhz)	Telecom HW SDRAM(1)	Telecom HW (3.9 W @ 24Mhz)	Frame CRC (1)
17.6 W	4 copies	14 W	5 copies
Peak Throughput (20 Kbit/s)		Peak Throughput : 5.2 Mbits/s	



# Device Utilization



TRIGA

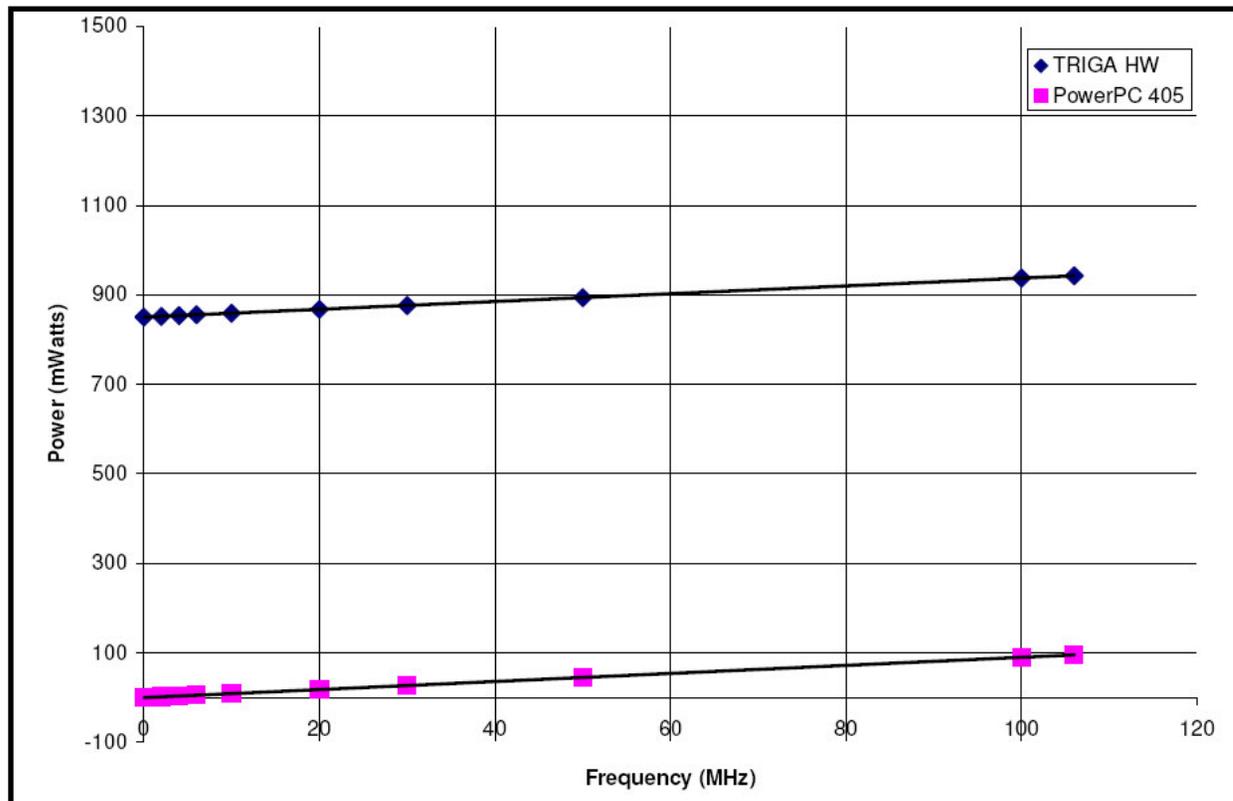
Component	Description	% of TRIGA HW
PPC Con Logic	Register Decode	2
PPC Peripheral	Xilinx IP Cores	7
C&DH I/F	Register Decode	4
Storage I/F	Memory Controller	5
FDU	Packetize File Data Unit	6
PDU	Packetize Protocol Data Unit	7
Packet	Packetize Space Packets	2
Frame	Packetize TM/TC Frames	7
Inbound	All Inbound Decoding Logic	26
Mac	GMII Interface to MAC PHY	34
<b>Total</b>		<b>100</b>



# Power Consumption



TRIGA



# System Level Improvements



TRIGA

- **C&DH Processing Burden:**
  - **Current Software Uses 55% of Processor Cycles for CFDP protocol processing**
- **TRIGA**
  - **4 Register Writes to Initiate Reliable Transfer**
  - **Minimal C&DH Usage for Creating Metadata (~34 byte packet)**
  - **Virtually a Total Reduction in Processor Cycles for the spacecraft C&DH**
  - **Decreased interconnection requirement between C&DH and the radio**
    - mass and spacecraft real estate saving
  - **One order of magnitude power reduction even with Single Event Upset Mitigation Design augmentation (Selective Triple Mode Redundancy) for radiation induced fault tolerance**
    - Full TMR increases the design size by 3.2 times maximum
    - TRIGA Selective TMR target design will require less than double the original resource utilization

