A 260-340 GHz Dual Chip Frequency Tripler for THz Frequency Multiplier Chains

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***Abstract*-We designed and fabricated a fix-tuned balanced frequency tripler working in the 260-340 GHz band to be the first stage of a ×3×3×3 multiplier chain to 2.7 THz. The design of a dual-chip version of this multiplier featuring an input splitter / output combiner as part of the input / output matching networks of both chips - with no degradation of the expected bandwidth and efficiency- will be presented.**

I. INTRODUCTION

Membrane technology enriched with beam-lead technology has opened new possibilities for frequency multipliers working at terahertz frequencies. The Jet Propulsion Laboratory (JPL) demonstrated in 2004-05 the first fully solid-state frequency tunable source able to pump a Hot Electron Bolometer (HEB) mixer at 1.9 THz [1][2]. Frequency multipliers offer the advantage of working at room temperature and providing 7-15 % of electronically tunable bandwidth in the 1-2 THz region. To go beyond 2 THz, more drive power in the range 800-1200 GHz and subsequently in the range 250-400 GHz is needed. The current work is aimed to create a wideband 300 GHz source to be used as a first stage of a ×3×3×3 chain to 2.7 THz.

II. SINGLE AND DUAL CHIP FREQUENCY TRIPLERS

A. Single chip frequency tripler design and results

The tripler features six GaAs Schottky planar anodes in a balanced configuration integrated on a few micrometer thick membrane. This tripler is similar to the 540-640 GHz tripler presented in [1]. The fabrication of the chip and the mechanical blocks was performed at JPL. Preliminary RF tests performed at JPL indicate that the multiplier covers the expected bandwidth and that the efficiency is in the range 1.5-7.5% with 100 mW of input power.

B. Dual chip frequency tripler design

A dual-chip version of the 260-340 GHz tripler was designed using two identical chips to increase power handling capabilities. The output matching circuit of both chips integrates a classic Y-junction that acts as a combiner. Similarly, a Y-junction is used to evenly divide the input power. Fig.1 shows a schematic of this multiplier. Simulations show that the dual-chip tripler should have the same bandwidth than the single-chip tripler with very similar efficiency.

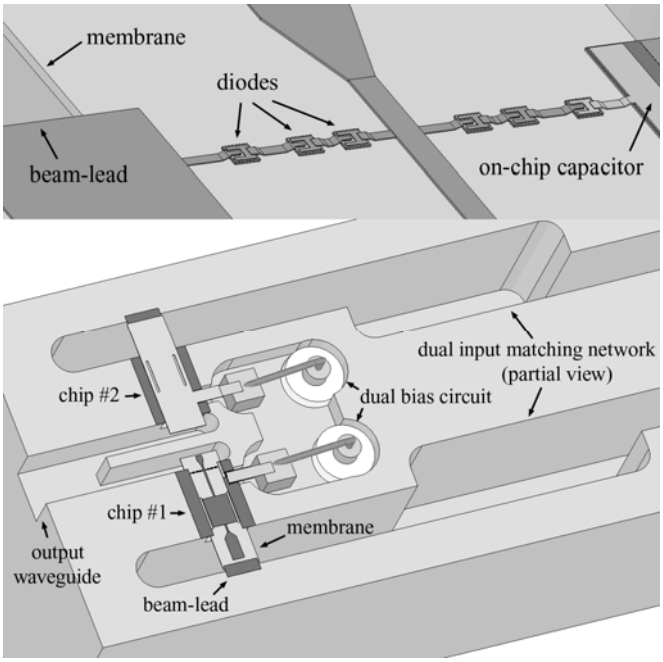

Figure 1. Top: Detail of the chip around the diodes. Bottom: schematic of the bottom block of the dual-chip 260-340 GHz frequency tripler (the dual input matching network is truncated). The waveguides in the top block are symmetrical with the bottom block.

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