Micro-Inspector Avionics Module (MAM): A Self-Contained Low Power, Reconfigurable Avionics Platform for Small Spacecrafts and Instruments

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ABSTRACT: This paper describes development of a radiation tolerant, low power, reconfigurable avionics module aimed at meeting the avionics needs of the JPL Micro-Inspector spacecraft. This module represents a complete avionics system, consisting of two PowerPC 405 CPUs embedded within a reconfigurable FPGA fabric of over 8 Million logic gates, 64MB of EDAC protected Flash storage and 128MB of EDAC protected DDR SDRAM or SDRAM memories, along with FPGA SEU mitigation logic, and all necessary power conversion. Processor SEU mitigation is achieved by running the two processors in a lock-step and compare configuration. All of these building blocks are integrated into a double sided circuit board that takes as little as 6 square inches of board space. This module can be embedded into a user system as part of a bigger circuit assembly or as a self contained module. This module is being developed as part of a JPL led Micro-Inspector Program, funded by NASA ESMD aimed at producing a 10Kg micro spacecraft.

1.0 Introduction

For future deep space and Earth orbiting missions JPL and NASA are pursuing the use of nano/pico-satellites in a variety of missions that up until now could only be accomplished using larger much higher cost system. These nano/pico sized missions require low power avionics that can fit within the physical constraints of such a system. The Micro-Inspector Avionics Module meets these needs by providing potential customers with a low power and mass avionics systems that can deliver state-of-the-art performance. This module can be used in areas besides nano/pico satellites such as small instruments and distributed systems in a larger spacecraft.

We intend to present our work in developing an integrated avionics platform based upon the Xilinx Virtex II Pro FPGA developed at JPL under the Micro-Inspector program that was sponsored by NASA Exploration Systems Management Division (ESMD), and the Mobility Avionics Internal Research and Technology Development (RTD) program. To meet the needs of these programs, an avionics platform must meet the following driving requirements:

Low Cost	Less than $50K for flight model
Low Power	Less than 3W total power consumption
Low Mass/Vol	Less than 200g; < 3” x 2” x 0.5”
Performance	Greater than 200MIPs
Radiation Tolerance	a) 100Krad for TID, b) 75MeV-cm2/mg for SEL, c) < 10E(-10) for SEU (after mitigation)

1.1 Prior Work: Mobility Avionics

The Mobility Avionics RTD, under the leadership of Gary Bolotin and R. Kevin Watson, led the way in the development of a Xilinx Virtex II Pro based avionics system. The goal of this effort was to develop a scalable, configurable, and highly integrated 32-bit embedded platform capable of implementing computationally intensive signal processing and control algorithms in space flight instruments and systems. This task developed a proof of concept of such a system based upon the Xilinx Virtex II Pro and commercial peripheral components. This task illustrated the modules power by demonstrating it in a distributed mobility application [1, 2]. This paper presents our work in taking this design to the next level of radiation tolerance by enhancing the design to include error detection and correction, and replacing the commercial peripheral components with ones with a direct path to flight qualification.

1.2 Micro-Inspector

The Micro-Inspector satellite is a light-weight, highly integrated satellite with less than 5 kg total mass with the following characteristics [4,5]:

- Avionics Package as described in this paper,
- a low-cost propulsion system with a specific impulse to providing delta-v capability,
- ultra-low power valves and thruster modules utilizing piezoactutaion technology,
- Celestial and vision-based navigation capability using a combination of cameras and laser range measurement instruments,
- Micro-transceiver UHF based telecommunication system for communication with host spacecraft,
- highly efficient triple junction cells
- Lithium ion battery for power storage.

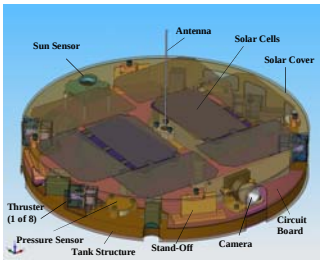

Figure 1: JPL’s MicroInspector

2.0 Avionics Hardware

The Micro-Inspector Avionics Module provides a self contained reconfigurable package with the capability to perform, signal processing, telecommunication, control algorithms, and distributed processing, and SEU tolerant processing at significantly lower power consumption, lower mass, and higher MIPS throughput than existing space qualified avionics This Avionics has the following characteristics:

Board Footprint:	5" x 6"
Board Mass:	200 grams
Processor:	Xilinx Virtex II Pro XC2VP40 FPGA with two Power PC405 CPUs
Memory:	192 MB (32Mx48) DDR SRAM, 96 MB (16Mx48) Solid State NOR Flash for mass storage, and 192 MB (32Mx48) SDR SRAM. All three have 16-bit additional data bits for error detection and correction (EDAC) capability.
Serial Interfaces:	Fast Ethernet, RS232
Features:	EDAC (single error detection, double error correction). **Flash File System**
Software capability:	Linux operating system
Electrical:	10-24 V input with about 3 W power consumption.

Figure 2: MAM: First Prototype

Figure 2, illustrates the completed first prototype of the Micro-Inspector Avionics Module as currently exists in the Micro-inspector avionics hardware testbed. We developed this module with components with a direct path to flight qualification. This module is the first demonstration of the avionics that will ultimately get embedded in the Micro-Inspector along with the avionics necessary to control the spacecraft. This module currently uses 7 bits of the 16-provided ECC bits for implementing an Error Detection and Correction scheme. In the future the full 16 bits can be utilized to accommodate high error control functions such as 8-bit correction and detection using Reed Solomon algorithms. For purpose of prototype testing the following features were added: one CPU reset push button and one FPGA reconfigure push button; Mictor connector for hardware and software debug; JTAG input port for external FPGA configuration.

Figure 3 illustrates the block diagram of the Avionics system. Major blocks include the FPGA with embedded processors, power converters, FLASH for mass storage, DRAM, PROM for FPGA image storage and I/O. Part selection for the major components was done by choosing components with flight heritage whenever possible. Issues such as radiation and temperature qualification were considered in the selection process. If a heritage component was not available then a search was done based upon components with a high likelihood of being successfully space qualified.

2.1 FPGA and Flight CPU

The two blocks at the center of the architecture are the Central Processing Unit (CPU) and the reconfigurable logic array. We looked at three options to implement these functions. The first was to partner a stand-alone CPU together with a Field Programmable Logic Array (FPGA). The second was to implement a CPU within the FPGA fabric as a soft core. The third was to see if we could take advantage of state-of-the-art system on a chip technology that packages a hard CPU core within an FPGA fabric. The following options were considered for these functions:

1. Actel RTAX-S with embedded ARM or 8051 core.
2. QPRO-R Virtex II with Micro-Blaze CPU implemented within the FPGA fabric.
3. Xilinx Virtex-II Pro with embedded 405 cores.

	Option 1	Option 2	Primary
Processor	ARM or 8051 core	Micro-Blaze	PowerPC 405
Type	Soft Core	Soft Core	Hard Core
Space Qualification	Yes	Yes	In-Progress
Frequency	30Mhz	150 Mhz	400 Mhz
MIPS		125 MIPs	600
MIPS/W	n/a	n/a	Up to1500
TID	200 krad(si)	200 krad	200 krad

We chose the path of the Xilinx Vitrex II Pro for its promise of space qualification, internal embedded CPU hard cores, and the ability to run the processors in lock-step for SEU detection and its raw performance of over 200MIPS and power normalized processor performance of over 1500MIPS/w. The Actel and Virtex II options both required either an external processor or a soft core in the FPGA fabric implemented from purchased IP and presented far less performance. SEU tolerance is achieved by running the two PowerPC processors in a lock step and compare fashion.

The Virtex-II Pro is the next generation of the Virtex II family with embedded IBM PowerPC 405 Processor hard cores, and RocketIOTM Multi-Gigabit Transceivers pins. It natively supports the low voltage differential signaling (LVDS) serial interface on hundreds of signal pairs and is capable of running real time operating systems: VxWorks and MontaVista Linux, on its embedded PowerPC processor(s). There could be as many as four embedded processors on a single FPGA, each running at speeds up to 400MHz, 600+ DMIPS. In addition, each RocketIOTM

MGT is capable of supporting data rates up to 3.125 Gb/s for high-speed serial transmission standards like Gigabit Ethernet, InfiniBand, RapidIO and PCI Express.

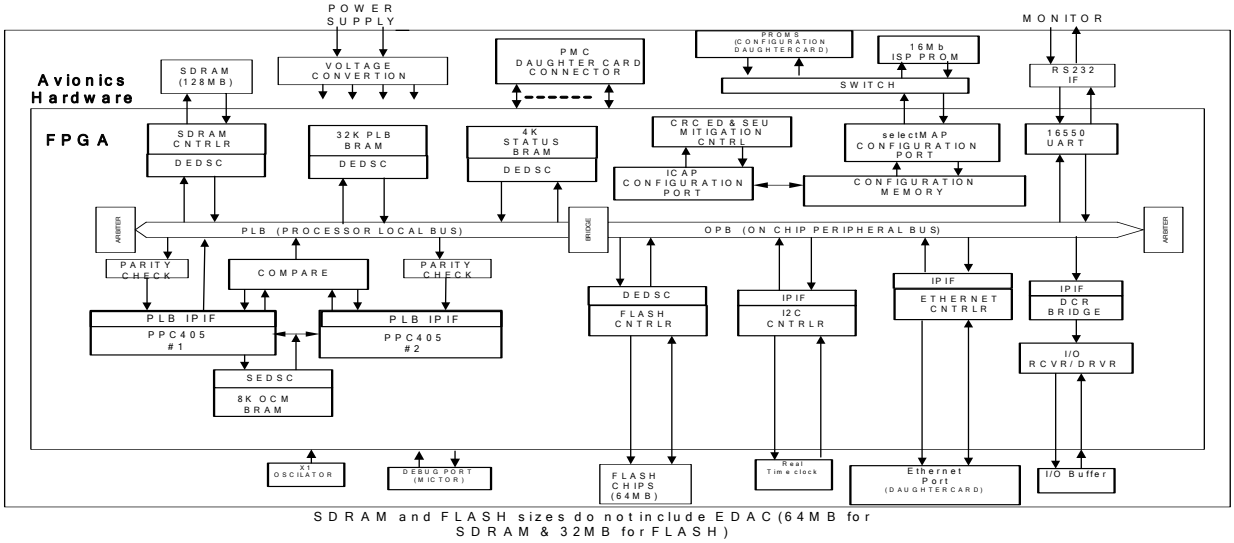

Figure 3: MAM: Block Diagram

2.2 Dynamic Memory– SDRAM, DDR SDRAM

Dynamic memory is used to store both the operating code and data for CPUs. In operation, code is copied from the non-volatile storage into the dynamic memory for execution. The following options were considered to meet the DRAM storage requirement.

1. Maxwell (97SD3248) 32Mx48 Module (uses Elpida SDR Die HM5225405B in a RadPak).
2. Elpida SDR (PN:EDS5116ABTA) 32Mx16.
3. Micron DDR (PN: MT46V32M16).

	Option 1	Primary	Backup
Part Number	Maxwell 97SD3248	Elpida EDS516ABTA	Micron MT46V32M16
Type	SDR MCM	SDR	DDR
Size	32Mx48	32M x 16	32M x 16
Max Speed	166 Mhz	166Mhz	200Mhz
Min Speed			~75Mhz
TID	200Krad(si)	200Krad(si)	unknown
SEL	>85MeV	>85 MeV-cm2/mq	unknown
SEU	2.7 MeV-cm2/mg	2.7 MeV-cm2/mg	unknown
TID	200 krad(si)	200 krad	unknown

The three options encompassed two versions of Single Data Rate (SDR) DRAM and a Double Data Rate DRAM device from Micron. Double Data Rate (DDR) memories provide higher density and access time performance than Single Data Rate (SDR) memories but currently they do not exist in a space qualified form. Preliminary radiation test data of DDR SDRAM show enough promise that we do feel that a DDR will be available in the future. We looked at SDR memories because they have been flight tested and flown in previous flight programs.

For the purpose of the Micro-Inspector, the Elpida SDR was chosen based on its known radiation tolerance. As a backup option we chose the Micron DDR because of its better performance and density. We did not choose this as our primary option because of its unknown radiation tolerance. Another DDR issue to consider is that DDR devices have a higher minimum frequency of operation requirement as compared to SDR memories. This leads to a higher minimum power draw when the system is operating in a safe and stand-by mode of operation. For the Micro-Inspector this was an important discriminator in that the Flight Software spends a good percentage of its time in a stand-by configuration.

We chose to develop our prototype module with both types of memory to keep our options open. The MAM utilizes three EDS5116ABTA (SDR) devices and three MT46V32M16 (DDR) chips on Micro-Inspector board. Two devices are allocated to the 32 bit external memory bus and one device is for error correction coding.

2.3 Non-Volatile Flash Storage

Non-volatile storage is used to store the flight software prior to execution, contains the boot loader and is used to store science and engineering data. The following options were considered to meet the non-volatile flash storage requirement.

1. Aeroflex Module PN: ACT-F2M32A, uses AMD Die Am29F016 in a Radhard package, used in MER, NOR Flash , 2Mx32 bits
2. Samsung PN: KM29U128T, used in X-2000, NAND Flash, 16Mx8 bits.
3. Maxwell Module PN: 69F1608, uses four 4Mx8 die, NAND Flash,16Mx8 bits
4. AMD/Spansion, PN:29JL064H90TAI00, NOR Flash,

	Option 1	Option 2	Option 3	Primary
Part #	Aeroflex ACT-F2M32A	Samsung KM29U128T	Maxwell 69F1608	AMD/Spansion 29JL064H90TAI00
Type	NOR Flash	NAND Flash	NAND Flash	NOR Flash
Size	2Mx32	16M x 8	16M x 8	4M x 16

Voltage	3.3v	3.3v	5.0v	3.3v
Controller	Simple	Complex	Complex	Simple
Availability	No	No	Yes	No
Space Qual	Yes	Yes	Yes	Unknown

Our candidates for non-volatile storage has been based on the flash based devices. These devices come in two basic types, NAND flash where a "NAND" gate builds up the basic building block and "NOR" flash where a "NOR" gate forms the basic building block. Based on preliminary radiation testing of Flash devices we believe that current NAND based flash devices are most likely to perform better in a radiation based environment. The JPL Mars Exploration Rover program flew successfully NOR flash based storage devices. However, these devices do not exist. Preliminary testing of current NOR flash devices has revealed the potential for latch-up related issues. From a user interface point of view, NOR based flash devices allow the user to write to the memory a word at a time. This is an important consideration for saving of state information in a real time system.

The inherent transistor circuit level architecture of the NAND Flash makes them less likely to experience latch-up but more vulnerable to Single Event Upset (SEU) than the NOR. The incorporation of NAND flash into a system is more difficult than NOR flash for two reasons. From a user interface point of view an entire block of memory is required to be written even if just a single byte write is required. In addition, the use of NAND FLASH requires a more complex memory controller than NOR Flash. On the positive side NAND flash devices come in higher density devices. In this case the AMD/Spansion part was used and Maxwell module or other NAND flashes could be utilized as well. In Micro-Inspector the flash is where the operating system resides. Upon power up a boot-loader along with the configuration file is loaded from PROM to the DDR SDRAM and fetches the operating system from the flash into DDR SDRAM. There are 12 NOR Flash (total capacity of 64MB user flash + 32MB EDAC) parts (PN: 29JL064H90TAI00) on this board. Four flash chips are used for 16-bit EDAC data bus.

2.4 I/O Interface

The MAM was designed to be embedded within the Micro-Inspectors main circuit board in addition to containing the avionics, this board would contain all the instrument, Guidance Navigation and Control (GNC) sensors electronics, and camera electronics. Adapting to this multitude of sensors and sensor interfaces posed a challenge to the development. We made use of the Xilinx Virtex II Pro capabilities by incorporating a majority of the functions either as cores within the FPGA fabric or implemented in software on the embedded PowerPCs. The reconfigurable nature of the FPGA and the ability to quickly change software made the accommodation of design changes, sensor requirement changes and fixes to design errors easy. For some applications this feature can be carried forward to flight operation.

The MAM was required to interface to the following sensors. Each of these sensors required their own custom interface core and software to communicate with the flight software:

1) Micro-sun sensor
2) cameras
3) laser based range detection
4) inertial measurement unit
5) Telecom
6) Power System
7) Thermal
8) Propulsion.

All of these I/O devices interface to the Avionics through custom or purchased cores connected directly to the OPB/PLB bus of the core connect bus architecture within the FPGA. An Ethernet interface was added to give our software development quick access to download software for ground and development operations. We intend to disable this interface in flight.

2.5 Serial PROMs

The Xilinx Virtex II Pro is a volatile device and needs external storage to store its initial configuration data, initial hardware state, and initial software load. The MAM required 16Meg bits of configuration data. We implemented this memory two different ways one for flight and one for development operations, selectable by jumpers on the board. The first option was implemented with a single space qualified electrically erasable XC17V16 PROM. For non-flight operations four of the Xilinx XC18V04 devices were required to hold the entire configuration dataset.

2.6 Avionics Software

2.6.1 Driving Requirements and Architecture

Design of the MAM Board Support Package (BSP) software is driven by the following requirements:

- Seamless integration with the hardware memory organization to provide a holistic computing environment for flight software applications.
- Open standard to facilitate fast and easy software development and to explore alternatives.
- Small binary footprint to maximize persistence storage available for application software.

The MAM BSP software is composed of five elements: (1) the mini boot-loader packaged with the FPGA configuration bit-stream, (2) the main boot-loader implemented with *U-Boot* [6], an open source universal boot-loader most popular, flexible, and actively-developed in the embedded systems community. (3) the open source Linux kernel ported to the MAM hardware, (4) the root file system shrink-wrapped and mounted as ram-disk, and (5) the generic memory I/O interface software implemented as a user space application.

Collectively they perform bootstrapping, hardware initialization and interfacing, and basic run-time services that include multi-task (process) scheduling and management, memory management, file systems, interrupt handling, time services, TCP/IP networking, hardware device control, etc. The following table shows its characteristics.

BSP Component	Size	Storage Media
Mini boot-loader	36KB	PROM
Main boot-loader	705KB	Flash Memory
Linux Kernel	602KB	Flash Memory
Root file system	1.61MB	Flash Memory
Memory I/O application	45KB	Flash Memory

2.6.2 Initialization Procedure

1. The mini boot-loader is stored in the PROM along with the FPGA configuration bit-stream. After FPGA configuration is finished and the on-chip PowerPC CPU powers up, it is loaded into the FPGA on-chip SRAM and starts execution. It then copies the main boot-loader from the flash memory to the off-chip DDR SDRAM and transfers control to it.
2. The main boot-loader executes in the 128MB DDR SDRAM and provides first-pass necessary hardware initialization and configuration, loads into the RAM the OS kernel and the root file system, passes the boot parameters, and hands over the control.
3. The Linux kernel boots up and mounts the root file systems.

2.6.3 Two Distinct Boot-loaders

The reasons of two distinct boot-loaders of various sizes are two folds: (1) Meet the small-size constraint of on-chip SRAM (128KB), and (2) decouple software development from hardware development so that constant changes in the main boot-loader do not lead to repackage with the FPGA bit-stream that requires the vendor-proprietary CAD tool.

2.6.4 The Generic Memory I/O Interface Software

A generic memory I/O interface software is implemented as a user space application based upon *mmap()* function. It provides a handy tool for developing new hardware.

2.6.5 Flash File System

File system management on the flash memory is implemented as *jffs2* (Journaling File System Version 2) using Linux MTD (Memory Technology Device) framework. It is a log-structure file system that provides wear leveling, data compression, and power-down reliability. Four partitions are created on the MAM flash memory as shown in the following table.

Partition	Size (MB)	Access Permission	Description
1	1.152	Read-Only	U-boot image and environment variables
2	1.25	Read-Only	Linux kernel
3	2.156	Read-Only	Root file system
4	58.25MB	Read-Write	Applications

Summary

The same architecture presented here with the flight qualified parts, could easily be extended for use in harsher environments than Mars and Leo orbit. For that purpose, it is possible to increase the TMR logics and even extend the memory error control methods to more than 8 bits detection and correction. The algorithms to control and navigate to perform flight operation are yet to be developed. The degree by which autonomy of the space craft is designed is application dependent and it could range from a fix to a very adaptive system.

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