Self-Adaptive System based on Field Programmable Gate Array for Extreme Temperature Electronics

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Abstract

Space missions often require radiation and extreme-temperature hardened electronics to survive the harsh environments beyond earth's atmosphere. Traditional approaches to preserve electronics incorporate radiation shielding, insulation and redundancy at the expense of power and weight. In this work, we report the implementation of a self-adaptive system using a field programmable gate array (FPGA) and data converters. The self-adaptive system can autonomously recover the lost functionality of a reconfigurable analog array (RAA) integrated circuit (IC) [3]. Both the RAA IC and the self-adaptive system are operating in extreme temperatures (from 120ºC down to -180ºC). The RAA IC consists of reconfigurable analog blocks interconnected by several switches and programmable by bias voltages. It implements filters/amplifiers with bandwidth up to 20 MHz. The self-adaptive system controls the RAA IC and is realized on Commercial-Off-The-Shelf (COTS) parts. It implements a basic compensation algorithm that corrects a RAA IC in less than a few milliseconds. Experimental results for the cold temperature environment (down to -180ºC) demonstrate the feasibility of this approach.

1. Introduction

The design of extreme environments electronics (outside the military temperature range) is a challenging task. The traditional approach uses thermal controls, which occupy volume, require power and reduce science payload. Another approach employs a *self-adaptive system* that automatically compensates for the functionality of the electronics which is lost due to thermal effects. Analog electronics experience drift in their characteristics and consequently need reconfigurable device, such as RAA IC, that can adapt to extreme temperature under programmable control [3]. On the other hand, digital electronics are more immune to such lost functionality as already demonstrated for extreme environment robotic applications [6] and therefore are excellent candidates to implement a self-adaptive algorithm using COTS parts. Experiments using a mixed-signal programmable chip (field programmable transistor array, FPTA) [1] and a stand-alone board-level evolvable system (SABLES) based on a digital signal processing (DSP) system [7] demonstrated the self-recovery of the FPTA functionality for temperature up to 280ºC and with total radiation dose up to 175krad. However the DSP system was operated at room temperature. In this work, we report an analog filter coupled with a compensation algorithm, both operating in extreme environment.

The rest of the paper is organized as follows: Section 2 provides an overview of the system. Section 3 describes the implementation details. Section 4 presents the control and command implemented on the Virtex-II Pro FPGA. Section 5 reports the experimental results of the self-adaptive algorithm. Finally, Section 6 provides conclusions.

2. System Overview

The self-adaptive system would take its inputs from a sensor, such as a water detector for a cold Moon environment [5], and feed the signal into our RAA IC. The RAA IC is performing analog signal conditioning such as filtering and amplification. The functionality of the RAA would be monitored periodically by generating excitation signals (such as sinusoids at different frequencies up to 1MHz) and applying these to the RAA. Its response is analyzed using the feature extraction block which performs a Fast-Fourier Transform (FFT) followed by amplitude and phase spectrum computations. In case the frequency response of the RAA deteriorates due to, for example, the

extreme temperature, the self-adaptive system will compensate for the degradation by re-configuring the RAA (Figure 1). The RAA is reconfigured by setting analog controls (Vbias from 0 to 3 V with 183µV precision) and programming digital controls (10 switches). The high resolution and low noise excitation signal feeding into the RAA allows the use of a low resolution ADC to evaluate the RAA response.

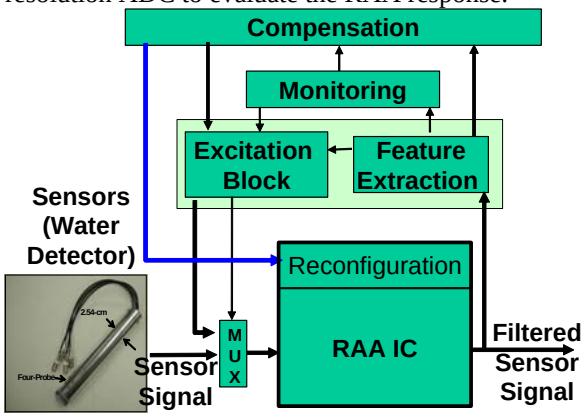

Figure 1 Self-adaptive system and RAA IC

The frequency response of the RAA IC is then re-evaluated. The compensation of low-order filter on the RAA IC uses dynamic hill-climbing algorithm in a small search space (up to 2 Vbias). Complex filters are compensated by evolutionary algorithm since the large search space (10 switches and 8 Vbias). The monitoring and the compensation mechanisms take only a few milliseconds.

3. Implementation

The electronics system is built around the RAA IC, a FPGA digital board, and few data converter boards.

The RAA IC, fabricated using TSMC 0.35µm silicon fabrication technology, consists of an array of four first-order Gm-C filter cell interconnected by 10 switches. The RAA achieves 20MHz bandwidth. The analog filters can be tuned by changing the two biasing voltages (two Vbias by Gm-C filter cell) to meet the specifications at extreme temperatures. The switches can be programmed to change the order of the filter implemented by the RAA IC [3]. In the self-adaptive system configuration, the two bias voltages of the first Gm-C filter are controlled by two DACs while the 10 switches are programmed directly by the FPGA.

The digital board has been implemented using a Xilinx Proto-board with a 100MHz clock PowerPC and 2MHz clock for the FPGA fabric. The data converter boards include three COTS DACs and one ADC which communicate with the FPGA as shown in Figure 2. Two DACs set the two Vbias (0 to 3 Volt with 183µV precision) of the first Gm-C filter cell in the RAA. The other DAC generates the excitation signal (sinusoid up to 50MHz). The FPGA is also connected to the RAA to program the 10 switches of the RAA. Finally the FPGA extracts the response signals from the RAA using one ADC. The PC executes a hyperterminal window to control the different functionalities implemented on the FPGA such as setting the Vbias, programming the switches, and reading the temporal and frequency response of the RAA IC stored in FIFOs.

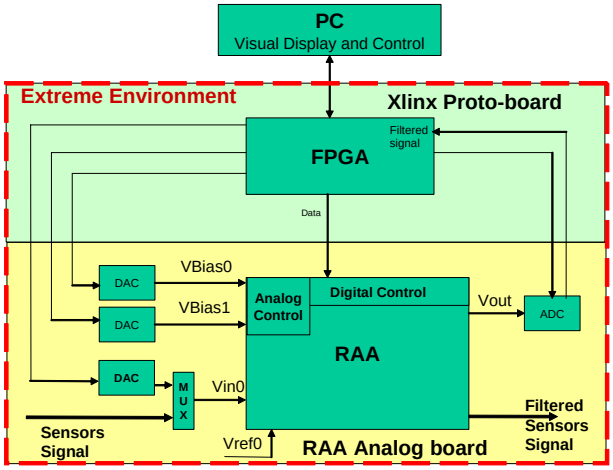

Figure 2 Hardware/software architecture

Extreme temperature tests were performed individually upon devices necessary for the self-adaptive system. Though the performance deteriorates, the ADC-DAC chain can be effective at cold temperature[2]. The Xilinx FPGA Proto-board was also been tested to verify its operation at cold temperature with external clocks and DC power supplies.

Figure 3 shows a photograph of the entire hardware platform which includes the FPGA Proto board on the right side and the custom analog/digital boards on the left. The modular hardware platform enables the addition of DACs and ADCs boards depending on the controls of the RAA ICs. The hardware platform employs an external 2MHz common clock connected to the FPGA fabric through the ADC. Another 100MHz clock is connected to the Xilinx Proto board to feed to the PowerPC on the FPGA. The PC controls the FPGA through a serial bus interface. For extreme temperature testing, the hardware platform, except the power supply board, was put in the cryogenic thermal chamber.

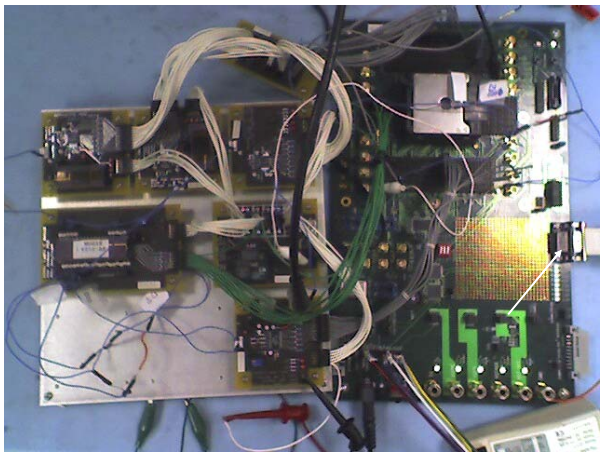

Figure 3 Hardware/software implementation

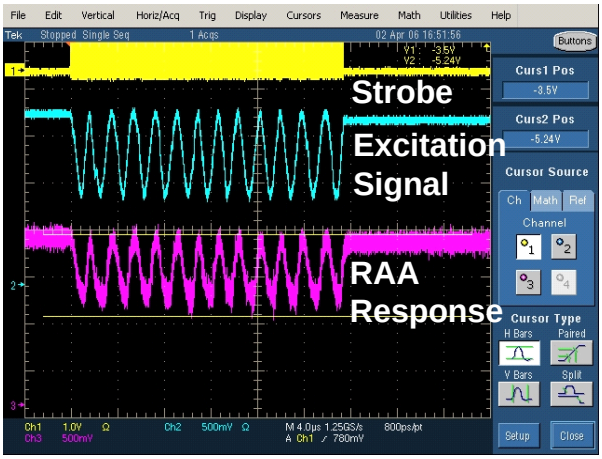

Figure 4 Excitation signal and RAA response

In the future, the RAA-IC will take its input from multiple sensors and compensate not only for extreme temperatures but also for sensor degradation.

4. FPGA Implementation

The FPGA implementation includes software and hardware modules. The software modules control the sequence of operations using a simple user interface running on the PC. The hardware modules control the DACs, the ADCs, and the RAA.

The reconfiguration algorithm hardware intellectual property (IP) was implemented on the FPGA fabric and includes blocks such as an excitation signal generation block to generate a sine wave from a few Hz up to 1 MHz; a RAA configuration block to program the RAA switches; a block to extract the frequency response of the RAA IC; and DAC control block to set the Vbias through the DACs. We have used also IP cores from the Xilinx LogiCore Library. The user interface and reconfiguration algorithm software resided on the block RAM (embedded memory) on Virtex II Pro and was executed by one PowerPC cores of the FPGA.

Figure 4 shows an oscilloscope picture of the excitation signals and the corresponding RAA response at room temperature. The FPGA acquires the RAA response through the ADC and extracts the frequency response using the on-board FFT block. The excitation signal frequency can be varied from 1Hz to 1 MHz (with 2 MHz ADC clock).

Figure 5 shows an oscilloscope picture of the RAA response for different Vbias values. Vbias1 is fixed and Vbias0 is swept. The excitation signal is a 50kHz sine wave. We can observe that there is a narrow range of optimal values for the Vbias0 which yield maximum amplitude of the RAA response as depicted by white vertical line.

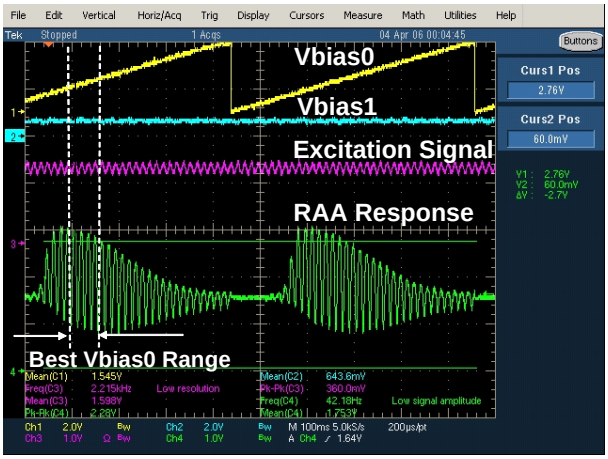

Figure 5 RAA Response of a 50kHz sine wave input signal when sweeping Vbias0 and fixing Vbias1.

5. Self-Adaptive Algorithm

The goal of the system is to compensate autonomously for the effect of temperature on the frequency response of the RAA by changing the two Vbias voltages. We have used the Dynamic Hill-Climbing algorithm introduced by Yuret et al. [4]. This algorithm reduces the number of evaluations and performs well for smooth fitness landscape. We start with a potential solution represented by a point in a two dimensional search space such as the optimal value of Vbias0 and Vbias1 at room temperature. We then use a hill-climbing method to find the best neighboring point and continue until no more

improvements are observed. Then we decrease the search radius to zoom in on the optimum. If the found optimum value is of unacceptable fitness, a new starting point is found by computing a location that is farthest in the search space from all local optima already found. We repeat the process until a desirable optimum is found.

We applied the algorithm to search for the values of the two Vbias voltages to obtain the maximum gain of the RAA filter at 50kHz at cold temperature. The result of the algorithm operation is shown on Figure 6. The horizontal axis indicates the number of evaluation. Each evaluation is associated with Vbias0 and Vbias1 values. The vertical axis shows the peak to peak amplitude of the RAA response. In this experiment, the excitation signal is a 50kHz sine wave.

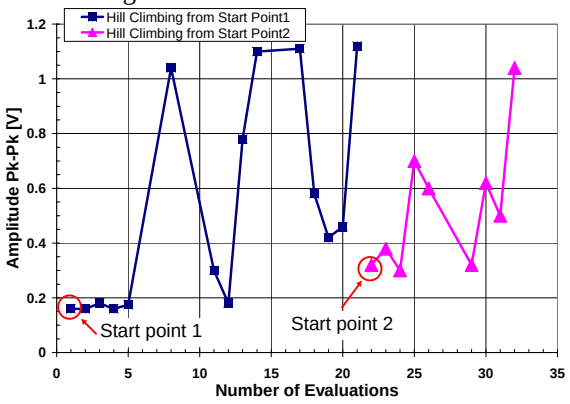

Figure 6 Evolution of the amplitude Pk-Pk of the RAA response through dynamic hill-climbing at T=-180ºC.

We invoke the algorithm when the temperature in the chamber is T=-180ºC. The Vbias were kept at their optimal values at room temperature providing a gain of +20dB for a 50kHz sine wave input signal (Start Point 1) (Figure 7). If the new Vbias0 and Vbias1 yield a better response than the current best one, we keep it and restart the exploration around that point (Figure 6).

Figure 7 RAA Response at -180ºC before optimization of the gain of the RAA at 50kHz.

The algorithm was able to increase the gain of the RAA filter at 50kHz back from -7dB to +10dB by changing the Vbias0 and Vbias1(Figure 8).

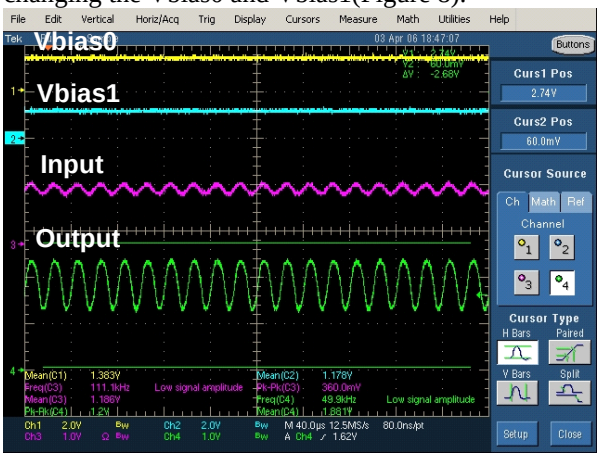

Figure 8. Best RAA Response at -180ºC after 21 evaluations using start point 1 for Vbias voltages.

The algorithm continues with a new starting point of the Vbias voltage (Start Point 2) providing a gain of -1dB at -180ºC (Figure 7). The algorithm was able to increase the gain of the filter at 50kHz from -1dB to +9.1dB by changing the Vbias0 and Vbias1 (Figure 9).

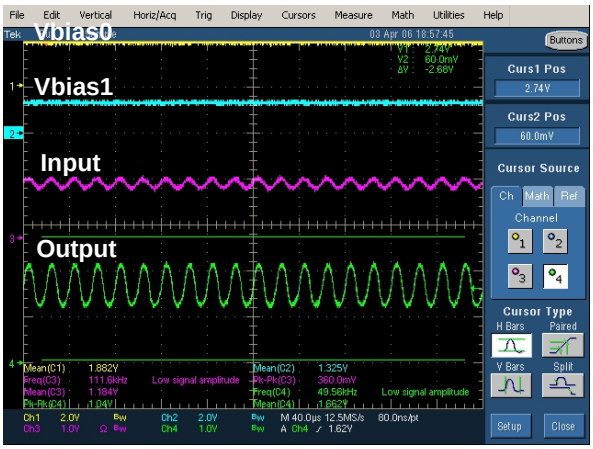

Figure 9. Best RAA Response at -180ºC after 12 evaluations using start point 2 for Vbias voltages

The evaluation of each Vbias0, Vbias1 pair takes 150µs. It includes the time to set the two Vbias voltages (2*32µs), to generate the excitation signal (28µs), and to calculate the FFT from the RAA response (50µs). The algorithm (written in C) is currently implemented on the PowerPC.

6. Conclusion

The compensation method for the RAA based on an self-adaptive reconfiguration algorithm shows great promise as a technology to replace the thermal protection or the expensive development of new technology processes surviving at extreme temperatures for future NASA applications. We demonstrated experimentally at -180ºC, using a self-adaptive system using COTS components graded for only commercial range of temperatures that we can, for the first time to our knowledge, autonomously compensate for the gain of analog filter by changing Vbias voltages. We also showed that our self-adaptive system is able to evaluate the response of the RAA and to modify the Vbias voltages in less than 150µs, thus decreasing the time required for compensating to a few milliseconds. Additionally, a future design will include the data converters and the digital processing on-chip next to the RAA to allow for *in-situ* compensation of RAA if there is an unexpected change in the behavior due to temperature shift, radiation or other faults.

The novel capability of fully automated analog circuit compensation, integrated in a single device next to the sensor(s), would enable robust, low-mass, low-power, and low-noise sensor(s) operating in extreme environment.

Acknowledgments

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