



Temperature-adaptive circuits on reconfigurable analog arrays

**Adrian Stoica
Ricardo S. Zebulum
Didier Keymeulen
Rajeshuni Ramesham
Joseph Neff¹
Srinivas Katkooi²**

Jet Propulsion Laboratory
California Institute of Technology

¹SPAWAR

² University of South Florida



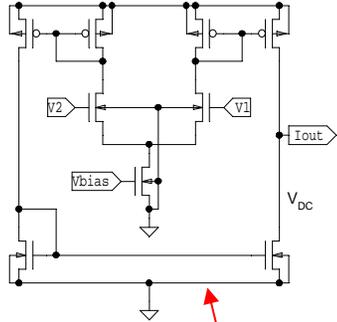
- Introduction
- Reconfigurable Analog Array (RAA)
- Self Adaptive System
- Experimental Results
- Conclusions

- Demonstration of a self-reconfigurable Integrated Circuit (IC) that would operate under extreme temperature (-180°C and 120°C) and radiation (300krad), without the protection of thermal controls and radiation shields.
- Self-Reconfigurable Electronics platform:
 - Evolutionary Processor (EP) to run reconfiguration mechanism;
 - Reconfigurable chip (FPGA, FPAA, etc).

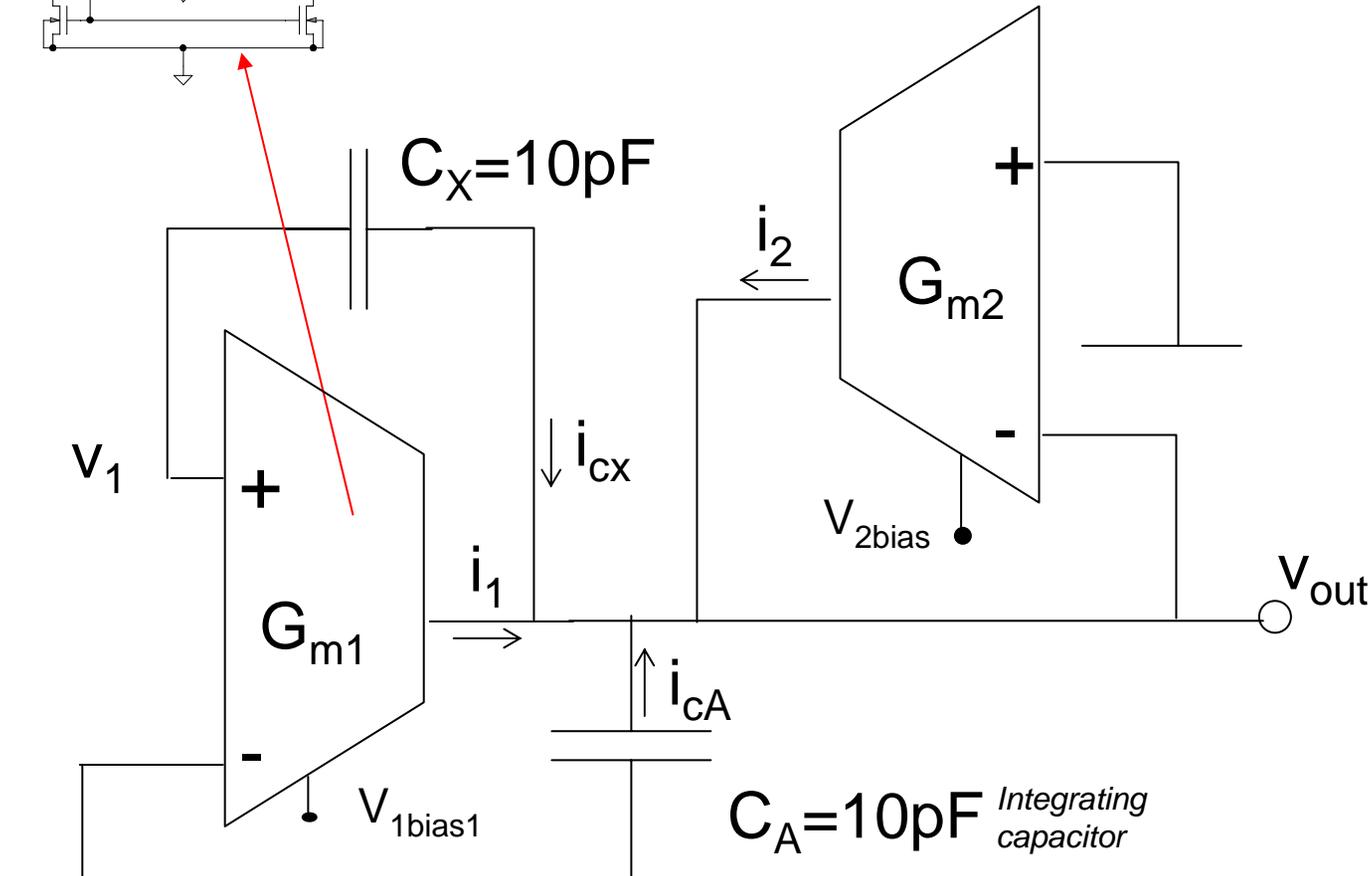


Reconfigurable Analog Array (RAA) **JPL**

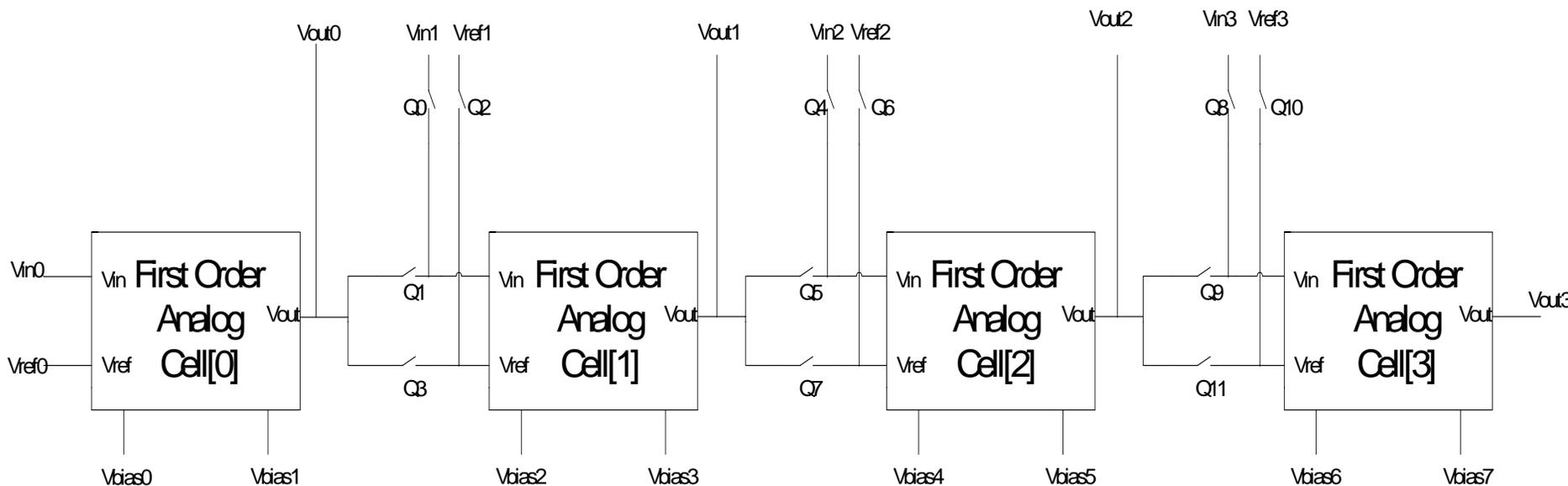
WRTA block:



Analog cells - 1st
order low-pass
Gm-C filter



- WRTA transconductance, G_m , dependent both on the temperature and on the voltage applied to V_{bias} ;
- Circuit response can be corrected at extreme temperatures through changes in the V_{bias} ;
- A prototype RAA IC was fabricated as an array of 4 first-order G_m -C filters interconnected by switches using TSMC 0.35/3.3V;





Self Adaptive system

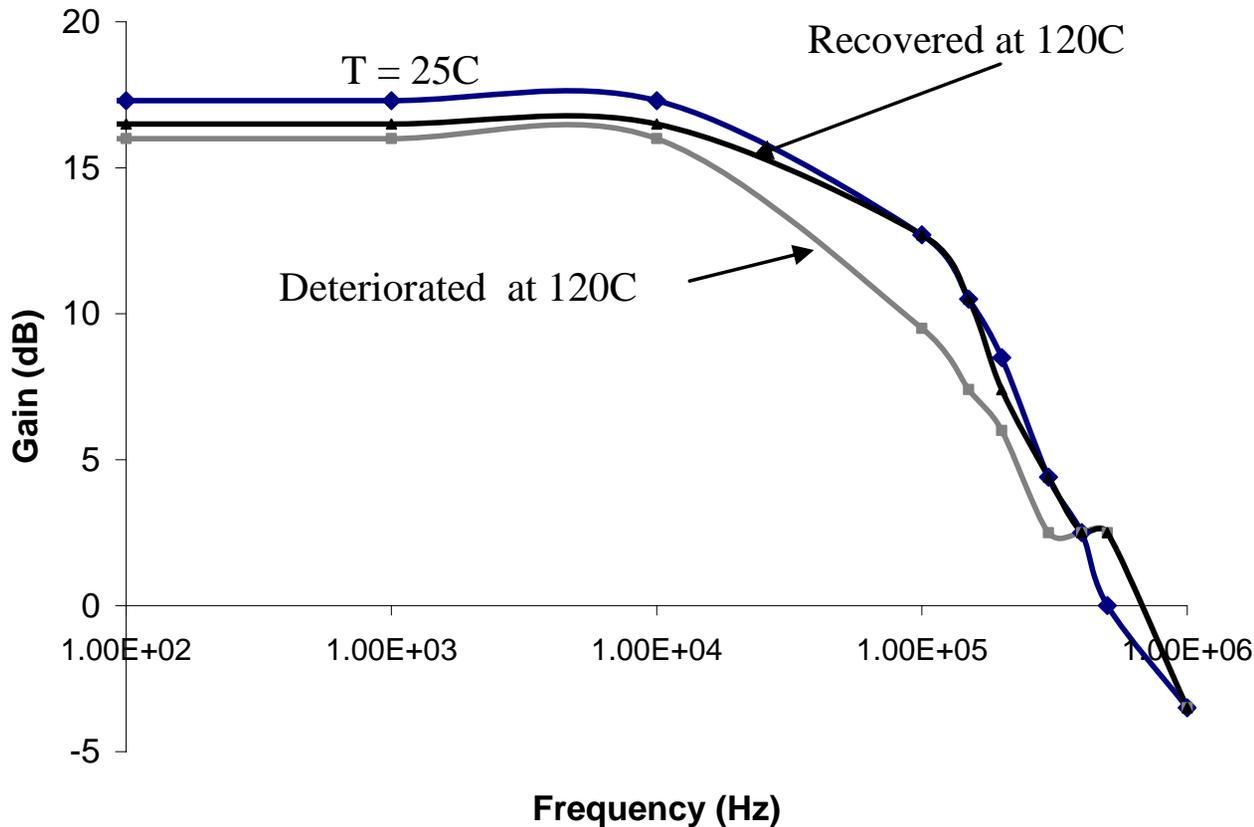


- Includes Evolutionary Processor (implemented in an FPGA) and reconfigurable analog device (RAA);
- Two board system:
 - FPGA Virtex-II Pro Protoboard;
 - Analog board based on RAA (including data converters and power distribution).
- FPGA controls reconfiguration based on search algorithms (dynamic hillclimbing) seeking solutions over bias voltage values.
- Analog board:
 - Two digital-to analog converters (DAC) daughter boards send bias voltages (programmed by the FPGA) to configure the RAA (motherboard), and the third one sends the input signal synthesized by the FPGA to the RAA;
 - ADC daughter board reads back the RAA output to the FPGA board.



Experimental Results – High Temperatures **JPL**

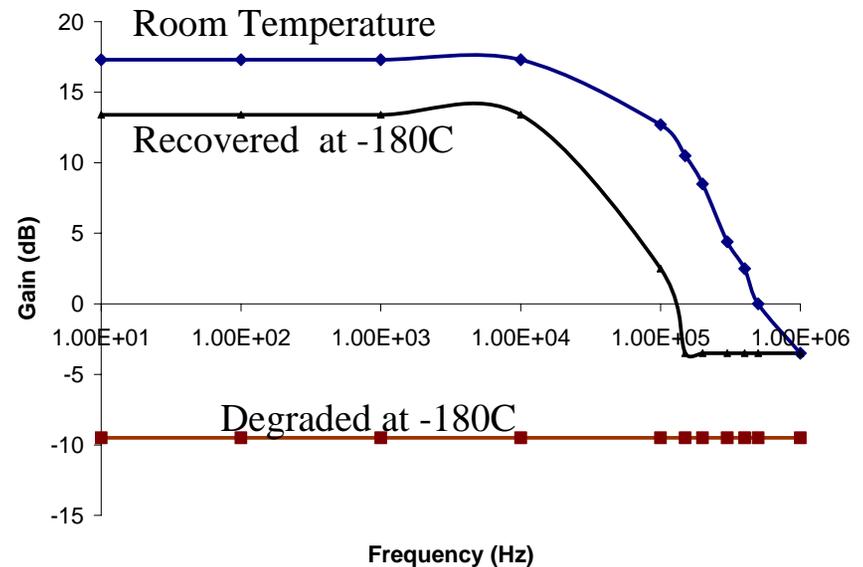
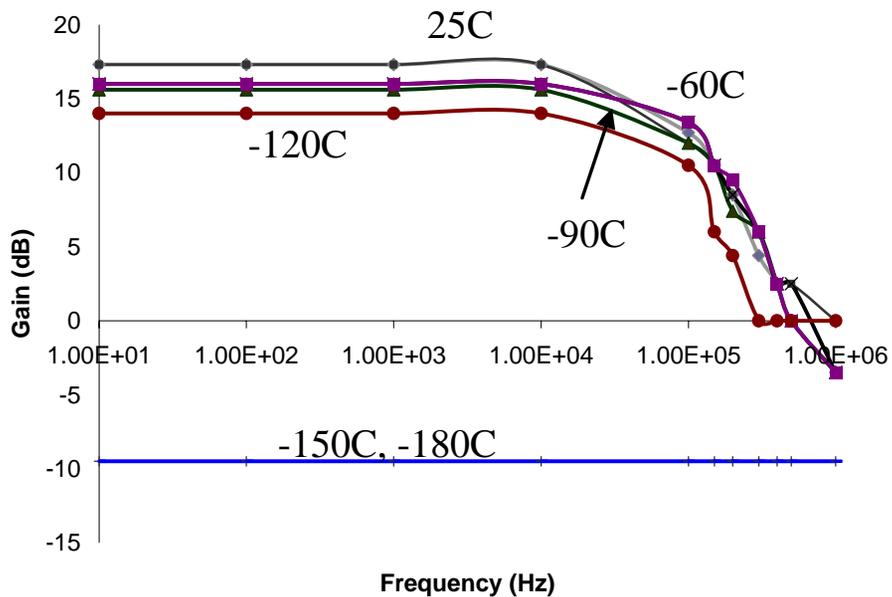
- Low pass filter: 20dB gain, 100kHz cut-off frequency;
- Initial setting for bias voltages ($V_{b1} = 0.9V/V_{b2} = 0.7V$);
- A small deterioration in the filter response is observed at 120°C. After **manually** changing the bias voltages V_{b1} and V_{b2} to 1.1V and 0.6V respectively, a partially recovered response was achieved.





Experimental Results – Low Temperatures **JPL**

- Response degrades below -120°C ;
- **Manual** recovery at -180°C : change in V_{b1} from 0.9V to 0.8V



Low Temperature – Automatic Recovery Through HillClimbing

Room Temperature

Vb1
Vb2
Input
Output



T = -180°C Deterioration



T = -180°C Recovery

Vb1
Vb2
Input
Output



New solution for -180°C is Automatically found by search Algorithm (new bias voltages are 1.89V and 1.31V)

- Demonstration of self-adaptive system at extreme temperatures;
- Circuit recovery performed in less than one minute;
- Future works:
 - Recovery of higher order filters;
 - Recover from combined effects of extreme temperature and radiation;



Acknowledgements



- The work described in this paper was performed at the Jet Propulsion Laboratory, California Institute of Technology and was sponsored by the National Aeronautics and Space Administration (NASA). We are grateful for encouragement and support from Project Manager Dr Michael Watson from NASA Marshall Space Flight Center, and NASA Program Managers Dr Mita Desai and Dr. Chris Moore.