Power Actuation and Switching Module Test Results

Greg Carr*, Frank Deligiannis, Lauro Franco, Loren Jones, Barbara Lam, Ron Nelson,
Jose Pantaleon, Ian Ruiz, John Treichler, Gene Wester
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, CA 91109

Jim Sauers, Paul Giampoli, Russ Haskell, Jim Mulvey, John Repp
Lockheed Martin – Commercial Space Systems
100 Campus Drive
Newtown, PA 18940

Abstract—

The X2000 Power System Electronics (PSE) is a Jet Propulsion Laboratory (JPL) task to develop a new generation of power system building blocks for use on future deep-space missions. The effort includes the development of electronic components and modules that can be used as building blocks in the design of generic spacecraft power systems. All X2000 avionics components and modules are designed for use in centralized or distributed spacecraft architectures.

The Power Actuation and Switching Module (PASM) has been developed under the X2000 program. This component enables a modular and scalable design approach for power switching applications, which can result in a wide variety of power switching architectures using this simple building block. The PASM is designed to provide most of the necessary power switching functions of spacecraft for various Deep Space missions including future missions to Mars, comets, Jupiter and its moons. It is fabricated using an ASIC process that is tolerant of high radiation.

The development included two application specific integrated circuits (ASICs) and support circuitry all packaged using High Density Interconnect (HDI) technology. It can be operated in series or parallel with other PASMs. It can be used as a high-side or low-side switch and it can drive thruster valves, pyrotechnic devices such as NASA standard initiators, bus shunt resistors, and regular spacecraft component loads. Each PASM contains two independent switches with internal current limiting and over-current trip-off functions to protect the power subsystem from load faults. During turnon and turnoff each switch can limit the rate of current change (di/dt) to a value determined by the user. Three-way majority-voted On/Off commandability and full switch status telemetry (both analog and digital) are built into the module. This paper is a follow up to the one presented at he IECEC 2004 conference that will include the lessons learned and test results from the development.

* Engineering Manager, Section 346, 4800 Oak Grove Drive/Mail Stop 303-300, AIAA Member.

I. Introduction

The X2000 Power System Electronics (PSE) Development is a Jet Propulsion Laboratory task developing a new generation of power system building blocks for use on future deep space missions[1]. The development approach has been to partition the power system architecture into functional building blocks that can be developed to meet the environmental requirements of deep space missions. Each building block is assessed on the criticality of the function and the number of times the function is repeated throughout the power system.

The X2000 PSE has been functionally partitioned into a power control function, power distribution function and house-keeping supply function. Each function has been subdivided into building blocks where the some of the common building blocks will be used across the functional boundaries. The functional elements are shown in Figure I-1.

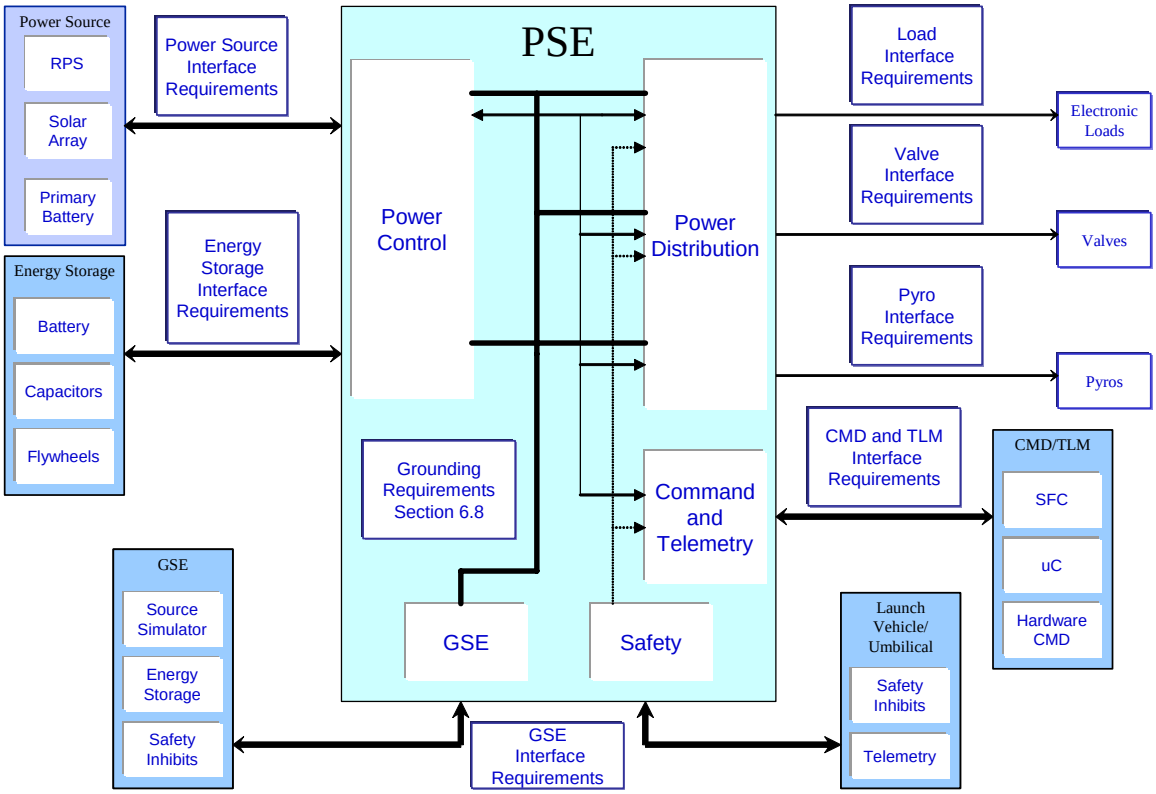

Figure I-1: PSE Functional Block Diagram

Based on the functional partitioning, some building blocks were identified and developed. Each building block would be available for the next higher level of integration. The different levels of building blocks are shown in Figure I-2. Products exist at all levels for use on multiple missions. The lowest level is the intellectual property level of library cells, and software code. A level above that is at the ASIC or module level where the complete part can be used in a function. The next level is the board level where the size of the board and overall functionality can be used depending on the packaging requirements of the mission. For example a probe might require custom packaging in order to reduce the overall system mass. Use at the assembly level will bring the most benefit to the mission by reducing cost and risk.

Intellectual Property Level
* ASIC Library
* Verilog Code
* Firmware Code
* Power Control Algorithm
* Power System Architecture

ASIC and Module Level Components
* SCAH
* SCAL
* PWMA
* CIA
* AIA
* PASM

Slice Level Components
* Power Control Slice (PCS)
* Power Switch Slice (PSS)
* Dual Converter Slice (DCS)

Subsystem Level
* Power System Electronics (PSE)
* Power Control
* Power Distribution
* Valve Drive Electronics
* Pyro Drive Electronics
* Power Conversion

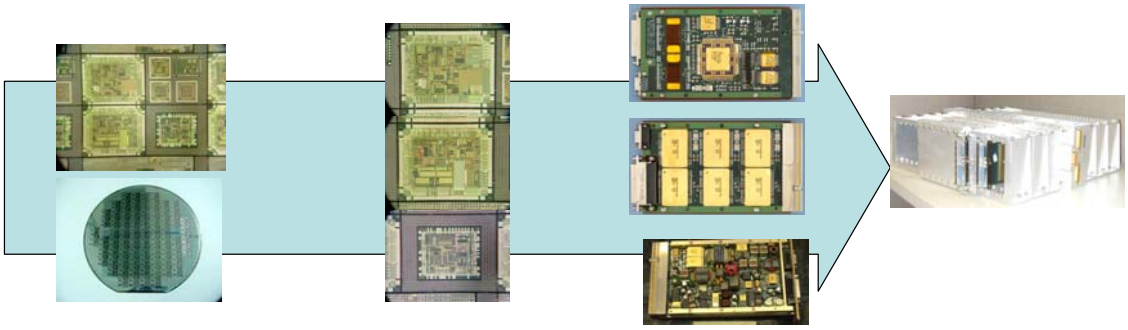

Figure I-2: X2000 PSE Development Approach

II. Power Distribution

The power distribution function provides the spacecraft electrical load switching, pyro firing, and valve actuation. The implementation of power distribution is accomplished by using a board level building block approach. The board is defined as the power switch slice and can be configured in the backplane to provide the standard load switching, or safety critical pyro firing and valve actuation. The power switch slice is a compactPCI 3U form factor circuit board (Figure II-1).

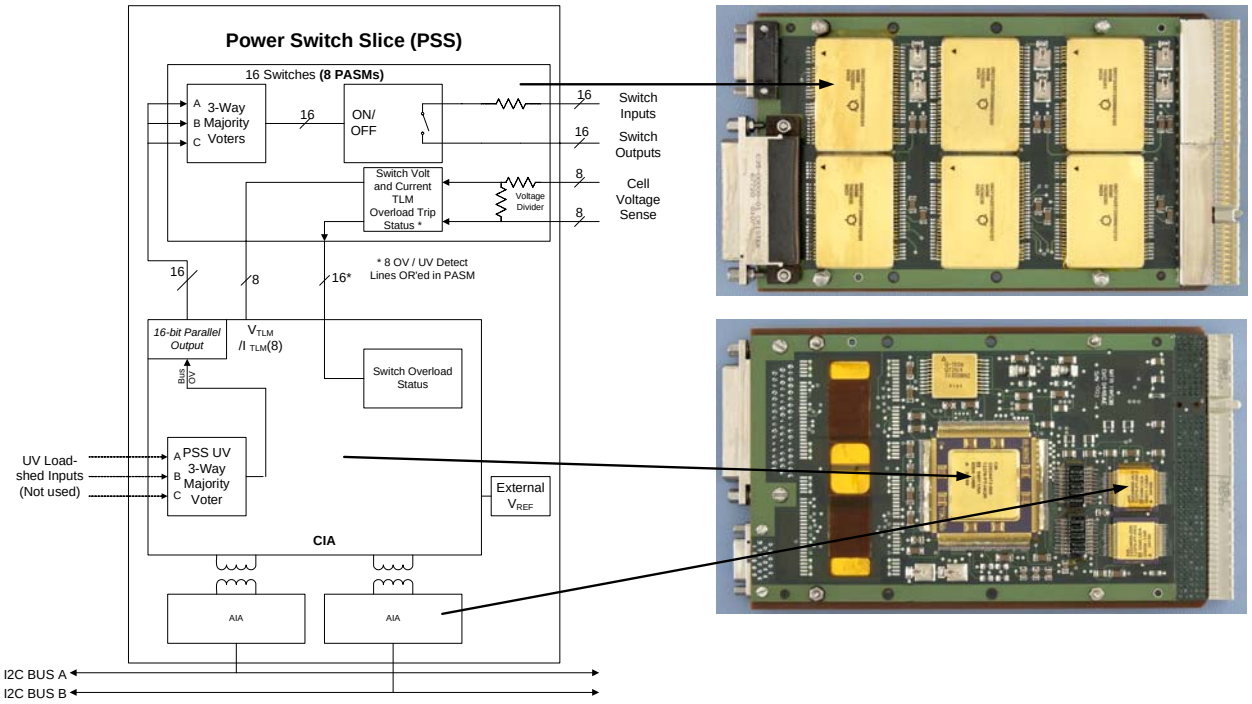

Figure II-1: PSS Functional Block Diagram and picture of CompactPCI 3U board

A. Power Actuation and Switching Module (PASM)

The PASM is a solid-state, general-purpose switching module. Each PASM has two independent MOSFET power switches that can be used in various configurations. These switches can be used in a series or parallel configuration and as high-side or low-side connection to the load, thus, providing greater flexibility to the system architect when designing the power system. Some of the key features of the PASM are over-current trip, current limiting, soft start (closed-loop di/dt control), switch current and voltage telemetry, and back-EMF suppression for inductive loads. The PASM is capable of driving regular loads (e.g., heaters, traveling-wave tube amplifiers, spacecraft computers), pyro devices, and inductive loads (thruster valves, motors).

B. Analog Interface ASIC (AIA)

The AIA provides power-return isolation between the data buses and the power system electronics. The AIA receives and transmits commands to the CIA via two I^2C transceivers. Figure III-2 exhibits the block diagram of the Command Interface. Transformers are used to isolate the signals between the AIA and the CIA. An internal 6.29 MHz clock is designed on chip with the capability of interfacing with an optional external clock. An on-chip oscillator watchdog forces the AIA into a fail-silent mode in the event of an oscillator failure. This chip is powered by redundant 3.3V power sources. A power-on-reset signal must be provided by an external source such as a power converter. Like the SCA, it is fabricated on the Honeywell HX2000 process, which makes the chip 1Mrad hard. The first ASICs were produced June 2003. Prototype ASICs were packaged and have been tested individually and with the Command Interface ASIC. The AIA passed all functional verification tests.

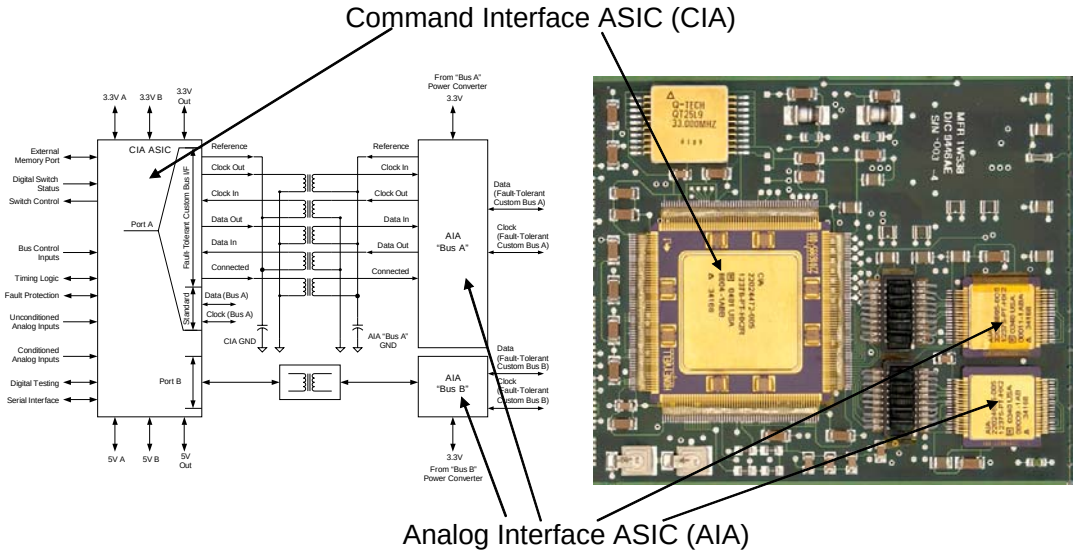

Figure II-2: Command Interface Building Block

C. Command Interface ASIC (CIA)

The CIA is a micro-controller that is based on a M8051 core processor with multi-frequency operation[2]. The CIA has been fabricated on the Honeywell HX3000 0.3µm, SOI process line. The CIA has two modes of operation, one at 16.5 MHz and another at 8.25 MHz. In addition it has a sleep mode for low power consumption. It can interface with the spacecraft computer via an I^2C standard data bus. The design provides two I^2C ports, which allow communication on primary and redundant data busses. There is 8KB and 12KB of program and data memory respectively available on chip. The CIA also has the capability to boot up from an external ROM and store data to a larger external memory device. The external ROM feature allows user specific programming of the micro-controller. The chip can be powered by two 5.0V sources for the analog circuitry and two 3.3V sources for the digital circuitry. Both voltages are then cross-strapped internally for redundancy. At least one of each voltage is

needed for proper CIA functionality. Internal power-on-reset (POR) circuits are also designed to hold the circuit in a known state during initial power on and power cycling. The CIA is designed to work with the other building blocks of the power system, and as such contains a multiplexed 8-bit analog–to-digital converter, which processes the analog telemetry from the PASM. The CIA has the ability to measure bus voltage and current directly across an external resistor network and report this telemetry on the I^2C bus. An internal watchdog timer in the design forces a fail silent state on the I^2C bus in the event of a failure.

Prototype versions of the AIA and CIA have been tested at JPL. Functionality of each block of has been targeted by a series of tests. All blocks have successfully passed performance testing at ambient temperature. A simulated spacecraft computer was used to send I^2C commands and receive telemetry back from the test card containing two AIAs and one CIA. Each time the automated test is run approximately 2.3 million I^2C commands are sent and a telemetry status response is received for each command. Tests were run using primary and redundant I^2C busses; all commands resulted in the expected telemetry and power-switch status indication. The fail-silent and power cross-strap functions of both ASICs performed as expected.

III. PASM Description

The PASM provides current limit and trip capability, and current and voltage telemetry. It provides soft start of capacitive loads, and permits clamped reverse-voltage turnoff of inductive loads. Figure III-1 shows the PASM block diagram. Each PASM has two independent identical isolated solid-state switches that can be connected to the load in a variety of series, parallel, or bi-directional configurations. Figure III-2 shows how a PASM switch can be connected in either the supply line (high-side) or return line (low-side), relative to the load. PASM switches provide a great deal of flexibility in system architecture. The PASM can replace most fuses and relays, resulting in greater system reliability. If current exceeds the trip value for about 20 ms, the PASM switch gracefully turns off the load within 31 ms. Fault (or overload) current is actively limited to a maximum of 6.5 A within 100 µs. The nominal current trip and limit capability of each PASM switch is 3.7 A and 5.75 A respectively. By simply jumping two pins, the user can select a set of lower current trip and limit values; namely, 1.5 A and 2.25 A, respectively. Once tripped a switch latches off until it is reset by either recycling the ASIC power or by commanding the switch OFF and then ON again. In addition telemetry of the overload trip status is available.

PASM switches are designed to limit inrush current during turnon, and to limit inductive kickback voltage during turnoff. The rate of current change, di/dt, is actively controlled at a nominal value of 7.5 A/ms during turnon and turnoff. The controlled di/dt feature can be disabled by the user for inductive load applications to provide quick turnon and turnoff response. Inductive kickback voltage during turnoff is limited by passive components that operate the MOSFET switch as a power Zener, thus dissipating the transient energy in a device that is rated to handle power.

Each MOSFET switch in a PASM is controlled by a pair of Switch Control ASICs (SCAs), as shown in the block diagram of Fig. 3. The Low-Side SCA receives commands, a clock, and housekeeping power, and it transmits telemetry; so it is referenced to the power-system ground. The High-Side SCA monitors and limits switch current, so it floats with the switch and is referenced to the switch output voltage, which can be up to 40 V above power-system ground. Two separate ASICs are necessary because the Silicon On Insulator (SOI) breakdown voltage is inadequate to provide the required voltage level shifting in a single ASIC.

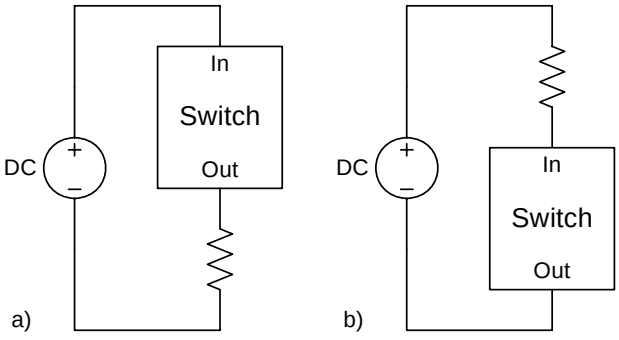

Figure III-1. PASM switches can be connected as either (a) High-Side, or (b) Low-Side, relative to the load.

It is desirable in some applications (e.g., driving propulsion valves) to extinguish inductive load current quickly when the load switch is opened. PASM switches are designed to apply a negative voltage to inductive loads during turnoff, to reduce inductor current decay time. This is achieved using diodes to bias the power MOSFET at a voltage that is larger than the input voltage. The inductive energy is absorbed in the power MOSFET - that is rated to handle power - rather than in the clamping diodes. The clamping diode network is effective for both high- and low-side switches.

IV. Design Approach

The chipset is powered by redundant 5 V power supplies that feed the Low-Side SCA. Foldback current limiting in the Low-Side SCA protects the power supplies from ASIC faults or overloads. Power-on-Reset (POR) circuitry was designed to keep the circuit in a known state during initial power-on and in the event of power loss. On-chip voltage references are provided in both ASICs. The chipset provides analog telemetry of switch current and voltage. Logic command inputs are compatible with both 3.3 V and 5.0 V standard CMOS logic. Currently the chipset is designed to drive a 100 V MOSFET for use in most lower-voltage applications. However, with adequate isolation between the interfaces of the two chips it can be used also in higher voltage applications.

Bias power for the High-Side SCA is developed from the Low-Side SCA. After consideration of alternative approaches, a two-phase charge pump was selected for powering the High-Side SCA. It is low-profile, reasonably efficient, and is implemented on-chip with the exception of two small chip capacitors. The charge pump supplies a full-bridge synchronous rectifier, in parallel with a voltage tripler, in the High-Side SCA to produce 5 V and 12 V bias power.

A novel low-power interface technique was developed to couple commands and telemetry between the Low- and High-Side SCAs. This interface scheme uses series capacitors to couple clock signals from the sending side to the receiving side of the interface. These capacitors are built into the ASICs using interconnected metal layers to form parallel plates. There are two channels for each command and status signal; the clock is gated into one channel for Logic High and to the other channel for Logic Low.

PASM analog telemetry is controlled by two digital commands. One command selects either switch current or switch voltage; the other either enables or inhibits output of PASM analog telemetry.

For telemetry of switch current, which is sensed in the High-Side SCA and telemetered in the Low-Side SCA, a pulse-position scheme was developed. When a periodic ramp signal crosses the switch-current sense signal, a pulse is transmitted through a series coupling capacitor from High-Side SCA to Low-Side SCA, which triggers a circuit to sample and hold the value of a slave ramp signal in the Low-Side SCA. The sampled and held value of switch current is buffered and fed to the telemetry output multiplexer.

For telemetry of switch output voltage, the voltage is fed directly to the Low-Side SCA, where it is scaled, buffered, and fed to the other input of the telemetry output multiplexer.

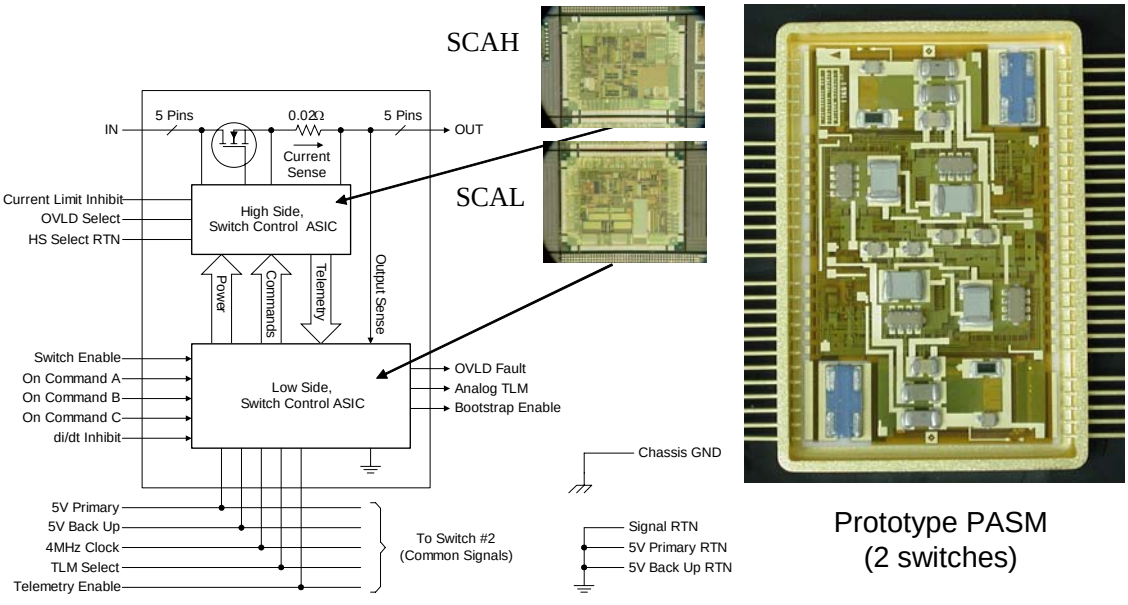

Figure IV-1: Switch Control ASICs and PASM Building Blocks

V. Physical Description

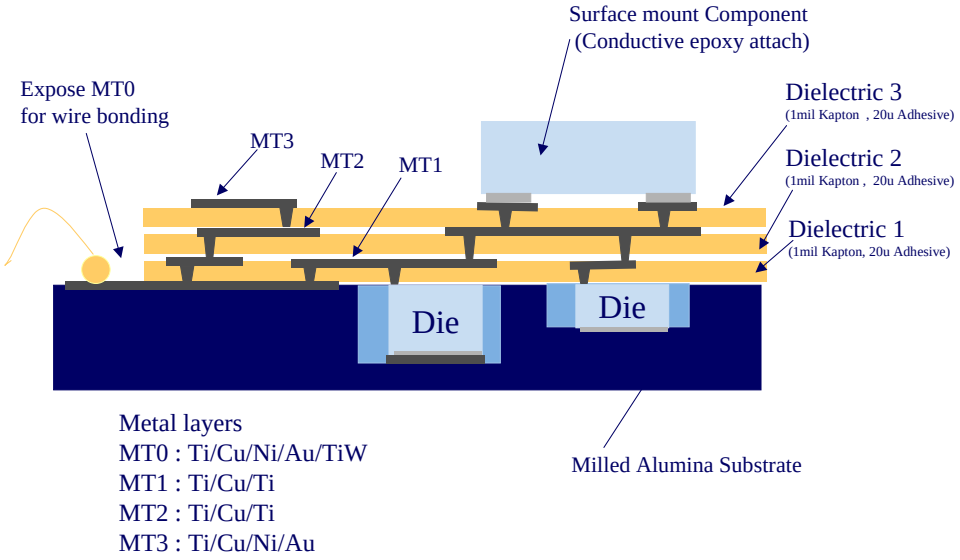

Figure V-1: HDI cross-section

JPL's industry partner, Lockheed Martin – Commercial Space Systems (Newtown, PA), is designing the PASM. The PASM package design is based on a new Power High-Density Interconnect (Power HDI) technique developed by General Electric. As shown in Fig. V-2, the HDI cross-section looks somewhat like a multilayer PCB, but it has smaller dimensions, which translates to higher power density and enhanced high-frequency performance. Discrete components can be placed on top or mounted in recessed cavities within the substrate, much like parts can be mounted on both sides of a PCB.

Figure V-3 shows the PASM in a packaged HDI assembly. The package contains two switches, where each switch includes a power MOSFET, its associated SCA chipset, and other related components. The layout of one switch was designed, and then copied and simply rotated around the vertical centerline for the other switch.

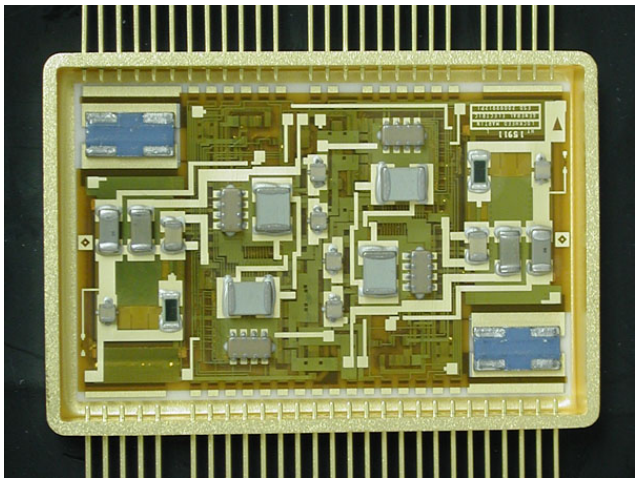

Figure V-2. PASM in HDI package.

VI. Test Results

The SCA chipset is fabricated using the Honeywell 0.8 µm Silicon-on-Insulator (SOI) HX2000 process and the first ASICs were completed in June 2003. Some of these ASICs were packaged as separate discrete parts to facilitate breadboard testing. In spite of increased parasitic loading and coupling, which attenuates interface signals and increases noise in comparison to the intended HDI package, these packages provided useful test results, which motivated us to take the next step and build and test some PASM prototypes in the HDI package format. Based on the test results of the first set of PASM prototypes, we found some noise coupling in adjacent signals on the SCA interface with the MOSFETs. We also discovered a safe operating area problem with latest generation MOSFET.

We decided to make some changes to the SCA on a second pass and use the previous generation MOSFET. The test results of the second pass SCA and PASM prototypes are shown below.

Figure VI-1 shows a PASM switch turning on into an overload. During turnon, current ramps up at a controlled rate designed to reduce noise, following an internal ramp signal. Without switch intervention current would rise to Vin/R = 40/4.7 = 8.5 A; however, the switch does intervene and limits current at 5.75 A. The switch will turn OFF automatically if current exceeds the default 3.7 A trip level for a time between 15 ms and 31 ms. In this test the switch was commanded OFF before the overload timer triggered turnoff. During turnoff the current ramps down, again at a controlled rate.

Figure VI-2 shows a PASM switch turning on a highly capacitive load. Spacecraft loads frequently have filter

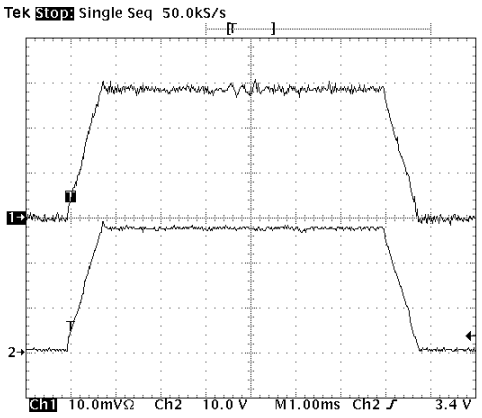

Figure VI-1. Turn ON, limiting current, and turn OFF of 4.7 Ω resistive overload; (1) load current, 2 A/Div, (2) load voltage, 10 V/Div.

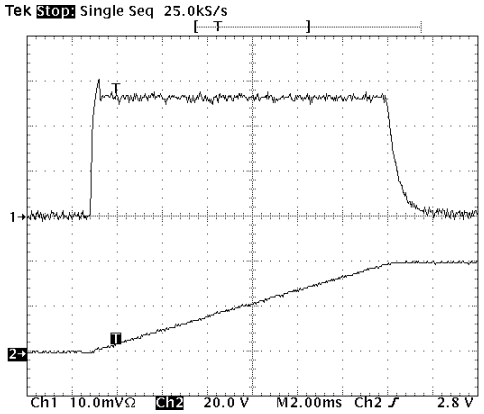

Figure VI-2: Turn ON of 1800 µF capacitive load in parallel with 1000

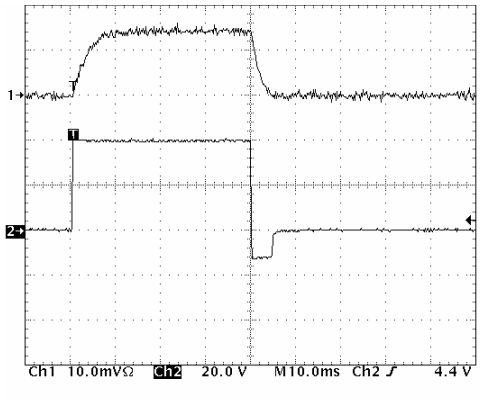

Figure VI-3: Turn ON/OFF of 25 mH inductive load in series with 13.4 Ω

capacitors that are initially uncharged when they are turned on. In this case the load voltage barely changes as switch current ramps up. The switch once again limits load current, and the load capacitor continues to charge. When the load voltage reaches the input voltage, current drops down to the steady-state resistive component.

Figure VI-3 shows a PASM switch turning ON, holding, and turning OFF an inductive load. As seen here the controlled di/dt feature has been disabled for inductive load applications to provide quick turnon and turnoff response. At turnon, the switch applies the full input voltage to the load, and load current rises exponentially to the steady-state value. At turnoff the load voltage is clamped at a negative value, which reduces the current decay time. When load current reaches zero, the load voltage also goes to zero.

VII. Summary

Development of the PASM switch module for power distribution functions in space environments has been described. Each PASM contains two independent switches, along with custom mixed-signal Switch Control ASICs and a few discrete support components. This compact and versatile component can switch low- or high-side loads. It can control current inrush during turnon, and limit voltage during turnoff. It continuously monitors load current, and it will automatically disconnect overloads and faults that persist for 20 ms, while limiting current in the interim. Those features provide PASM switches with the capability to fire pyrotechnic initiators, control propulsion valves, and distribute power to spacecraft loads.

The PASM is designed for flexibility, and can be configured using jumper connections to select reduced current trip and limit levels, or even to inhibit current limit. It has three majority-voted ON/OFF command inputs. Additional inputs for configuration and operation include signals to select telemetry options and to disable the

switch in safety-critical applications (e.g., pyrotechnic initiation) until appropriate arming and firing conditions are met. Telemetry outputs include overload status and analog switch voltage and current. The second phase of PASM prototype testing has been complete verifying the functionality.

Acknowledgments

This work was performed at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

References

[1] Jones, L., Carr, G., Deligiannis, F., Lam, B., and Wester, G., "New Generation Power System for Space Applications," *2nd AIAA International Energy Conversion Engineering Conference*, Providence RI, 16-19 Aug 2004, Paper Number: AIAA-2004-5538.

[2] Ruiz, I., "Open-Systems Architecture of a Standardized Command Interface Chip-Set for Spacecraft Power Switching and Control," *2nd AIAA International Energy Conversion Engineering Conference*, Providence RI, 16-19 Aug 2004, Paper Number: AIAA-2004-5691.