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# Single Event Effects Test Results for Advanced Field Programmable Gate Arrays

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**Abstract**—Reconfigurable Field Programmable Gate Arrays (FPGAs) from Altera and Actel and an FPGA-based quick-turn Application Specific Integrated Circuit (ASIC) from Altera were subjected to single-event testing using heavy ions. Both Altera devices (Stratix II and HardCopy II) exhibited a low latchup threshold (below an LET of 3 MeV-cm<sup>2</sup>/mg) and thus are not recommended for applications in the space radiation environment. The flash-based Actel ProASIC Plus device did not exhibit latchup to an effective LET of 75 MeV-cm<sup>2</sup>/mg at room temperature. In addition, these tests did not show flash cell charge loss (upset) or retention damage. Upset characterization of the design-level flip-flops yielded an LET threshold below 10 MeV-cm<sup>2</sup>/mg and a high LET cross section of about 1x10<sup>-6</sup> cm<sup>2</sup>/bit for storing ones and about 1x10<sup>-7</sup> cm<sup>2</sup>/bit for storing zeros. Thus, the ProASIC device may be suitable for critical flight applications with appropriate triple modular redundancy mitigation techniques.

**Index Terms**—Field Programmable Gate Arrays, ASICs, Single Event Latchup, Single Event Upset.

## I. INTRODUCTION

THE prospect of using reprogrammable devices in space is one that appeals to many designers due to lower development cost (compared to one time programmable FPGAs) and the ability to reconfigure or adapt a design at all stages of a mission. Re-configurability comes at a cost of upset mitigation due to the intrinsically “soft” nature of many of these devices. The three primary vendors of FPGAs are Actel, Altera, and Xilinx. Much work has been done to investigate Single Event Effects (SEE) and SEE mitigation techniques of the Xilinx SRAM-based FPGAs (Virtex-II family) [1], [7]. Altera’s SRAM-based FPGAs (Stratix family) have been tested and thus far proven to be extremely sensitive to latchup

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[2]. These experiments evaluate an advanced Actel FPGA for applications in space as well as a device from Altera’s current generation Stratix II for latchup characteristics. In addition, an Altera HardCopy II ASIC was tested for single-event latchup.

## II. DEVICE CHARACTERISTICS

### A) Actel ProASIC Plus

The Actel ProASIC family differs functionally from its counterparts by the fact that, rather than using SRAM configuration cells, it is a flash-based, non-volatile device, therefore not requiring external boot-up PROMs to support the device’s configuration. A single flash switch consists of a pair of transistors that share a floating gate that stores the program bit. The first transistor writes and verifies the floating gate voltage, and the second is the switching transistor. Flash memory cells are used for routing and assigning and logic values. Also, one can clear the design by erasing the flash cells by removing the charge stored by the floating gates.

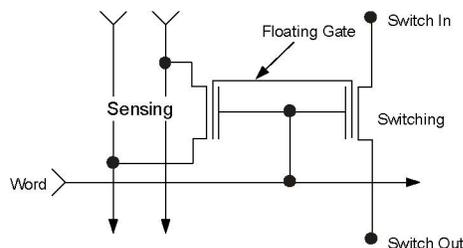


Fig. 1. Schematic representation of the Flash Switch Architecture of the ProASIC Plus device from Ref. [4].

The irradiated Actel DUT APA300-PQ208, date coded 0505 from a UMC foundry, consisted of 300,000 system gates with 290 user I/O’s, and 32 embedded block RAMs (each consisting of 72k-Bits). The DUT can be broken down into 8,192 tiles (registers) which can be configured as a flip-flop, latch, or a three input/one output logic device. The device operates with a 2.5V core voltage, with a 0.22 $\mu$ m feature size and supports either 2.5V or 3.3V I/O voltages.

### B) Altera Stratix II

The Altera Stratix II is a 1.2V core, 90nm, SRAM based FPGA. The device structure is a two-dimensional row- and column-based architecture that provides signal interconnections between logic array blocks (LABs), memory structures, and DSP blocks. The LABs consist of eight adaptive logic modules (ALMs), which implements user logic. In addition, I/O blocks provide the interface from package

pins to the internal signals. Re-configurability is established by programming the internal memory SRAM cells which determine the interconnects and logic functions of the FPGA.

The irradiated EP2S60F1020C4 consists of 48,352 logic elements (ALMs), 2,544,192 total user ram bits, 36 DSP blocks, 144 embedded multipliers, 8 phase-locked loops, and 718 user I/O's.

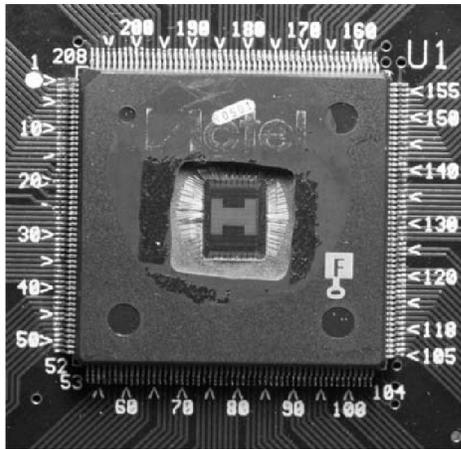
### C) Altera HardCopy II

The Altera HardCopy II is an ASIC that leverages development and verification from the FPGA-counterpart software toolset and is pin-compatible to the Stratix II. Development is intended to be performed with a Stratix II device, followed by integration to the HardCopy II. The particular device tested here is the HC220-TC1 which includes 1.6M ASIC gates, 3 million total ram bits, 4 phase-locked loops, and comes in a 672-pin FPGA package. The FPGAs for prototyping designs intended for this part are the EP2S60, EP2S90, and EP2S130.

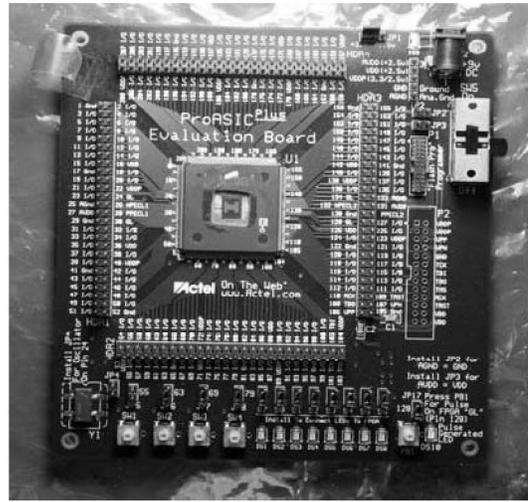
## III. HARDWARE PREPARATION

### A) Actel ProASIC Plus

Actel ProASIC Plus Evaluation Boards were used for development and testing. The test design filled the device with four serial shift registers in order to observe upsets. To exercise and provide visibility on the DUT board, a custom Service Board was developed. It provides the DUT with various desired patterns (ones, zeros, and checkerboard) as well as the master shift register clock; in addition, the Service Board detects and records upsets. The use of this board limited the speed that we could clock the shift register and detect errors to a few hundred kHz, but the SEU and SEL characteristics of this device are likely to be frequency independent. Terminating resistors were used on the signals for signal integrity, which are used to help reduce reflections. Three APA300s were de-lidded by the use of an acid etching machine and soldered to three development boards, as shown in figure 2.



(a)



(b)

Fig. 2. (a) A close-up of the de-lidded APA300-PQ208 DUT and with die exposed. (b) The ProASIC Plus Evaluation Board used for testing.

### B) Altera Stratix II

Altera DSP evaluation boards, board number DSP-DEVKIT-2S60, were used for development and testing. A similar FPGA design to that of the Actel test was used in order to verify functionality and, if no latchup had occurred, record upsets. In a similar manner, a Service board was used to provide shift register patterns, clock and reset, and to detect upsets. The Stratix II parts are in flip-chip packages, so three devices were de-lidded and the silicon back-side thinned to approximately 50 $\mu$ m so that the incident beams could penetrate to the active region. The devices were sent along with the development board to an assembly house to have the original parts removed and the thinned parts mounted, as shown in figure 3. The DSP-DEVKIT-2S60 DUT boards were modified so that the regulators were not used and individual biases could be applied and monitored by external laboratory supplies.

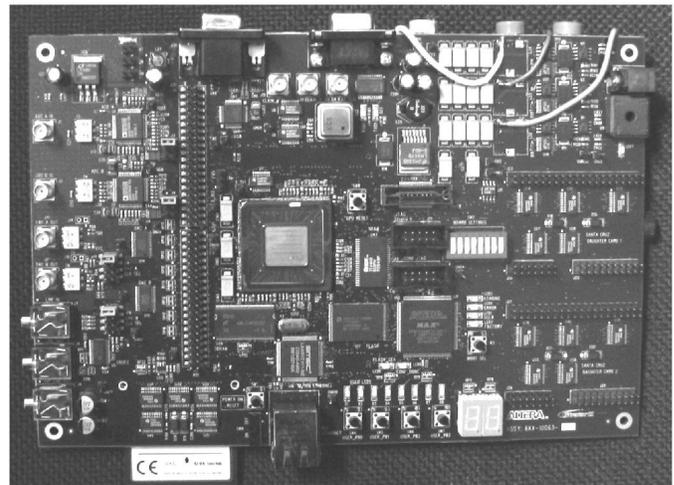


Fig. 3. The DSP-DEVKIT-2S60 evaluation board used for testing with the thinned EP2S60F1020C4 DUT in the center. The three added wires in the upper right are part of the biasing modifications.

### C) Altera HardCopy II

For this work, Altera supplied several HardCopy II DUTs containing a large functional design that exercised the various components of the part. Because latchup was the primary focus of this study, most of these functions were not clocked or observed. Custom boards were built to bias the part and real-time strip charts of the DUT currents and voltages were captured during the irradiations. Functionality of the DUT's JTAG capability was checked between irradiations.

## IV. SOFTWARE DEVELOPMENT

The VHDL developed for each of these tests was relatively straightforward. The Actel design consists of four 1023-bit shift registers with a built in synchronous reset. The reset signal was fanned out to every flip-flop in each shift register and when asserted sets all the flip-flops output to logic one. The clock was also fanned out to every flip-flop of every shift register in the design. Actel's IDE implemented the code and developed a shift register that consisted of a series of alternating reset logic followed by flip-flops (as seen in figure four). As previously noted, the APA300 consists of 8192 register tiles, 8184 of which were used in the design.

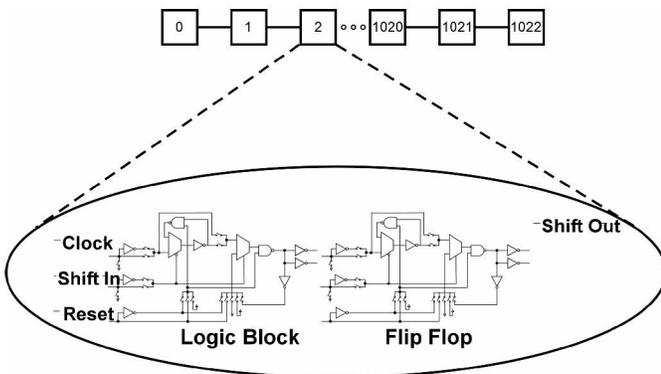


Fig. 4. Detection strategy for single events in the Actel test setup; one tile is used for the reset logic, and the second the register.

Similarly, the Altera design consisted of four 2048-bit shift registers with synchronous reset. The design used 4,096 ALMs, 16% of the total available.

## V. TEST SETUP AND PROCEDURE

### A) ProASIC Plus and Stratix II

The test setup for both experiments is shown in figure five. A laptop was used in conjunction with a GPIB interface to control a four channel programmable power supply. The voltage regulators on the board were bypassed in order to monitor and control voltages and currents manually. A custom Visual Basic program was used to control voltages and currents as well as to monitor SEL. A current limit was set to detect SEL via the custom software. Nominal voltages were supplied to the DUT. A Function Generator was used to supply the Service Board with a square wave to serve as the

design's clock in the case of the Actel test. The clock was generated on the Service Board in the case of the Altera test. The Service Board compared the shifted pattern out with the signal that was being shifted in, and sent error pulses out a 40-pin ribbon cable via receiver/driver cards to a custom-built counter board. The counter board separately counted the errors in each shift register and sends them to the functional monitor laptop where the errors are recorded and displayed in a strip chart of the accumulating errors using a Visual Basic interface program.

The Visual Basic program, in conjunction with the counter board, also allows the experimenter to control what pattern is being sent into the shift register by way of the Service Board.

A set protocol was followed during the test after each beam run to verify correct functionality of the DUT and support apparatus. Power was cycled between irradiations.

### B) HardCopy II

For the HardCopy II testing, only the power supply control and SEL monitor was needed. As in the other tests, a laptop running a custom Visual Basic program controls a primary power supply that supplied and monitored power, as well as controlled the enabling of a secondary power supply. A current limit was set to detect SEL via the custom software. Nominal voltages of 1.2V on the core, and IO voltages of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V were supplied to the DUT.

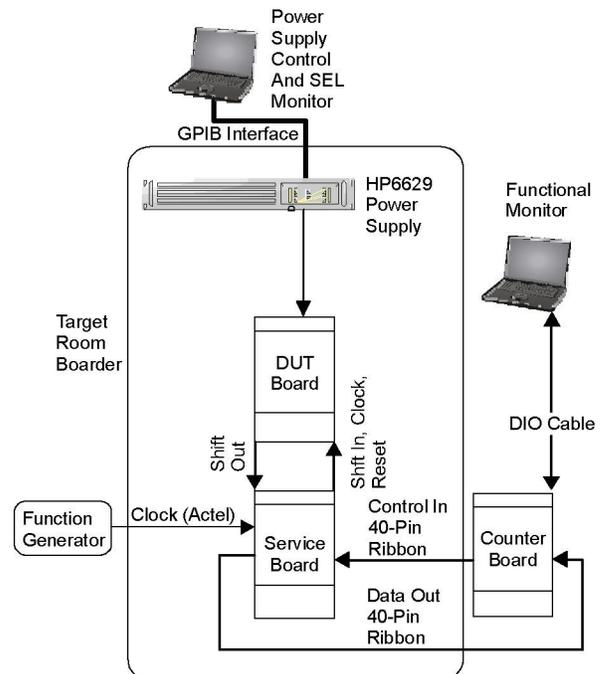


Fig. 5. Test Setup for both the Actel and Altera tests. For the Altera test, the function generator was not used as the clock was generated on the service board. Also, two HP6629's were used to power the Altera test.

## VI. TEST RESULTS AND BEHAVIORAL OBSERVATIONS

### A) Actel ProASIC Plus

The goal of this test was to characterize the behavior of the ProASIC Plus in the beam. Possible SEE modes that the behavior and data were being analyzed for were: latchup, upsets, and “stuck bit” behavior. All test runs were done at room temperature in air with nominal voltages of 2.5V for the core, with  $V_{DDA}$  at 2.5V and  $V_{DDP}$  at 3.3V. Current limits for latchup detection were set to 200mA for the core and I/O. No latchup events were observed with an effective LET of 75.0 MeV-cm<sup>2</sup>/mg and a total fluence of  $1 \times 10^7$  particles/cm<sup>2</sup>. Upsets were observed, recorded, and compiled in table II. The data is plotted in figures 6 and 7 where they are fitted with Edmonds and Weibull functions, respectively. Including the post irradiation pattern cycling protocol, other post-beam analysis was done to verify that there was no catastrophic damage to the DUT, and no such damage was observed. In a test of this nature, SETs would be hard to single out, and if they did occur and were observable, they would appear within the upset data collected. It is unlikely that many SETs were recorded with this particular test setup because they must be clocked into the design and this design was running at a relatively slow rate.

An unusual behavior occurred during a single test run when using the checkerboard pattern. Upsets accumulated gradually consistently with previous runs, then for a brief period the errors incremented in bursts of approximately 1023 upsets per read cycle (there are 32 read cycles per second). This behavior persisted for approximately six seconds, after which the errors accumulated at the expected, slower rate. This behavior began and ended in the first three shift register chains simultaneously, but the fourth chain remained unaffected. This behavior can most likely be attributed to an upset induced timing error, for example, a beam induced extra or missing clock pulse.

TABLE I  
LIST OF THE IONS USED AT THE TAM ACTEL TEST

Ion	Energy (MeV)	Angle (Deg)	Degrader	LET (MeV-cm <sup>2</sup> /mg)
Ne <sup>20</sup>	300	0°	None	3.07
Ne <sup>20</sup>	300	50°	None	4.55
Ar <sup>40</sup>	599	0°	None	8.57
Ar <sup>40</sup>	599	50°	None	13.3
Ag <sup>109</sup>	1634	50°	None	67.8
Ag <sup>109</sup>	1634	50°	1 at 36.1°	75

TABLE II  
COMPILATION OF REGISTER UPSET DATA ACQUIRED FOR THE ACTEL PROASIC PLUS

Effective LET (MeV-cm <sup>2</sup> /mg)	Total Effective Fluence (particles/cm <sup>2</sup> )	Total Errors	Pattern
75.0	1.00E+07	37554	Ones
67.8	2.03E+05	75	Zeros
67.8	1.00E+05	316	Ones
13.3	1.00E+07	396	Zeros
13.3	9.96E+06	3827	Ones
8.57	1.04E+07	383	Zeros
8.57	9.84E+06	2301	Ones
4.55	2.00E+07	18	Zeros
4.55	2.11E+07	127	Ones
3.07	2.00E+07	15	Zeros
3.07	2.00E+07	67	Ones

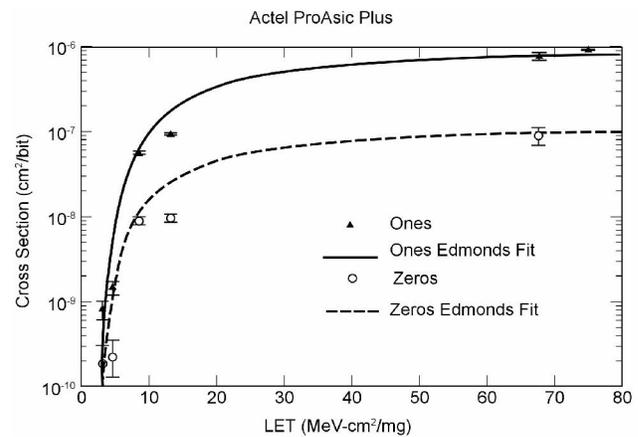


Fig. 6. Cross Section vs. LET for 0 → 1 upsets (zeros) and for 1 → 0 upsets (ones). Cross Sections fit with Edmonds equation [8]; see Table III for fitting parameters.

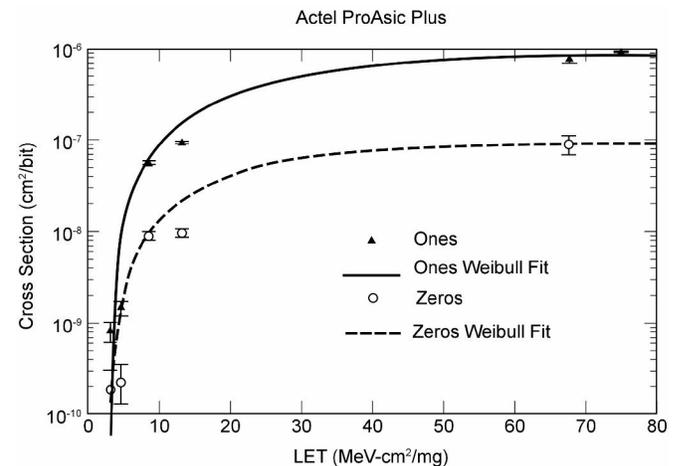


Fig. 7. Cross Section vs. LET for 0 → 1 upsets (zeros) and for 1 → 0 upsets (ones). Cross Sections with a four parameter Weibull fit; see Table III for fitting parameters.

TABLE III  
LIST OF FITTING PARAMETERS  
FOR ACTEL CROSS SECTIONS

Parameters Data Pattern	Edmonds		Weibull			
	$L_{1/e}$	$\sigma_{sat}$ MeV-cm <sup>2</sup> /mg	Limit cm <sup>2</sup>	Onset MeV-cm <sup>2</sup> /mg	Width	Power
Ones	24	1.10E-06	8.34E-07	3.00	28.0	1.60
Zeros	21	1.30E-07	9.00E-08	2.99	23.6	1.50

### B) Altera Stratix II and HardCopy II

The previous Altera family of FPGAs (Stratix) has been shown to exhibit single-event latchup [2] with a cross section of  $6 \times 10^{-7}$  cm<sup>2</sup> at an LET of 2.8 MeV-cm<sup>2</sup>/mg. The goal of this test was to determine latchup behavior, if any, of the Stratix II and HardCopy II. A secondary goal, if latchup was not a prevalent behavior, was to collect upset data. All tests were done at the operating temperature in vacuum with nominal voltages on the DUT. The current threshold for latchup detection was set to 750mA for the core on the Stratix II and to 1A on the HardCopy II.

Little part-to-part variation is seen from the limited data set of Ref. 2. There was little noticeable scaling trend seen between the Stratix as tested by Sanders et. al. [2], and the Stratix II devices. This fact, along with the relatively high cross section at high LET and the very low threshold LET suggests that scaling alone will not soon eliminate SEL susceptibility.

TABLE IV  
LIST OF THE IONS USED AT BERKELEY ALTERA TEST

Ion	Energy (MeV)	Angle (Deg)	LET (MeV-cm <sup>2</sup> /mg)
Xe <sup>38</sup>	1403	0°	58.72
Kr <sup>24</sup>	886	0°	31.28
Cu <sup>18</sup>	659	0°	21.33
Ar <sup>11</sup>	400	0°	9.74
Ne <sup>6</sup>	216	0°	3.45
O <sup>5</sup>	184	0°	2.22
B <sup>3</sup>	108.2	0°	0.87

TABLE V  
COMPILATION OF LATCHUP EVENTS ACQUIRED FOR THE ALTERA STRATIX II AND HARDCOPY II

Device	Effective LET (MeV-cm <sup>2</sup> /mg)	Total Fluence (particles/cm <sup>2</sup> )	SEL
Stratix II	58.72	4.09E+03	53
	31.28	1.25E+04	28
	21.33	1.00E+04	22
	9.74	1.25E+06	48
	3.45	1.00E+07	9
	2.22	1.00E+08	23
	0.87	1.00E+08	2
HardCopy II	3.45	2.10E+08	34

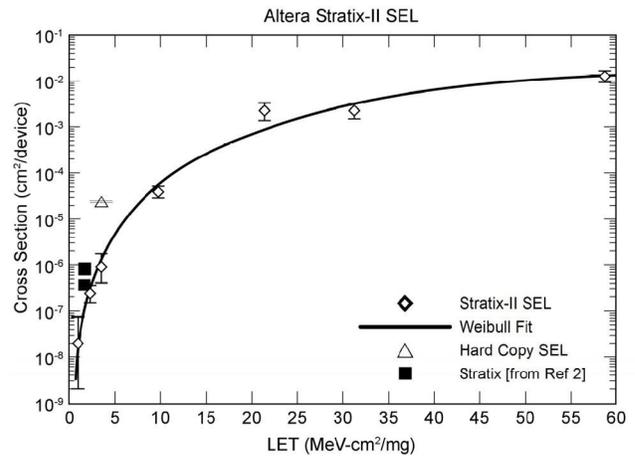


Fig. 8. Cross Section vs. LET for Altera Stratix II SEL. The four parameter Weibull fit is shown; see Table VI for fitting parameters. Two Stratix devices were tested by Sanders et. al. from Ref. 2 and are shown above.

TABLE VI  
LIST OF FITTING PARAMETERS FOR ALTERA STRATIX II CROSS SECTIONS

Weibull Parameters			
Limit (cm <sup>2</sup> )	Onset (MeV-cm <sup>2</sup> /mg)	Width	Power
1.80E-02	0.20	46.8	1.60

## VII. CONCLUSIONS

Unlike a device from the ProASIC family of Actel flash-based FPGAs [9], the ProASIC Plus device tested was not found to be sensitive to latchup at room temperature. For register upsets, the LET threshold is approximately 5 MeV-cm<sup>2</sup>/mg, with a saturation cross section of about 10<sup>-6</sup> cm<sup>2</sup>/bit. Appropriate application of design-level Triple Modular Redundancy (TMR) may be needed to mitigate upsets for critical space applications. Another important test would include irradiating while the device is programming to detect SEGR or other related phenomena, as suggested by [3]. For this test, no evidence of flash configuration cell charge loss, gate rupture, or other catastrophic events were seen. Additional tests are needed to measure the upset susceptibility of the embedded block RAMS, user I/O's, and PLL's, in addition to possible mitigation techniques of those components.

The Altera Stratix II and HardCopy II exhibited single event latchup. The onset LET for latchup was less than 1 MeV-cm<sup>2</sup>/mg for the Stratix II (and likely for the HardCopy II as well) with a saturated cross section of about 10<sup>-2</sup> cm<sup>2</sup>/device for the Stratix II device.

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