

Reconfiguration of Analog Electronics for Extreme Environments: Problem or Solution?

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Abstract

This paper argues in favor of adaptive reconfiguration as a technique to expand the operational envelope of analog electronics for extreme environments (EE). In addition to hardening-by-process and hardening-by-design, "hardening-by-reconfiguration", when applicable, could be used to mitigate drifts, degradation, or damage on electronic devices (chips) in EE, by using re-configurable devices and an adaptive self-reconfiguration of their circuit topology. Conventional circuit design exploits device characteristics within a certain temperature/radiation range; when that is exceeded, the circuit function degrades. On a reconfigurable device, although component parameters change in EE, as long as devices still operate, albeit degraded, a new circuit design, suitable for new parameter values, may be mapped into the reconfigurable structure to recover the initial circuit function. Partly degraded resources are still used, while completely damaged resources are bypassed. Designs suitable for various environmental conditions can be determined prior to operation or can be determined in-situ, by adaptive reconfiguration algorithms running on built-in digital controllers. Laboratory demonstrations of this technique were performed by JPL in several independent experiments in which bulk CMOS reconfigurable devices were exposed to, and degraded by, low temperatures (~-196°C), high temperatures (~300°C) or radiation (300kRad TID), and then recovered by adaptive reconfiguration using evolutionary search algorithms. Taking this technology from Technology Readiness Level (TRL) 3 to TRL 5 is the target of a current NASA project.

1. Introduction

Future NASA missions to Moon, Mars and Beyond [1] will face EE, including environments with large temperature swings, such as between -180°C and 120°C at the initial landing sites on the Moon, low temperatures of -220 °C to -230 °C during the polar/crater Moon missions, -180°C for Titan in-situ mission, -145°C and high radiation levels for Jupiter's Moons, 5MRad Total Ionizing Dose (TID) for Europa Surface and Subsurface mission, high temperature of 460 °C for Venus Surface Exploration and Sample Return mission, etc. EE induce drifts, degradation, or damage into electronic devices.

The current approach for space electronics designs is to use commercial/military range electronics protected through passive (insulation) or active thermal control, and high weight shielding for radiation reduction. This adds to sizable weight and volume, compounded by power loss, and additional cost for the mission. More importantly, as missions will target operations with smaller instruments/rovers and operations in areas without solar exposure, these approaches become infeasible. In many cases the electronics must be collocated with the sensor or actuator in the extreme environment, without the option of being insulated or shielded properly. Therefore, developing EE-electronics would have several advantages including lower costs, less power, and offering in some cases, the only reasonable solution.

Conventional approaches to Extreme Environment Electronics include *hardening-by-process* (HBP), i.e. fabricating devices using materials and device designs with higher tolerance to EE, (e.g using special materials like Silicon Carbide for high temperatures, or Silicon-on Insulator for radiation). Another promising approach is *hardening-by-design* (HBD), i.e. use of special design/compensation schemes. For example,

circuit techniques, such as auto-zero correction, are used to alleviate the problem of the (temperature dependent) offset voltages in Operational Transconductance Amplifiers (OTA) operated at low temperatures [1]. Both these hardening approaches are limited, in particular for analog electronics, by the fact that current designs are fixed and, as components are affected by EE, these drift, alter functionality.

A recent approach pioneered by JPL is to mitigate drifts, degradation, or damage on electronic devices in EE by using re-configurable devices and an adaptive self-reconfiguration of circuit topology. This new approach, referred here as **hardening-by-reconfiguration (HBR)** mitigates drifts, degradation, or damage on electronic devices in EE by using reconfigurable devices and an adaptive self-reconfiguration of circuit topology. ¹In HBR, although device parameters change in EE, while devices still operate (albeit on a different point of their characteristic) a new circuit design, suitable for new parameter values, is mapped into the reconfigurable system to recover the initial circuit functionality. Partly degraded resources are still used, while completely damaged resources are bypassed. The new designs, suitable for various environmental conditions, can be determined prior to operation or determined in-situ by reconfiguration algorithms running on a built-in digital controller.

HBR can also be seen as a related technique to HBD – with the characteristic that it uses an in-situ (re)design. HBR would benefit from HBD for the resources available on the reconfigurable chips. It would also work well in conjunction with HBP, contributing, as an extra layer of protection, to the expansion of the limits of operation in EE; HBP would provide inherent survivability to keep devices operational at higher EE limits, while HBR would provide the adaptation to changes in device characteristics needed for precise functions, specially needed for analog circuits. A somehow degenerated form of HBR would be the use on chip of several fixed circuits, each optimally designed for a temp range, circuits that can be multiplexed/switched in/out depending on the temp at that moment (this is different than mapping optimal designs on a reconfigurable array). A simple form of HBR would use a reconfigurable circuit, but circuit configuration for various extreme conditions would be predetermined and memorized for access when needed, as opposed to being determined in-situ, which is the harder, but potentially more powerful aspect of this technique.

This paper overviews the HBR technique and shows the results of experiments of recovery under radiation, and at low and high temperatures. The paper is structured as follows: Section 2 reviews the Evolvable Hardware approach. Section 3 describes the experiments. Section 4 outlines future work.

2. Evolvable Hardware

The rationale of the HBR approach is to mitigate drifts, degradation, or damage on electronic devices in extreme environments by using re-configurable devices and adaptive self-reconfiguration of the circuit topology. Automated reconfiguration of reconfigurable devices has been developed in the field of Evolvable Hardware. Evolvable Hardware is a set of techniques that address hardware that reconfigures under the control of evolutionary algorithms (the name is also used to refer to the hardware that evolves). Thus, evolvable hardware has two components: the Reconfigurable Hardware (RH) and the Reconfiguration Mechanisms (RM) that control reconfiguration. Not only evolutionary algorithms (EA), but other search

¹ This approach may appear risky, since not only existing circuits are affected by temperature, but also the overhead of circuits to ensure reconfiguration (granted that a very useful feature) are as well subject to similar EE-induced degradations. All practical reconfiguration systems today use switches, which add imperfections and noise. Thus reconfigurable circuits, although nice to have for the extra flexibility in possibly implementing various functions at will appears as a big problem. Yet, what is perceived first as a problem generator may turn out to be a problem solver. First, it is not absolutely necessary to implement conventional designs (obtained without considering the switches), but one can determine new designs that take the transistors that make the switches in consideration when synthesizing a circuit for the new function. In certain situations a price needs to be paid for flexibility and EE-survivability and that may be in bandwidth and signal to noise ratio. How to increase the efficiency of circuits mapped into analog arrays is still a subject of research.

algorithms can be used to find those circuit solutions for extreme environment; nevertheless, EA are particularly efficient search techniques for the large search spaces to explore when programming re-configurable chips.

An example of RH is the Field Programmable Transistor Array (FPTA-2) chip developed at JPL and used in the experiments presented later in the paper. The FPTA is a reconfigurable architecture with programmable granularity, the lowest being at the transistor level. It can map analog, digital and mixed signal circuits. The FPTA architecture is cellular, and in FPTA-2 it consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, Gaussian computational circuits, etc. It includes three capacitors of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its North, South, East and West neighbors. More details of FPTA2 are presented in [2].

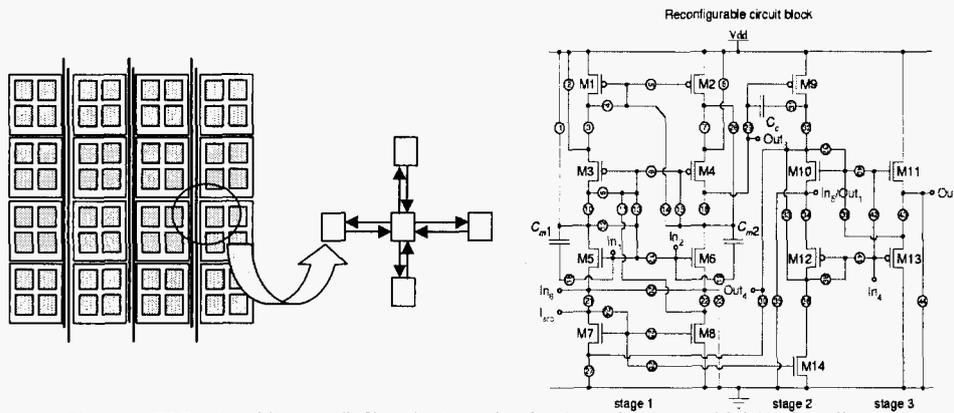


Figure 1: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

The RM determined the appropriate configuration for example by a search procedure. Thus, in evolutionary circuit synthesis/design and evolvable hardware (EHW) an evolutionary/genetic search/optimization algorithm searches the space of all possible circuits and determines solution circuits with desired functional response (here the word synthesis is used in most general sense). The genetic search is tightly coupled with a coded representation of the candidate circuits. Each circuit gets associated a "genetic code" or chromosome; the simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. Synthesis is the search in the chromosome space for the solution corresponding to a circuit with a desired functional response. The genetic search follows a "generate and test" strategy: a population of candidate solutions is maintained each time; the corresponding circuits are then evaluated and the best candidates are selected and reproduced in a subsequent generation, until a performance goal is reached. In this project, since device models for EE are not available, circuit evaluation is done directly in reconfigurable hardware. The steps of an EA are sketched in Figure 2. More details on Evolutionary Circuit Design can be found in [3].

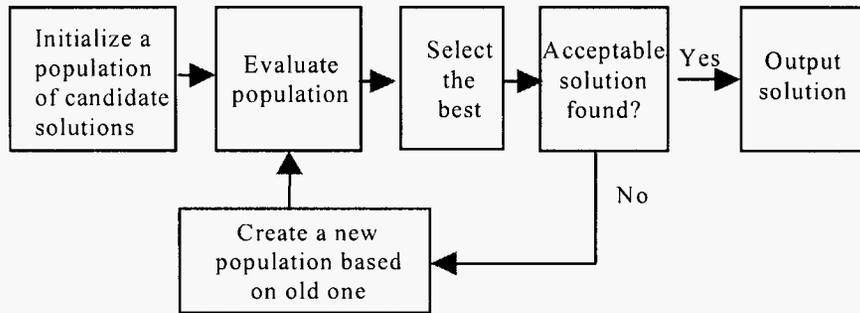


Figure 2: Block Diagram of a simple Evolutionary Algorithm

To create a complete EHW system, a stand-alone board-level evolvable system (SABLES) was built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm [4]. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is fast, with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature and radiation experiments. The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 individuals for 200 generations require less than a minute. Figure 3 shows the diagram of an EHW process and the schematic of SABLES system.

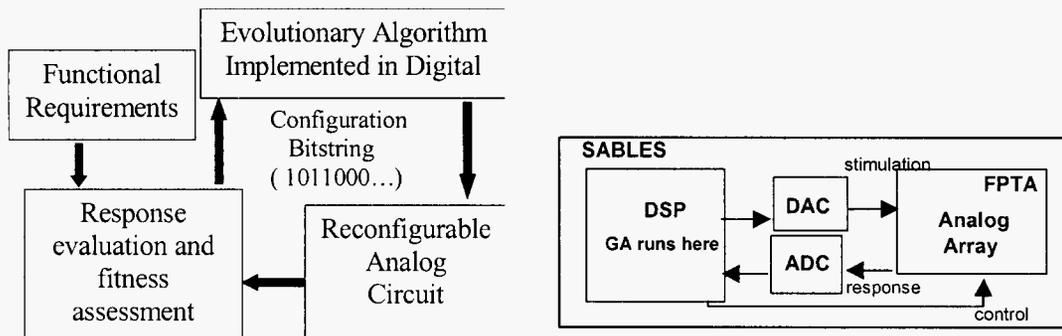


Figure 3: Block diagram of the evolutionary reconfiguration process. Reconfigurable analog circuits are reconfigured under the control of a reconfiguration algorithm, such as an evolutionary algorithm. JPL implementation used two chips, the reconfigurable analog circuits being part of a FPTA chip, the other functional blocks being run in a DSP. Only the FPTA was exposed to EE. In proposed work the entire system will be on one chip exposed to EE.

3. Experiments in functional recovery by evolution

3.1 Generalities

Multiple experiments on recovery of various functional circuits were performed. Initially a human designed circuit was mapped into the FPTA, or a circuit was evolved at room temperature, for the function of interest. The chips were then exposed to EE and degradation was observed. At that point evolutionary recovery was started and a new circuit, with same intended function was obtained – sometimes imperfect but still good approximation for the problem at hand. In some cases the function can not be recovered within the imposed precision: this may be either a limit of the hardware (no solution exists) or of the algorithm that was not able to reach a solution in the given time (sub-optimal algorithm or insufficient time). All the experiments illustrated below present the recovery of functionality of a half wave rectifier, and tests are done with a 2 kHz sine wave input. The experiments limited FPTA resources to the use of only two cells. Other circuits that

were recovered by evolution include logical gates, filters, amplifiers, and various analog computational circuits.

The fitness function given below does a simple sum of error between the target function and the output from the FPTA. The input was a 2 kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for } (t_s < n/2) \\ R(t_s) - V_{\max} / 2 & \text{otherwise} \end{cases}$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{\max} is 2V (the supply voltage). The output must follow the input during half-cycle, staying constant at a level of half way between the rails (1V) in the other half.

After the evaluation of 100 individuals, these were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), either among themselves or with an individual from the elite, and then mutation (4% rate). The entire population was then reevaluated. An oscilloscope snapshot during executions over a generation and a detail fragment are shown in Figure 4.

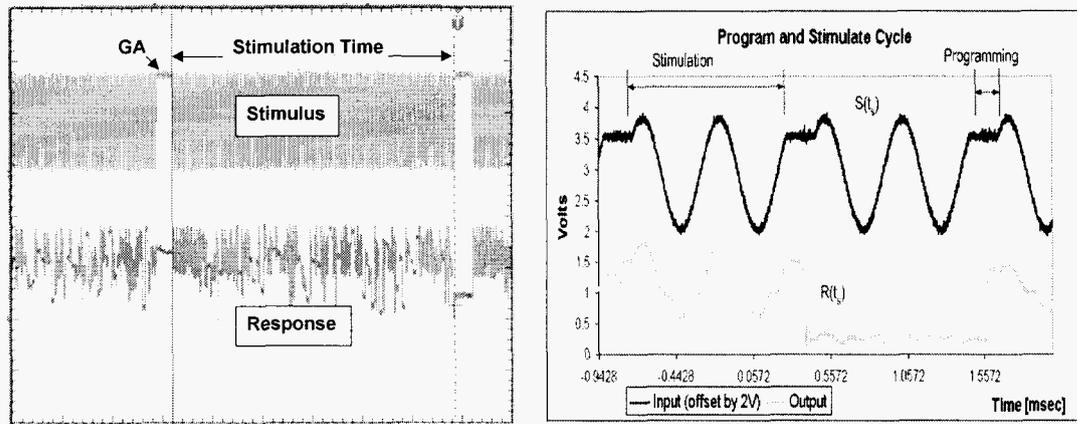


Figure 4. Stimulus-response waveforms during the evaluation of a population in one generation (left) and zoom-in for 2 individuals in the population (right). A full EA cycle includes stimulus/response sequence (113ms) and the generation of the next generation (6ms).

3.1 Recovery of Half wave rectifier at 300kRad TID

The radiation setup used in the experiments presented here used a Cobalt 60 sourced gamma rays instead of the electron beam used previously [5]. Compared to the radiation offered by electron beams and protons used previously, Cobalt 60 gamma rays are significantly higher energy and much more penetrating. Logistically, the test involved placing a FPTA chip and its associated host board 28.5 cm away from a shielded Cobalt 60 source. The host board was included to provide easy biasing. When exposed at that distance, the Cobalt 60 source subjects the chip to 50 rad/sec of gamma ray radiation. FPTA chips were radiated under both biased (power on) and unbiased (power off) conditions. The biasing scheme promotes ionization by introducing a potential difference across the inputs and outputs and thus facilitating the trapping of charge.

As opposed to our previous experiments reported in [5], in which case degradation started below 50kRad, no change in the behavior of the circuit for TID levels up to 200Krad was observed. This was consistent with

the monitored values of NMOS threshold voltage value, for which noticeable changes started at 200Krad. Figure 5a shows the original response without radiation, Figure 5b shows the slightly degraded half-wave rectifier response at 200Krad. Figure 5c depicts the degraded response at 300Krad and Figure 5d the response of the recovered circuit obtained through evolution. The circuit recovery was performed in about a 5-minute execution of evolutionary algorithm, sampling 200 individuals per generation, over 100 generations. More details are presented in [6].

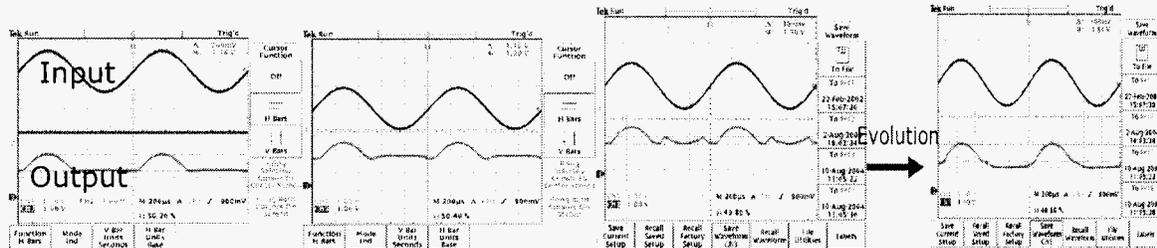


Figure 5: Response of the half-wave rectifier circuit before radiation was applied to the chip b) Half-Wave rectifier response at 200Krad c and d) Response of the Rectifier circuit after being radiated to 300kRads resulting in deterioration (left) through loss of rectification, followed by recovery through Evolution (right).

3.2 Recovery of Half wave rectifier at -196 °C

The low temperature testbed used liquid nitrogen establishing a temperature of -196.6°C. In order to study the effect of low temperatures on the FPTA device only, the chip was placed on a separate board that was immersed into liquid nitrogen. This setup did not allow a control for intermediate temperatures between room ambient and liquid nitrogen. A standard ceramic package was used for the chip. A half-wave rectifier was evolved at -196.6°C, the oscilloscope caption being shown in Figure 6a. This was not a robust solution (and it was not even expected to be, since evolutionary algorithm was not asked, through the fitness function, to respond to an entire temperature range) and when taken out to room temperature the response deteriorated as shown in Figure 6b.

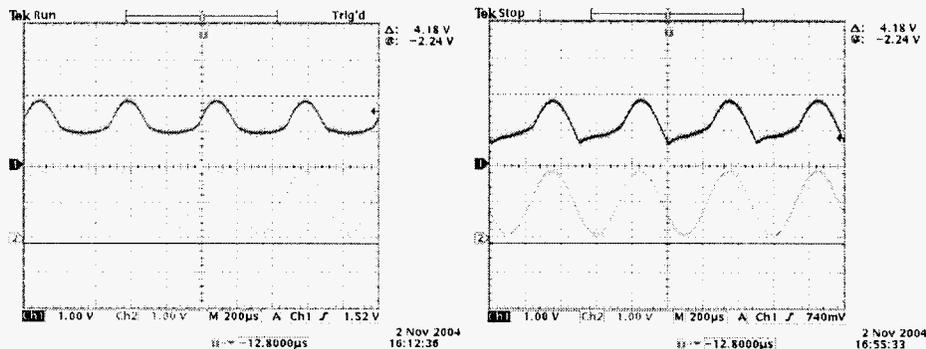


Figure 6: Half-wave rectifier recovered at -196C ; solution is not robust and degrades when returned to room temperature

3.3 Recovery of Half wave rectifier at 280 °C

A high temperature testbed was built to achieve temperatures exceeding 350°C on the die of the FPTA-2 while staying below 280°C on the package. The testbed includes an Air Torch system firing hot compressed air through a small hole of a high temperature resistance ceramic protecting the chip. Details of the set-up are given in [7]. Figures 7a and 7b depicts the response of the evolved circuit at room temperature and the degraded response at high temperature. Figure 7c shows the response of circuit obtained by running evolution at 280°C, where the functionality is recovered.

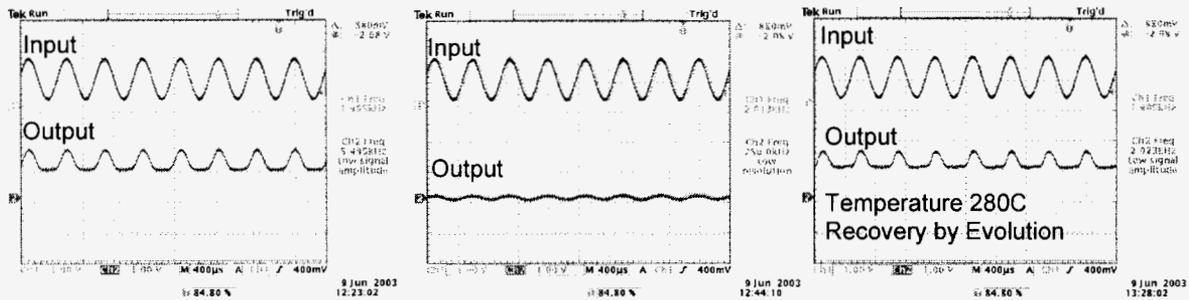


Figure 7: Input and output waveforms of the half-wave rectifier. a) response of the circuit evolved at 27°C. b) degraded response of the same circuit when the temperature is increased to 280°C c) recovered response from evolved circuit.

4. Future Work

The results summarized above prove the concept, yet have the following limitations: 1) the tests were of short duration, 2) did not implement temperature cycling, 3) did not use combined temperature/radiation testing, 4) the reconfiguration mechanism was running on a separate DSP which was not affected by temperature/radiation, 5) were not demonstrated on complex analog circuits performing in an application.

These are the goals of the next step, planned for this effort: to demonstrate the integrated reconfigurable array-reconfiguration logic in the same chip under temperatures cycles accurately replicating those in Moon and Mars and for longer duration and in combined radiation/temperature tests, performing a sensor processing function. More specific, the overall objective of the new effort is to develop/demonstrate reconfigurable analog electronics performing characteristic analog functions (filtering, amplification, etc) for extended operations in extreme environment with temperatures cycling in the range of -180°C and 120°C and cumulative radiation of at least 300kRad total ionizing dose (TID). The objective is to develop and validate Self Reconfigurable Electronics for Extreme Environments (SRE-EE) technology by demonstrating a Self-Reconfigurable Analog Array (SRAA) IC in sustained (over 200 hours) operation at temperatures between -180°C and 120°C , and irradiated to 300KRad total ionizing dose (TID). The temperature range of -180°C and 120°C covers the temperature range for both Moon and Mars environments and 300KRad TID reflects accumulative dose during very long Mars missions (100KRad for near-term missions), or missions beyond the Moon and Mars, such as to Jupiter's Moons. This would validate the technology for Moon and Mars temperature and radiation environments and the even harsher radiation environments for missions beyond. It will transition the SRE-EE technology to Technology Maturation Program (TMP) at TRL 5.

5. Conclusions

The paper presents the HBR approach and demonstrates it with laboratory experiments. The capability of adaptive self-configuration is demonstrated for radiation, low and high temperatures.

6. Acknowledgement

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7. References

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