



Considerations for operation of CMOS integrated circuits outside their cataloged temperature

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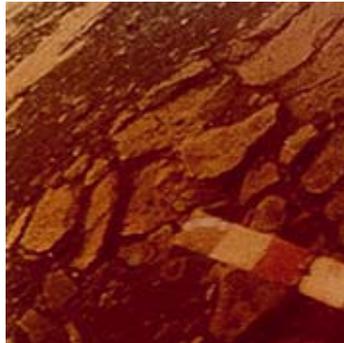
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Solar System Exploration Missions

Inner Planets:
Venus surface sample
return

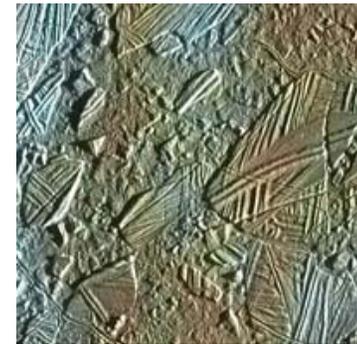


Primitive Bodies:
Comet/Asteroid Sample
Return

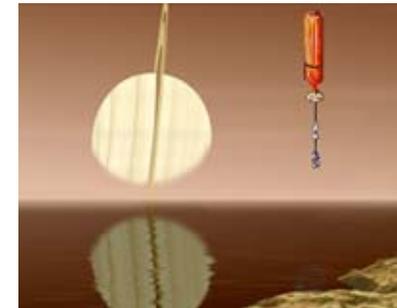


Large Satellites:

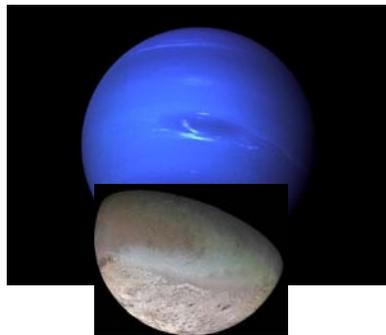
Europa Lander



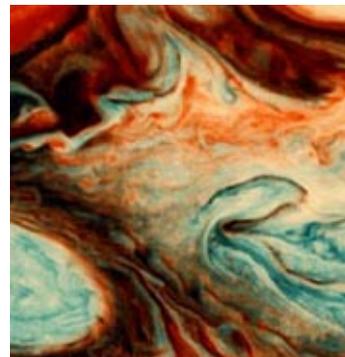
Titan *in situ*



Gas Giants



Neptune and Triton

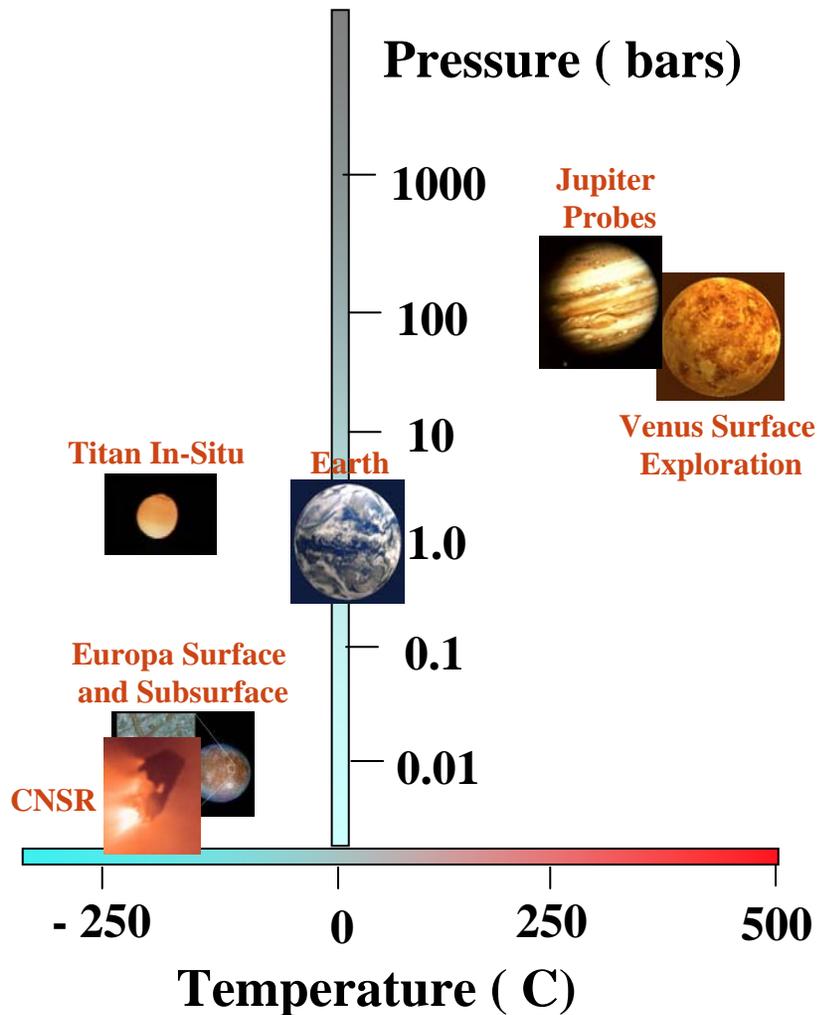


Jupiter Deep Probes

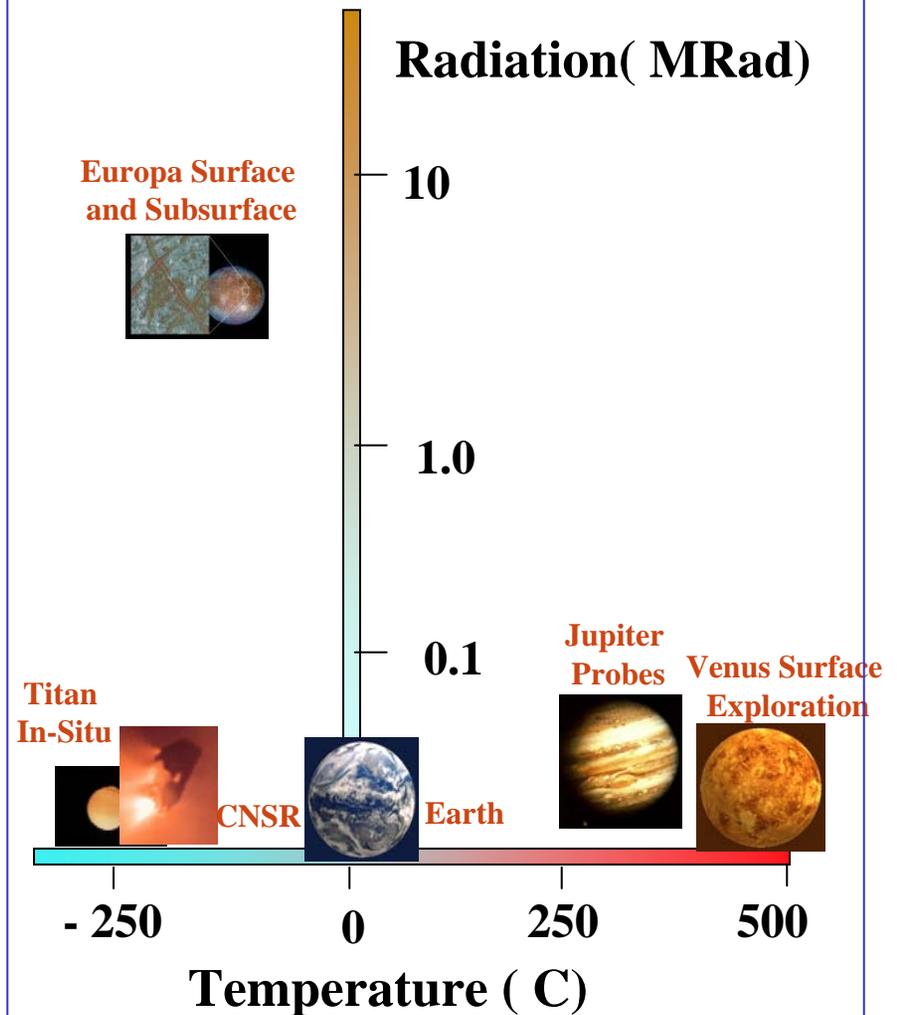


Temperature, Pressure, and Radiation

Pressure vs. Temperature



Radiation vs. Temperature





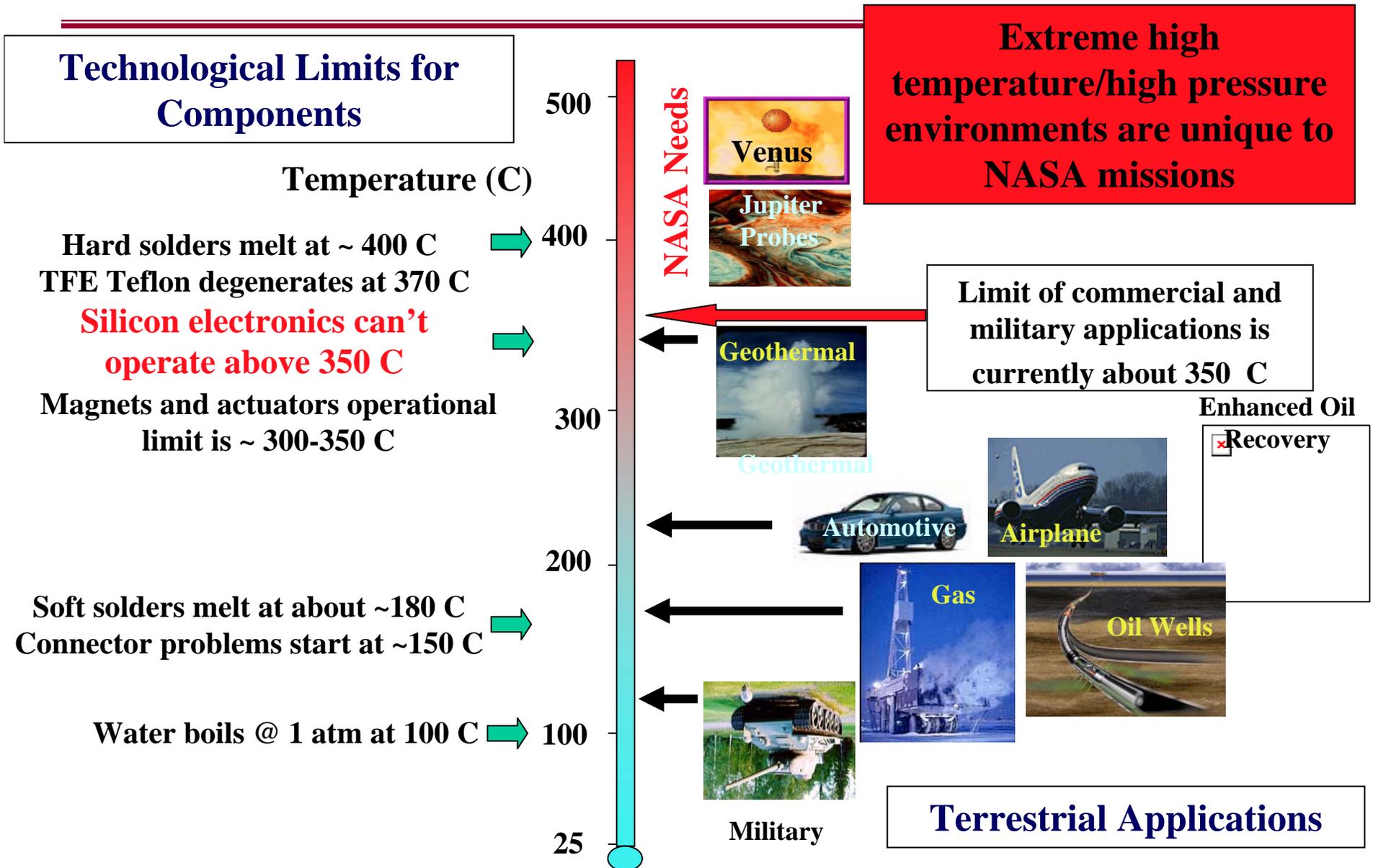
Extreme Environment Conditions Solar System Missions

Mission	Low Temp (C)	High Temp (C)	High Pressure (bar)	Radiation	Other Environmental Conditions
1. Aitken Basin Sample Return	-170				
2. Jupiter Multi-Probes	-140	380	100	6 Mrad	
3. Venus In-Situ Expl.		460	90		Sulfuric acid clouds at 50 km 97% CO2 at the surface
4. Comet Sample Return	- 140				Dust
5. (Titan In-Situ)	-180		1.5		2-10% Methane Clouds Solid/liquid surface
6. Mars Surface Expl.	-120	20		300Krad	Low Temperature Cycling
7. JIMO (with probes)	-180	350	100	6 Mrad	

Challenge: All Solar System Exploration in-situ missions have to survive in extreme temperature, pressure, and radiation environments.



High Temperature Limits of Conventional Components



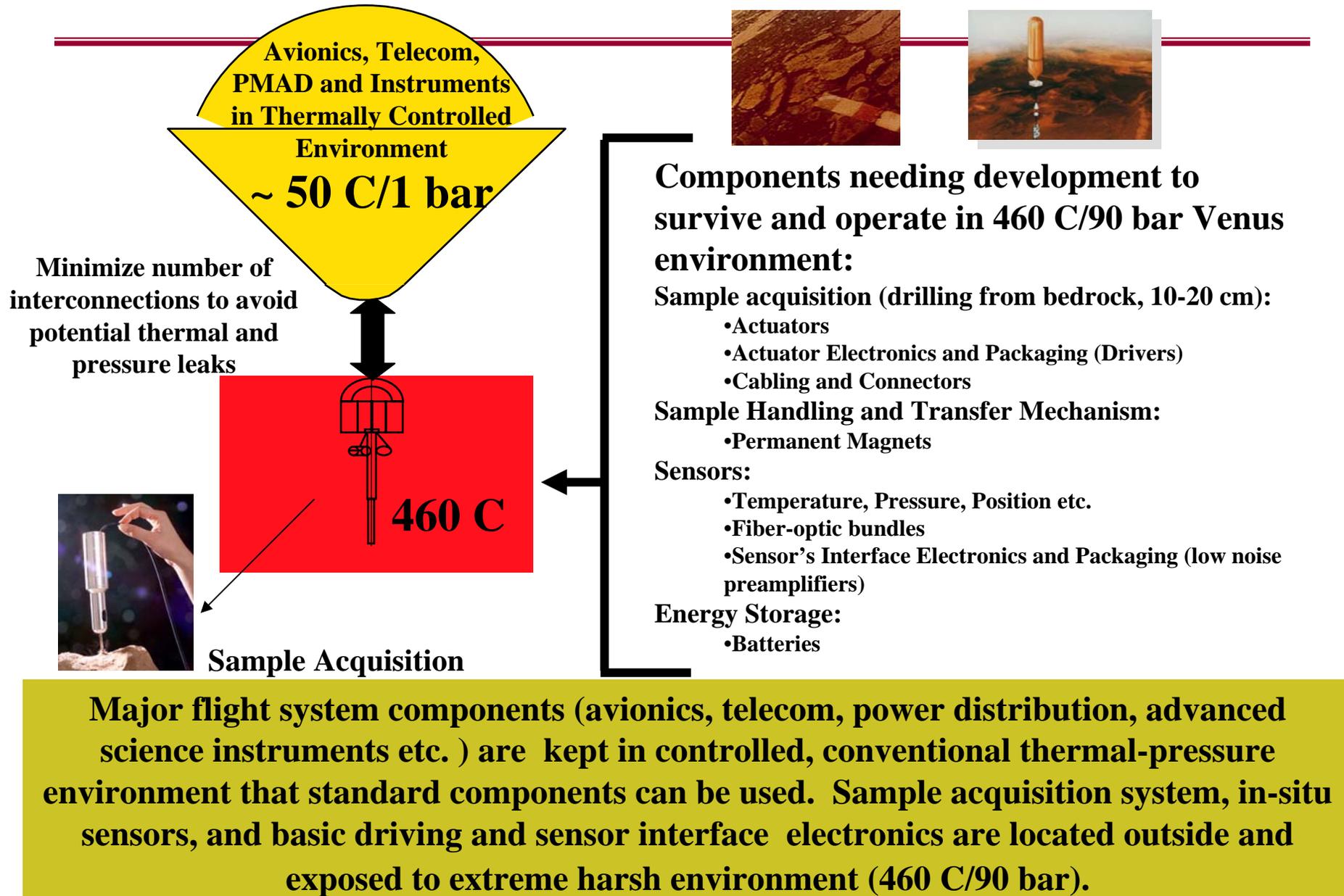


CMOS For HT Electronics

Silicon On Insulator Clearly Outperforms

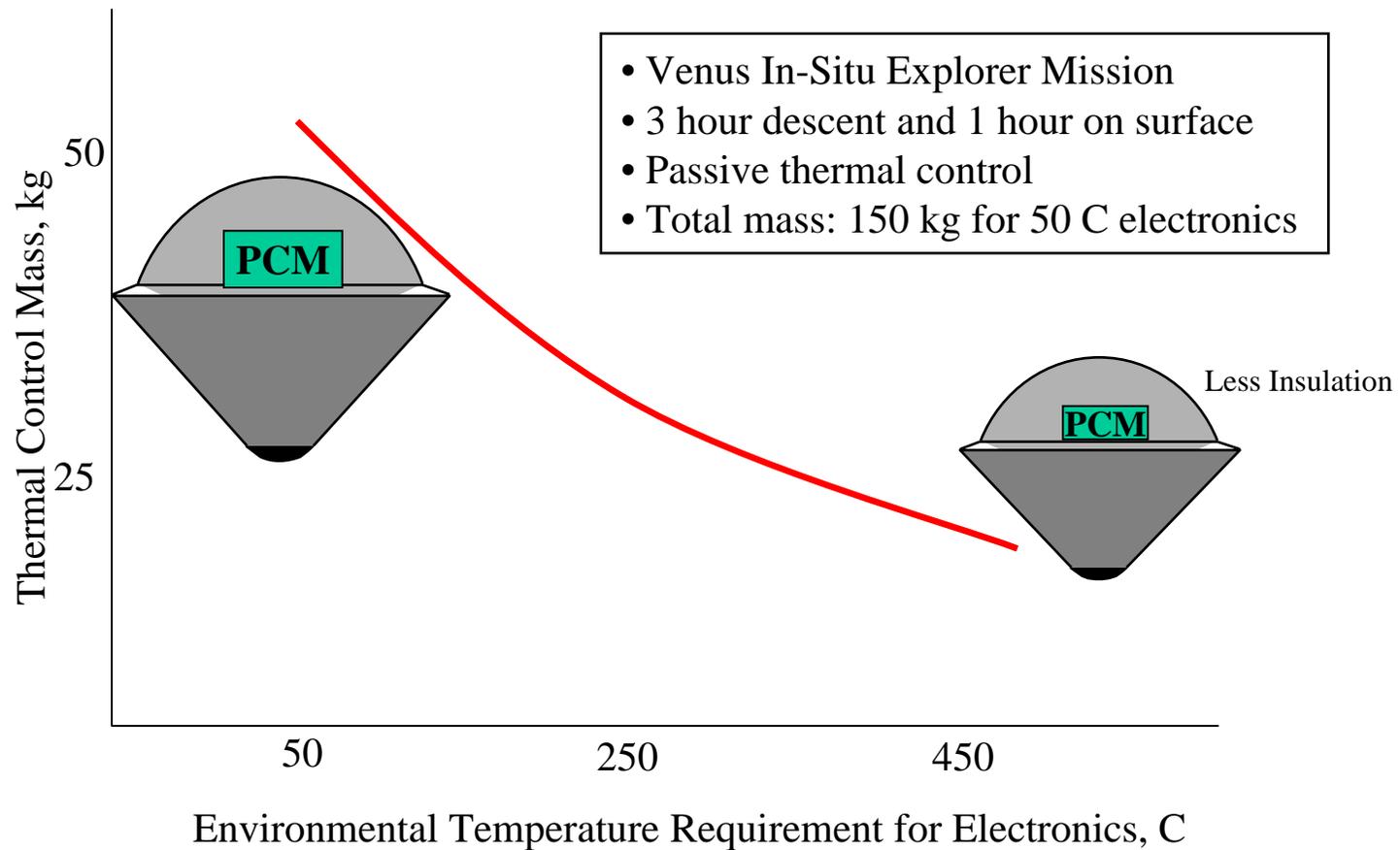


Venus Exploration - Hybrid Solution



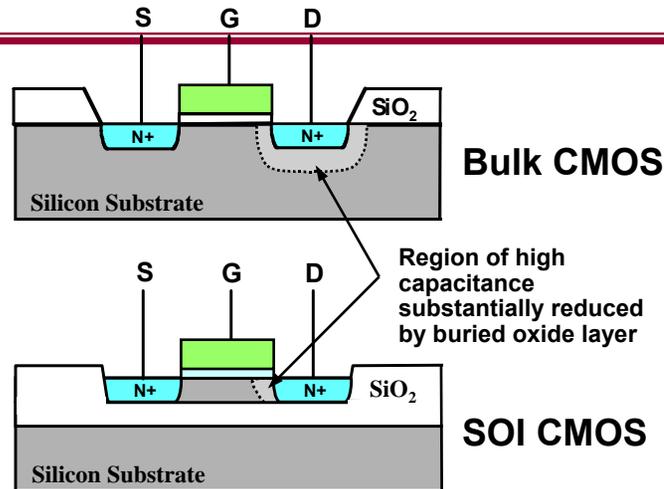


Electronics Temperature and Thermal Control Mass





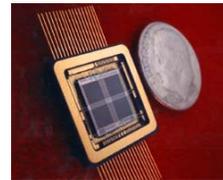
SILICON ON INSULATOR TECHNOLOGY



Buried SiO₂ Insulating Layer Provides The Following Benefits

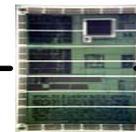
- 30% To 40% Faster Circuits
- 30% To 40% Lower Power
- Better Isolation For Mixed Signal ASICs
- High Reliability – No latch-up
- High Temperature Operation : 225°C continuous and excursions to 300°C
- Improved Sensor Accuracy And Stability

Digital SOI CMOS



- ASICs & Memories
- DoD And Commercial Applications
- 0.8 And 0.35 Micron Features
- IN PRODUCTION SINCE 1995

Mixed Mode



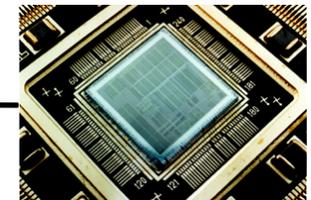
Sensors



Hi Temp Electronics



System on a Chip



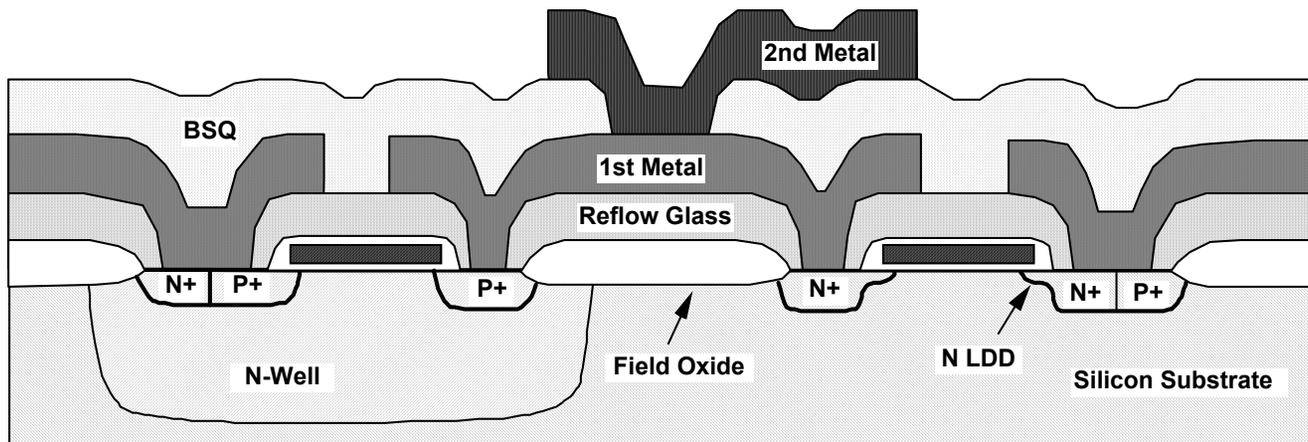
Integrated Hi Temp Sensor Systems



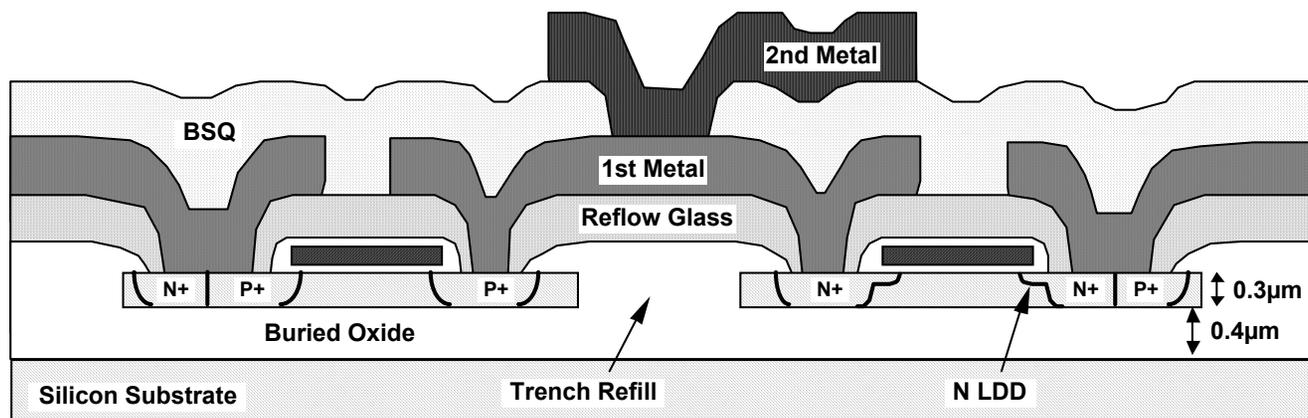
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Bulk Vs. SOI Cross-Section



Bulk

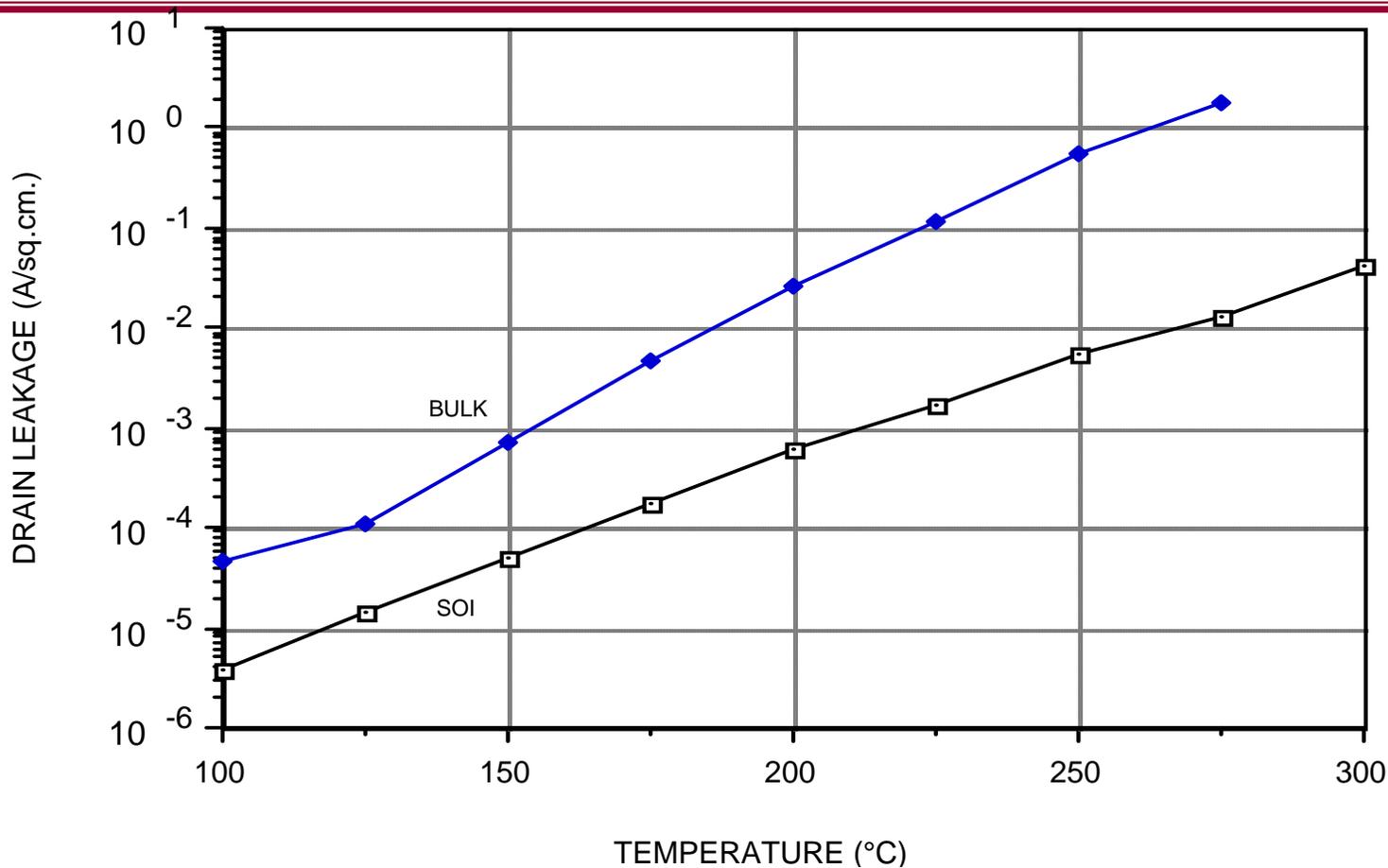


SOI



SOI vs. Bulk Leakage and Delay (1.2 μ Process)

Junction Leakage vs Temp.

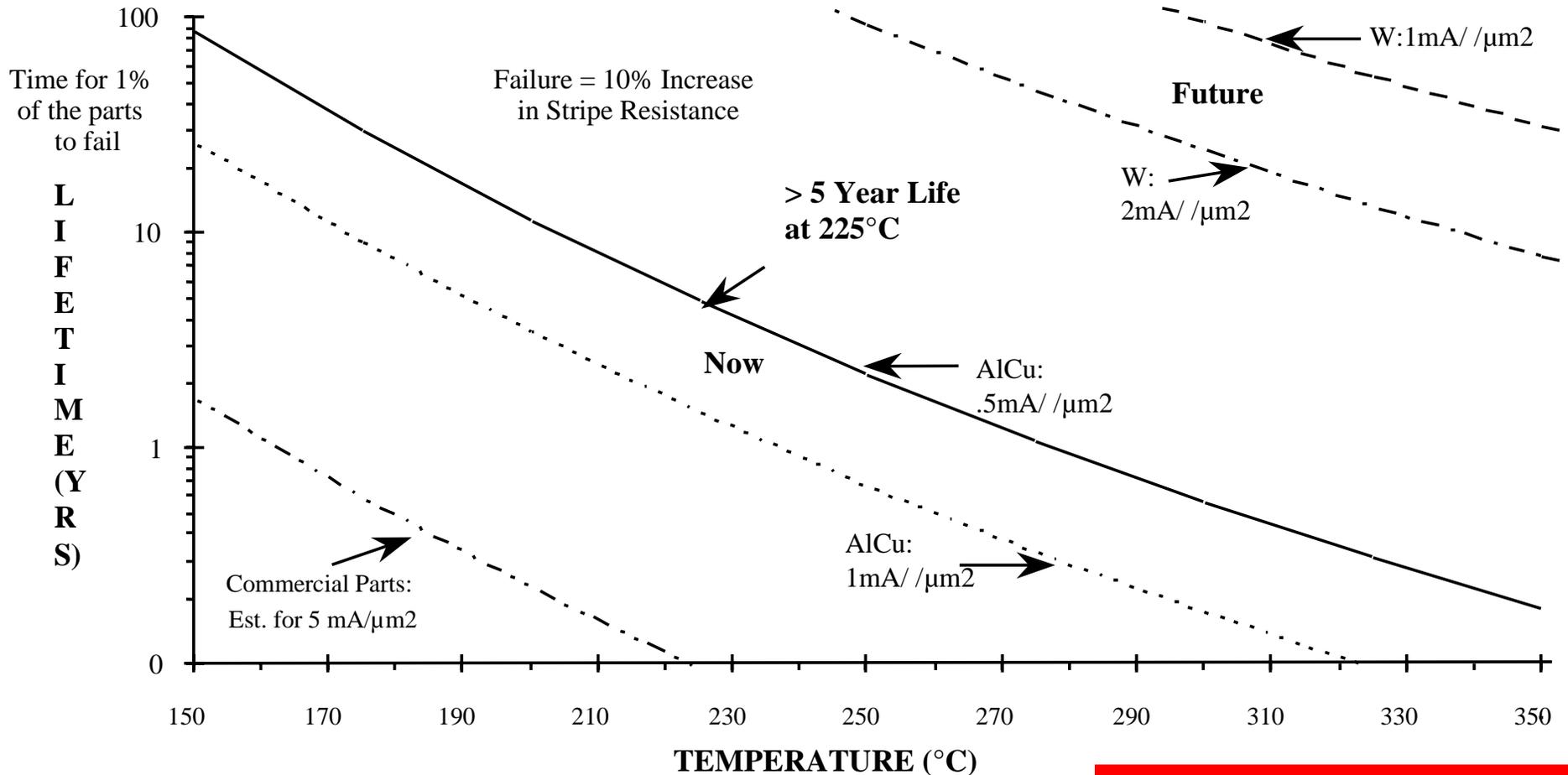


SOI has >10x less leakage than Bulk





Electro-Migration Lifetime vs. Current Density





High-temp. Issues & Mitigation Approaches



Junction Leakage

- Junction leakage doubles every 10°C (above $\approx 170^\circ\text{C}$)
- Use SOI processes – full oxide isolation

Sub-threshold transistor leakage

- Threshold voltage has a negative temperature coefficient typically $-2\text{mV}/^\circ\text{C}$. Standard SOI processes leak badly above 200°C due to sub-threshold conduction.
- Re-target room-temp. V_t 's to compensate
 - Trade-off vs. drive current, voltage head-room.
 - One reason why 5V process persists for HT vs. 3.3, 2.5, 1.8.

Electro-migration

- Aluminum inter-connect migration exponentially related to temperature
- Design to more conservative design rules
 - Wider metal traces / more vias and contacts
 - OR reduce the operating frequency (digital circuits)
- OR develop alternative inter-connect metalization (e.g., Tungsten)

Honeywell



High-temp. Issues & Mitigation Approaches



Reduced mobility vs. Temperature

- Reduces digital drive currents, analog gain (gm)
- Use larger devices for digital logic (or de-rate speed at HT)
- Temperature compensate bias currents to stabilize gain vs. temp. (increases power consumption at high temp.)

Bias voltage drift with temperature

- Mobility and V_t drift with temperature may cause wide range of bias voltage variation, eating into common-mode input range or output range
- Use “Zero Temperature Coefficient” biasing
 - Play V_t shift against mobility shift to stabilize bias voltages
 - Requires good models over temp.

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Current HTMOS Standard Electronic Products



Product #	Function	Die	SCP
HT1104	Quad Op Amp	Now	Now
HT1204	Quad Switch	Now	Now
HT506	16:1 Analog Mux	Now	Now
HT507	8:2 Analog Mux	Now	Now
HT6256	256K Bit SRAM	Now	Now
HT83C51	8 Bit Micro Controller	Now	Now
HT2080	80K Gate Digital Array	Now*	Now*
HT2160	160K Gate Digital Array	Now*	Now*
HTCCG	Crystal Clock Generator	Now	Now
HTPLREG	+5, +10 Or +15V Voltage Regulator	Now	Now
HT574	12 Bit A/D Converter	Now	Now
HTANFET	Power FET	Now	Now
HT6656	256K Bit ROM	Now	Now

Products in Red are 5V, 0.8 μ SOI4 High Temp. Process

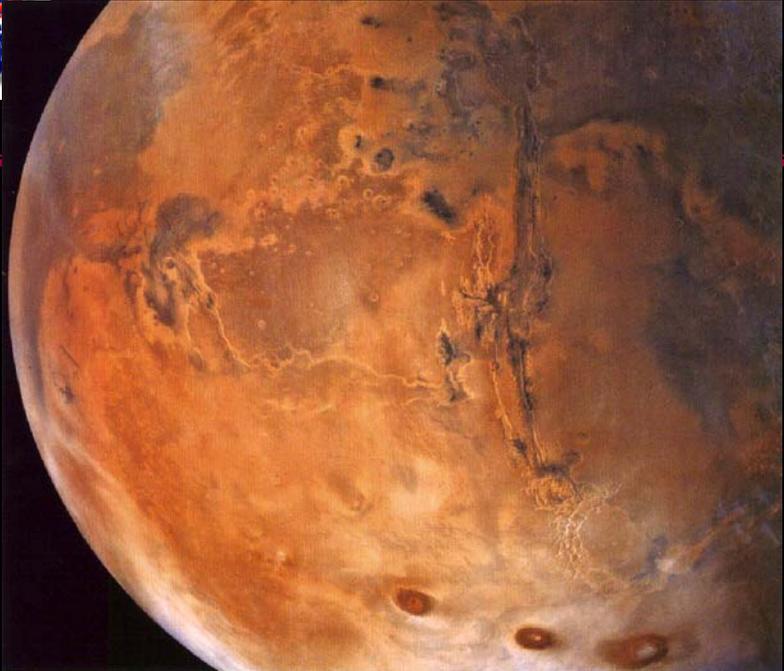
Products in Black are 1.2 μ 10V-Linear High Temp. Process

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Summary SOI CMOS for HT

- **SOI CMOS is widely recognized as the most viable near-term solution for extending operating temperature for integrated circuits above 175°C**
- **SOI CMOS is capable for analog/mixed-signal signal conditioning and control applications**
- **For high power-density actuator/driver applications SOI is at a disadvantage relative to SiC**
- **Minor modifications to SOI processes are needed to extend temperature range for complex IC's beyond 200°C**
- **Complete solutions are required: Analog/mixed-signal in addition to digital**
- **Exploiting synergy between SOI for rad-hard DoD and SOI for high-temp. down-hole applications will benefit both user communities**





Mars Missions



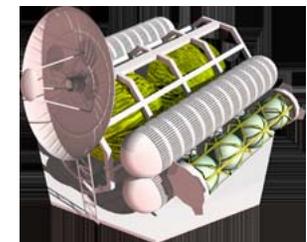
Balloons



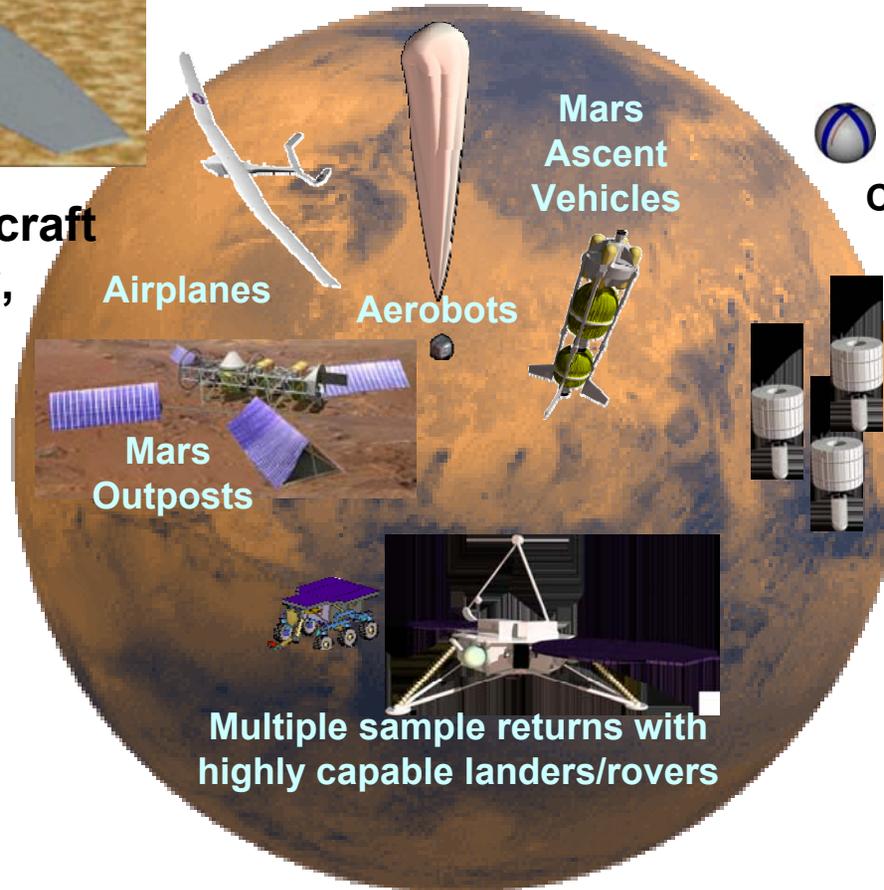
Sample Return Canisters



Networks of Microprobes



Science Micromissions

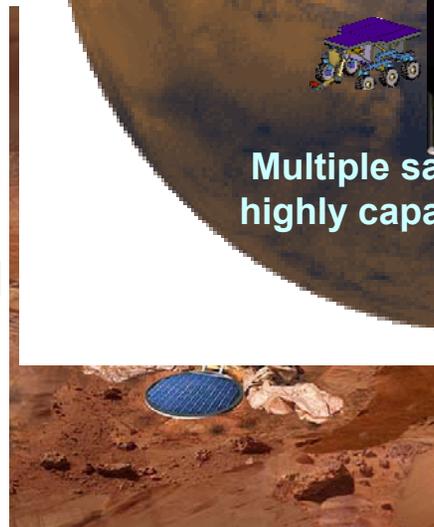


- Highly diverse spacecraft (size, power, mobility, lifetime, ...)

- Globally distributed missions

- Complex and demanding surface and orbital operations

- Evolving capabilities

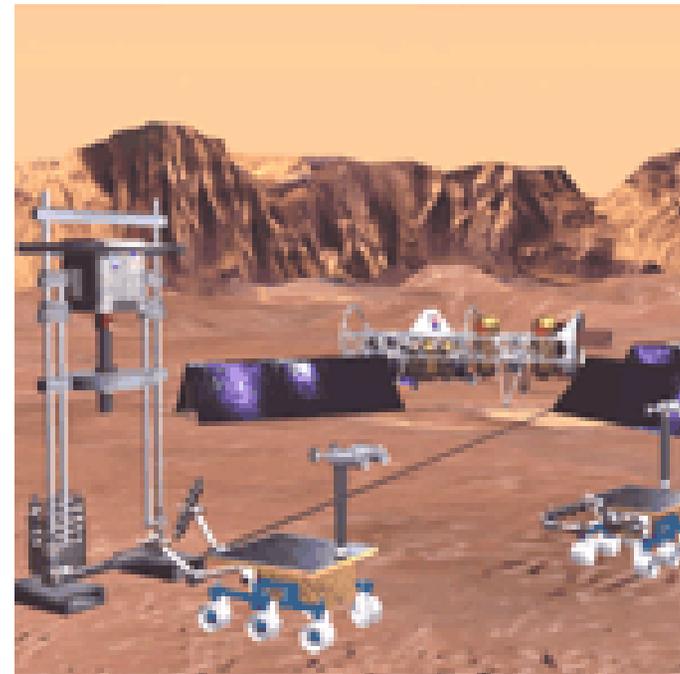




Motivation for Low Temperature CMOS



- **NASA plans to launch a long range rover for exploring the surface of Mars by 2009**
- **The temperature on Mars can vary from -120°C to $+20^{\circ}\text{C}$ depending on time of day and location**
- **A major challenge for Mars rover missions is developing robust instrumentation and control electronics that can function properly over a broad temperature range.**





Can we use commercial electronics for direct use in Mars? 85C>T>-120C



Key Challenges in Electronics:

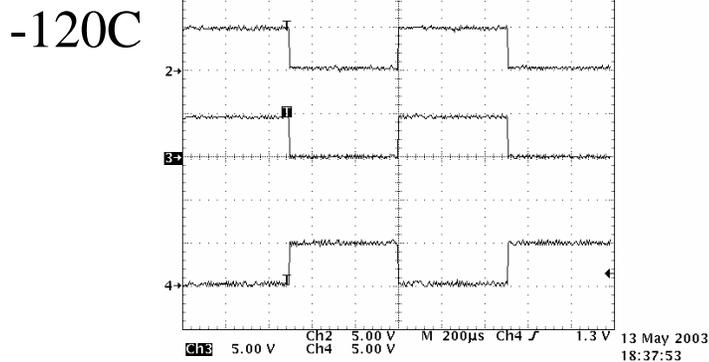
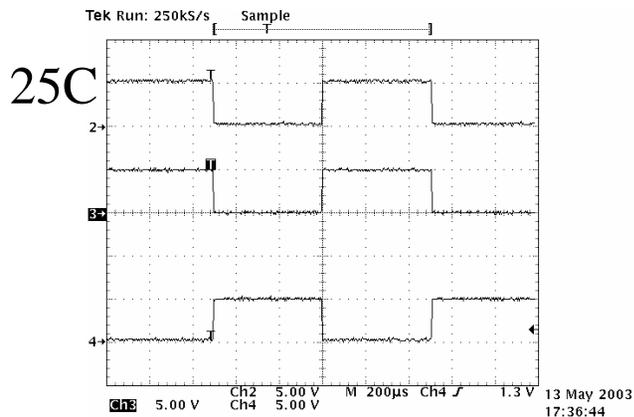
- **Commercial Off The Shelf analog electronics (transistors, amplifiers, ADC's...) are designed and tested down to -55C. These parts have unknown electrical characteristics at temperatures lower than -55C.**
- **Complex programmable digital circuits Field Programmable Gate Arrays (FPGAs) may have issues with Clock Tree, Anti Fuse technology , On board RAM, PLL, Setup and Hold times.**
- **The reliability of both analog and digital commercial CMOS components at lower than -55C is generally unknown.**
- **There are no design rules or simulation models for fabrication of electronics components operating at -120C**



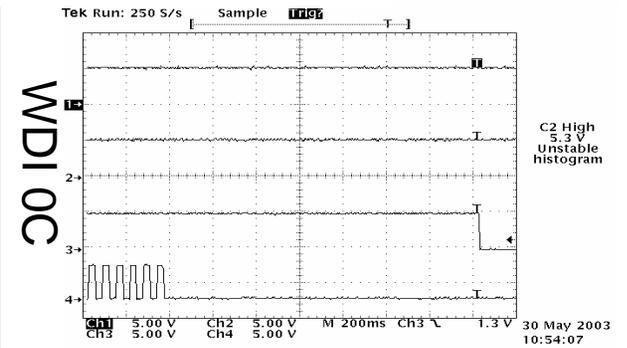
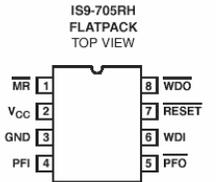
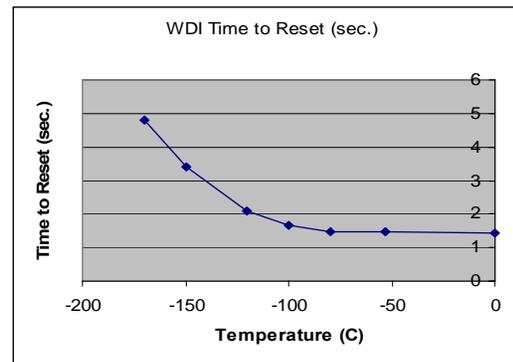
Experimental Results

-Hex Inverter and Power-on Reset Circuit

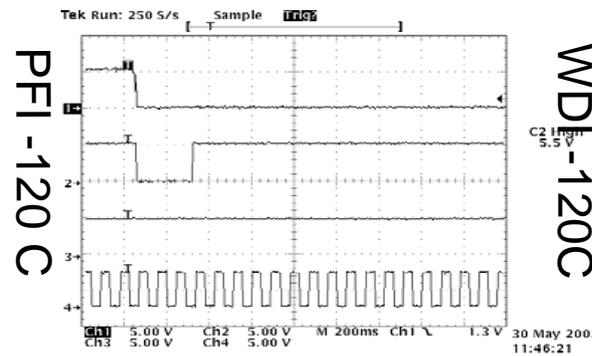
HCS114MS Hex Inverter



Power-On Reset IS-705RH



WDI ~1.42 sec. to reset



WDI ~2.1 sec. to reset

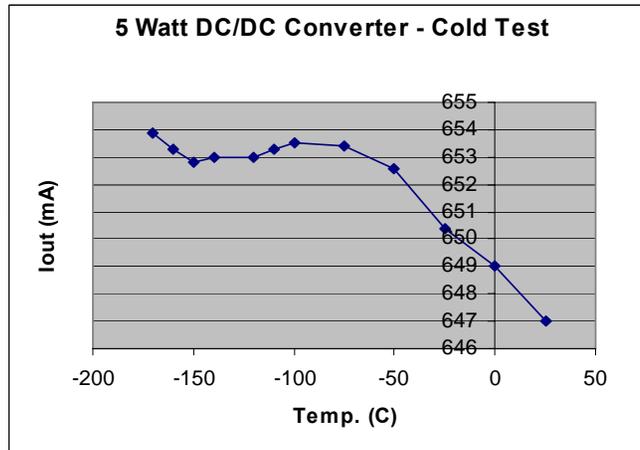


Experimental Results – Interpoint DC-DC Converter

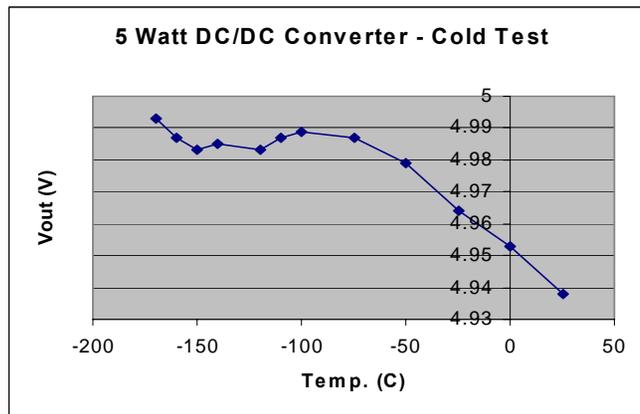


1.075 x 1.075 x 0.270 inches
(27.31 x 27.31 x 6.86 mm)

5W DC-DC Converter

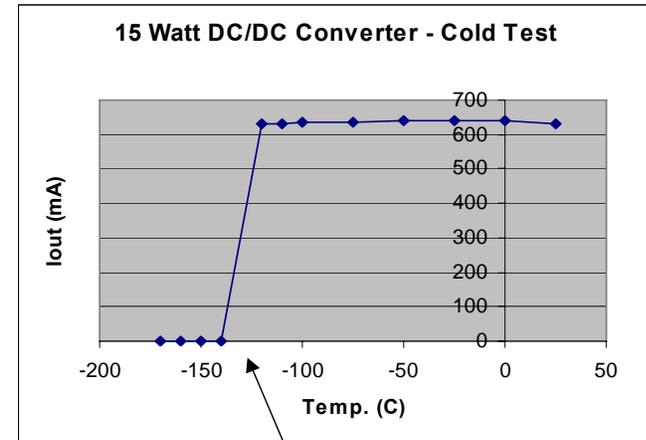


Below -150 °C the device took noticeably longer to come out of inhibit mode

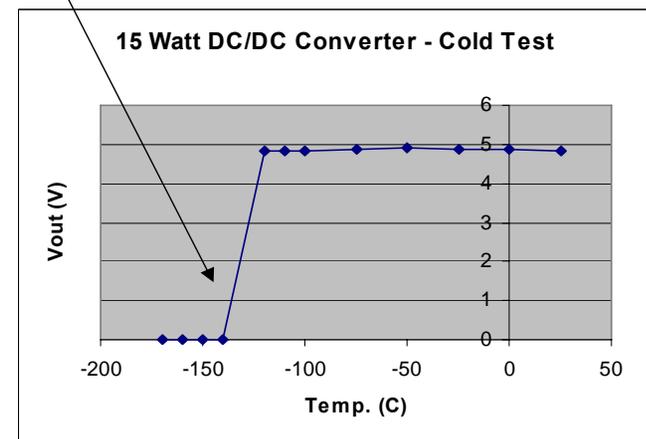


- **5W converter functioned down to -160C.**

15W DC-DC Converter



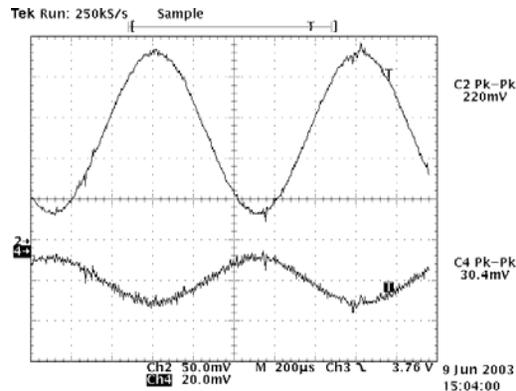
Device failed at slightly colder than -120 °C



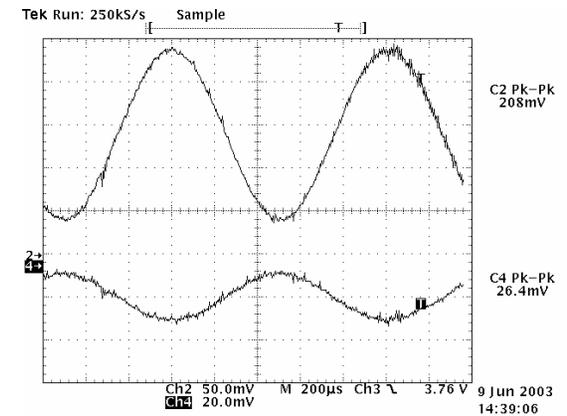
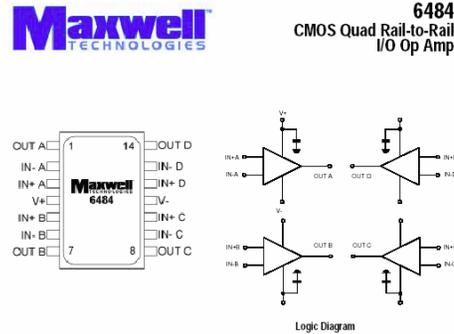
- **15W converter only functioned down to -130C.**



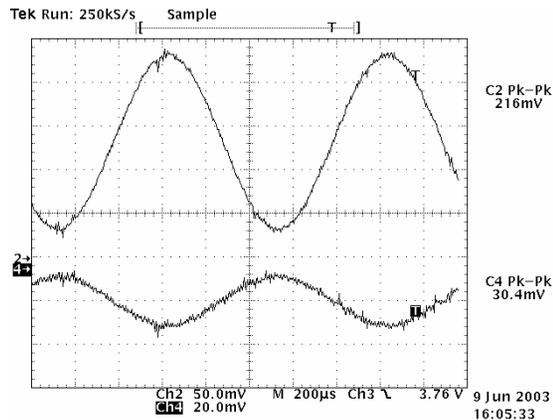
Experimental Results - OPAMP LM 6484



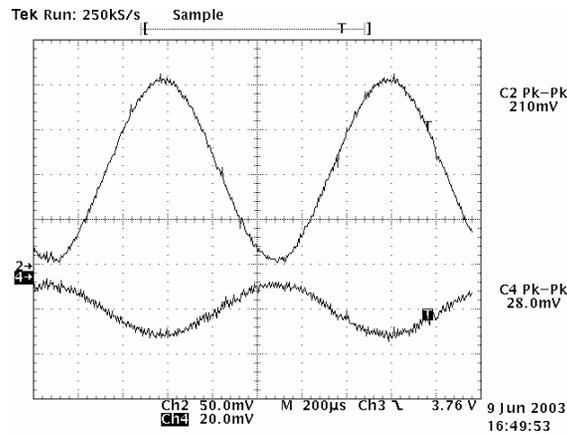
6484 - Plastic 25 °C



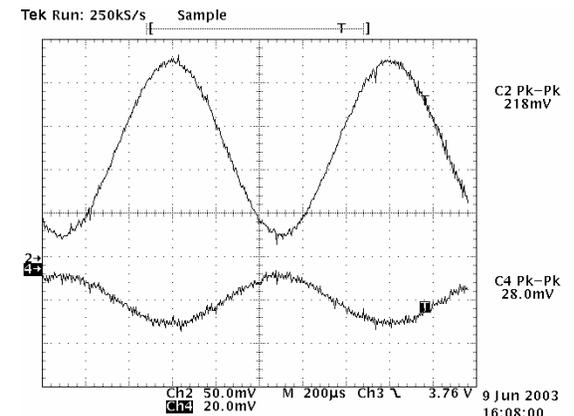
6484 - RAD 25 °C



6484 - Plastic -120 °C



6484 - RAD -165 °C

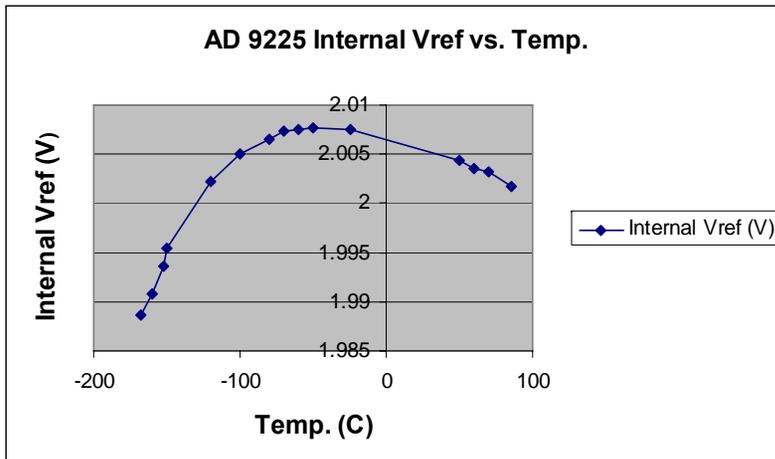
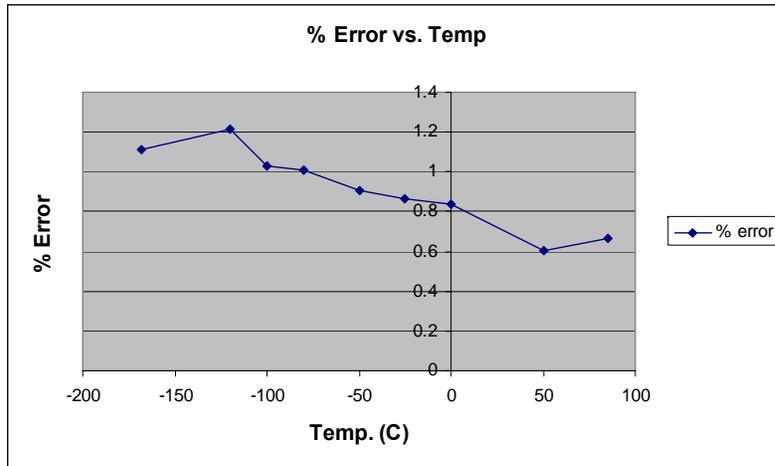


6484 - RAD -120 °C

OPAMP worked down to -165 Deg C



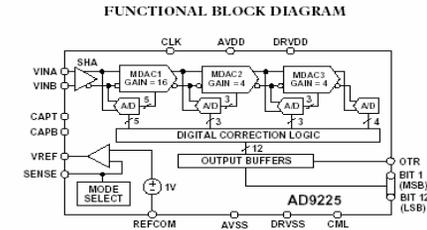
Experimental Details – ADC 9225



Complete 12-Bit, 25 MSPS
Monolithic A/D Converter

AD9225

FEATURES
 Monolithic 12-Bit, 25 MSPS A/D Converter
 Low Power Dissipation: 280 mW
 Single +5 V Supply
 No Missing Codes Guaranteed
 Differential Nonlinearity Error: ± 0.4 LSB
 Complete On-Chip Sample-and-Hold Amplifier and Voltage Reference
 Signal-to-Noise and Distortion Ratio: 71 dB
 Spurious-Free Dynamic Range: -85 dB
 Out-of-Range Indicator
 Straight Binary Output Data
 28-Lead SOIC
 28-Lead SSOP
 Compatible with 3 V Logic

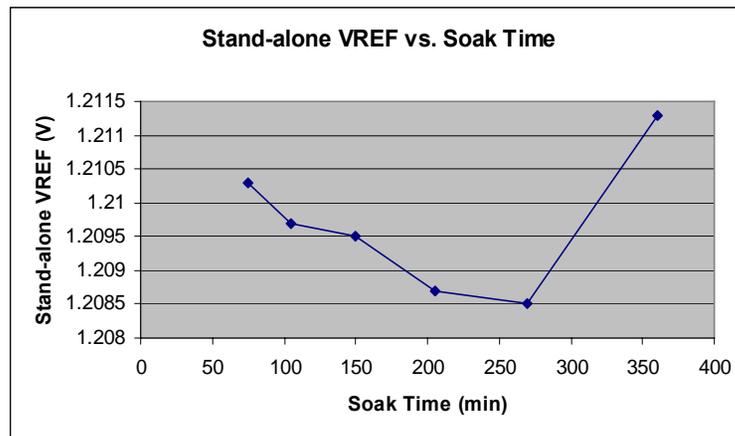


- The AD9225 analog-digital converter (12-bit) yielded 11-bit resolution at -80 °C and 10-bit resolution down to -168 °C.
- This performance meets the needs of the actuator task
- After cold soaking for 5 minutes at -160 °C, Vref stabilized and output had 1.2 % error.

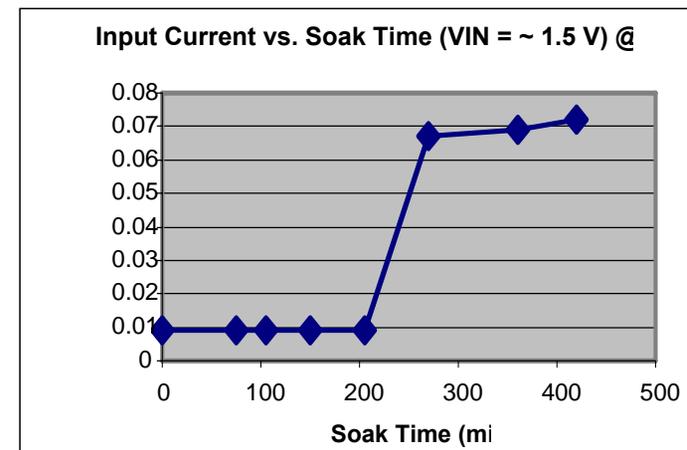
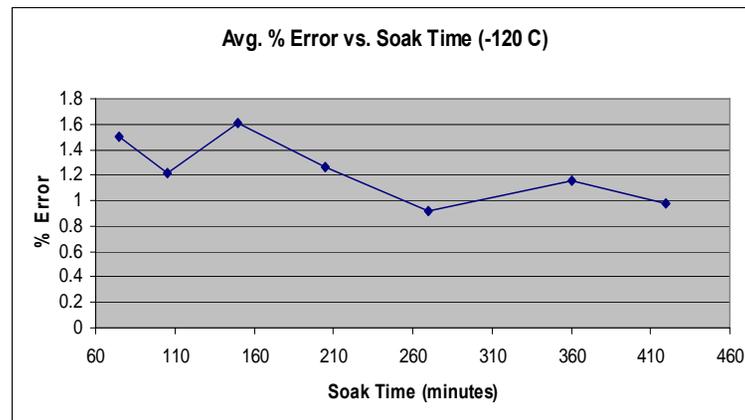


Experimental Results – ADC 9225

ADC performance after 500 minutes of soak at -120C suggests that further cold temperature analysis is needed



- **Vref and input currents increased after 200 minutes of operation at -120C .**
- **There may be a potential long term reliability problem for continuous operation under cold temperature.**
- **Will do long term cold temperature soak**





Experimental Results – FPGA

ACTEL FPGA	Density (System Gate)	RAM	Radiation (TID) (Krad)	Package	† TMR	Temp (°C)
RT54SX72S	108 K	No	100	208-Pin Ceramic Quad FP	*Yes	-55 to +125
A54SX32A	48 K	No	No	144 Thin Quad FP	No	-40 to +85
FPGA Xilinx	Density (System Gate)	RAM	Radiation (TID) (Krad)	Package	† TMR	Temp (°C)
XQVR600	661 K	Yes	100	228-Pin Ceramic Quad FP	No	-55 to +125
XCVR600	661 K	Yes	No	240-Pin High Heat Dissipation Quad FP	No	-40 to +100

Commercial Actel FPGA (A54SX32A) results: Digital logic functioned down to -165C. Power cycling functioned to -165 C

Commercial Xilinx FPGA (XCVR600) results: Digital logic (program load at 0C) functioned down to -165 C. Power cycling, initialization current increased from 10 mA at 0C to 800 mA at -40C.



TCRE Experimental Results Summary

Power and Switching FETs			Voltage Regulator / Power Supply / Reference		
P Channel - IRHNA597260	International Rectifie	PASS at -165 C	HS-117RH (adjustable)	Intersil	Died at -130 C
N Channel - IRHNA57260SE	International Rectifie	PASS at -165 C	SMSA2805S / OO / HO / HR / HK	Interpoint	PASS at -170 C
RIC7113L4 - High / Low Gate Dri	International Rectifie	PASS at -165 C	LM184-1.2	National Semiconduct	PASS at -165 C
JANSR2N7262	International Rectifie	PASS at -165 C	A to D		
IRHG597110	International Rectifie	PASS at -165 C	AD9225AR	Analog Devices	PASS at -165 C
IRHG57110	International Rectifie	PASS at -165 C	Inverters		
IRHNJ57034	International Rectifie	PASS at -165 C	HCS14MS	Intersil	PASS at -120 C
IRHNJ597034	International Rectifie	PASS at -165 C	Power On Reset		
OP-AMP / Discrete Transistors / FETS			IS-705RH	Intersil	PASS at -170 C
U430-2	Vishay	PASS at -165 C	Level Shifter		
2N3811	Microsemi	PASS at -165 C	CD40109BDMSR	Intersil	PASS at -165 C
LM394CH	National Semiconduct	PASS at -165 C	Resolver		
FPGA			CT5028-2-I (Preliminary Info)	Aeroflex	
XQVR600-CB228 (QPro Virtex 2	Xilinx		New Parts Additions		
XCV600-5HQ240I	Xilinx	800 mA at -40C			
RT54SX72S-1CQ208-1	Actel				
A54SX32A-144	Actel	PASS at -165 C			

- Tested 22 components down to -165C
- 2 components failed



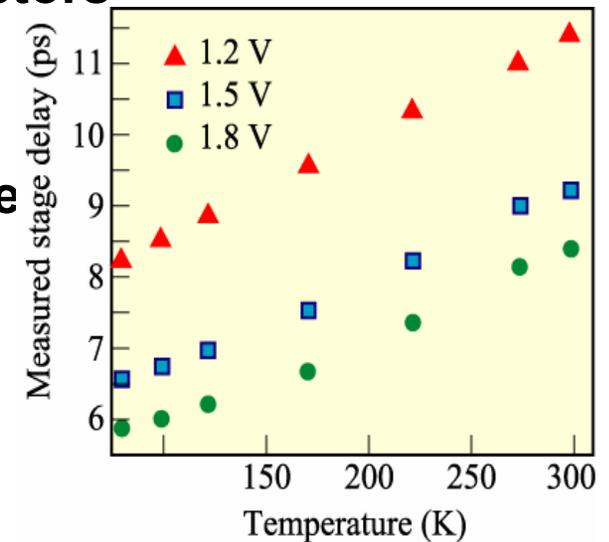
What if COTS Fail

**Is Custom Mixed Signal ASICS for Cold Temperatures
and Option?**



Why is cold silicon cool ?

- Improved transport properties
 - higher mobility ($\mu \sim T^{-1.5}$) and saturation velocity (+ 50-100%)
 - velocity overshoot in ultra-short devices
- Better subthreshold swing ($S \sim T$)
- Reduced leakage current ($I \sim e^{-E/kT}$)
- Reduced electromigration & interconnect resistance
- Possible combination CMOS + superconductors
- Lower thermal noise
- Improved thermal conductivity of silicon
- Ideal for quantum and single-electron device
- Improved speed for cryogenic operation



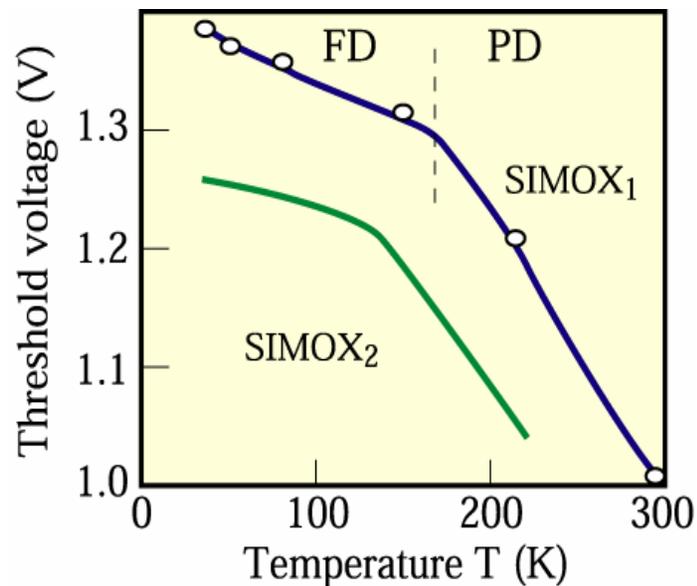


Threshold Voltage



At low T:

- Fermi level increases
- Threshold voltage increases
- Depletion depth extends
- Double slope: transition from partial to full depletion
 $dV_T/dT = 1.9 \text{ mV/K}$ (PD, $\alpha = 1$) or 0.6 mV/K (FD, $\alpha = 0$)

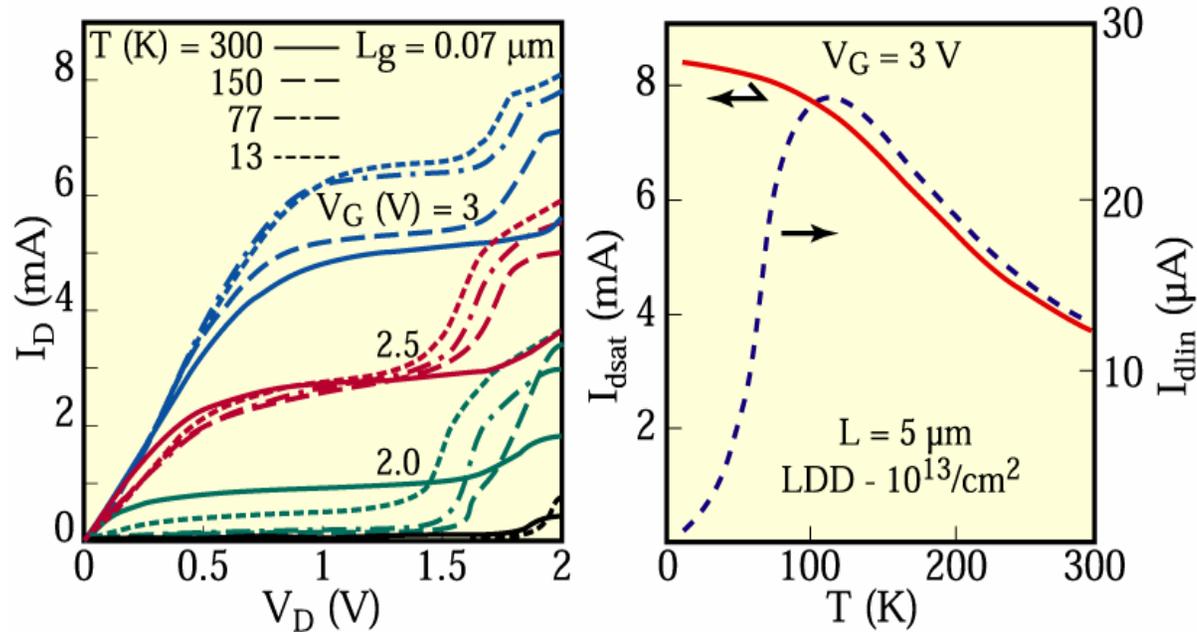


$$\frac{dV_T}{dT} = \frac{d\Phi_F}{dT} \times \left(\alpha \frac{C_D}{2C_{ox}} + \frac{qD_{it}}{C_{ox}} + 2 \right)$$



Drive Current

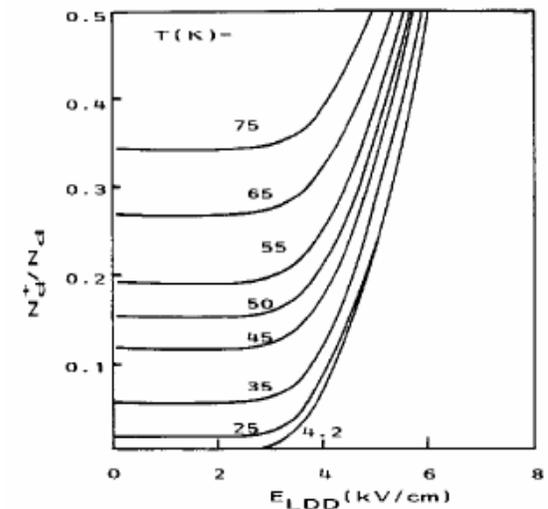
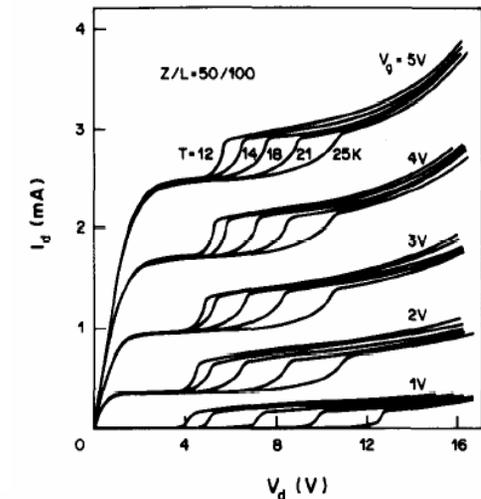
- Drain current can increase or decrease at low-T
- Impact of device architecture (inversion or accumulation mode, LDD, ...)
- Competing mechanisms
 - mobility, threshold voltage, series resistance (all increasing at low-T)





Impurity Freeze-Out

- **77 K : weak freeze-out**
 - R_{SD} increases \Rightarrow LDD optimization
 - lateral field decreases \Rightarrow less impact ionization
- **30 K : strong freeze-out**
 - field-effect ionization (via V_G and V_D)
 - $I_D(V_G)$ curves may change according to V_D
- **SOI-like kink even in bulk MOSFETs**
- **Fully-depleted SOI MOSFETs**
 - naturally kink free
 - suppressed kink-related excess noise
- **Forget about body contacts**





Hot Carrier Injection

Causes

- Caused by large electric field at the drain of the MOSFET
- Significantly impacts NMOS more than PMOS since mobility, mean free path, ionization rate for $e^- \gg$ holes
- HCI is supposed to be max. when $V_{GS} = V_{DS}/2$ for NMOS [1]
- Low temperature operation of the device further degrades the device characteristics

Impacts

- With an increase in the drain voltage, HCI increases causing an increase in the reverse-biased body-drain diode current—this reduces the output impedance of the MOSFET
- For a given device and drain current, *lifetime* $\propto W \times (I_D)^k$, i.e. a wider device offers increased lifetime [2]
- No avalanche breakdown observed in SOI5 measurements for $V_{DS} = 5V$



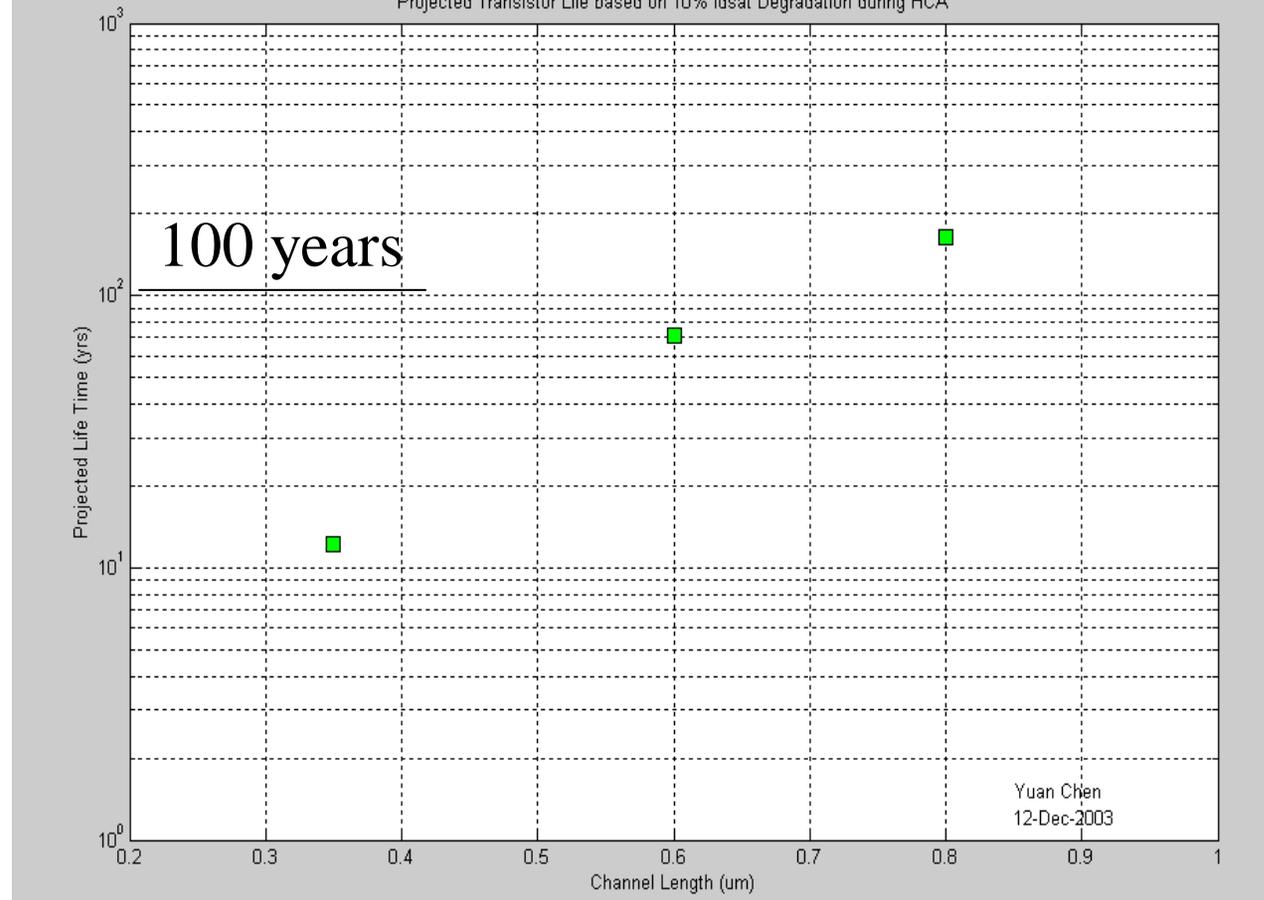
Modeling Life Cycle of CMOS MOSFETs function of L

- Anticipated life test of SOI CMOS Transistors

- **For digital application:**
 - **0.35 μm produces 12 years of life**
 - **0.6 μm produce 70 years of life**
- **For analog applications other parameters like Gm and Vth need to be evaluated**

Channel Length Dependence – I_{dsat}

Projected Transistor Life based on 10% I_{dsat} Degradation during HCA





Overview of Available SOI

Process & Vendor	Feature size	Operating voltage	High voltage option	Total Dose
Honeywell SOI4	0.8 μm	5 V	40 V LDMOS	2 Mrad
Honeywell SOI5	0.35 μm	3.3 V	20 V LDMOS	2 Mrad
Honeywell SOI6	0.25 μm	2.5 V		1 Mrad
Honeywell SOI7	0.15 μm	1.8 V		300 krad
Honeywell MOI5	0.35 μm	3.3 V	Thick oxide (5 V)	NA
IBM SOI CMOS	0.13 μm	1.2 V		NA
TSMC SOI CMOS	0.13 μm	1.2 V		NA



CMOS Device Design Considerations for Cold Temp CKTS

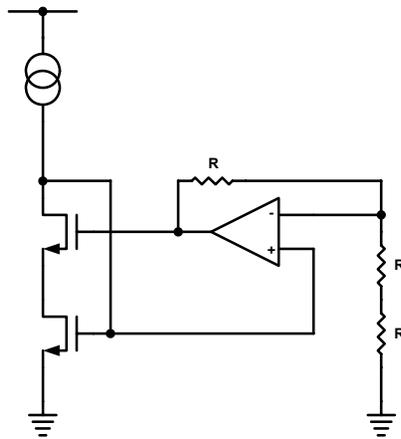


Summary of Important CMOS Temperature Characteristics		
Device Parameter	Variation with Temperature	Effect on Analog Circuit Performance
Threshold (V_{T_0})	<i>Increases with Decreasing</i> temperature	Reduced ICMR in amplifiers, reduced dynamic range for analog switches
Mobility (μ)	<i>Increases with Decreasing</i> temperature	Increased intrinsic speed and transconductance
Thermal Noise	<i>Decreases with Decreasing</i> temperature	Increase in dynamic range and achievable resolution
1/f Noise	Relatively <i>Constant</i> with temperature	Increased noise corner at low temperatures, reduces expected gains in dynamic range at low temperatures

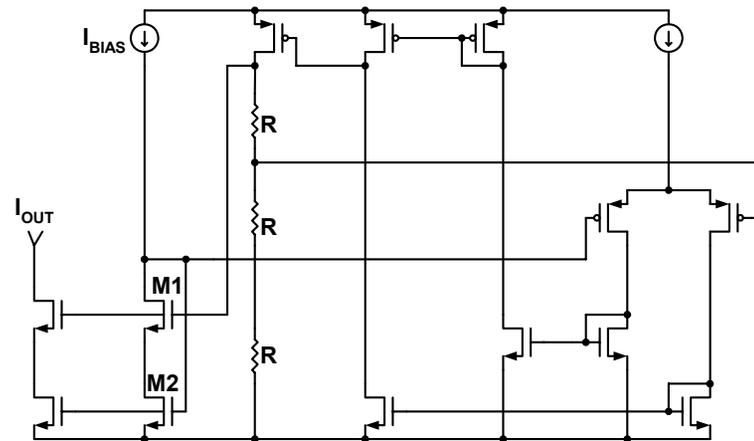


Robust LVCCM Biasing

- The V_{GS} -multiplier is a new LVCCM bias technique developed at Univ. of Tennessee
- The salient feature of the V_{GS} -multiplier is that it is guaranteed to maximize the V_{DS} on both the top and bottom device in the mirror – independent of bias current, temperature, or any other circuit or environmental characteristics



V_{GS} -Multiplier Concept

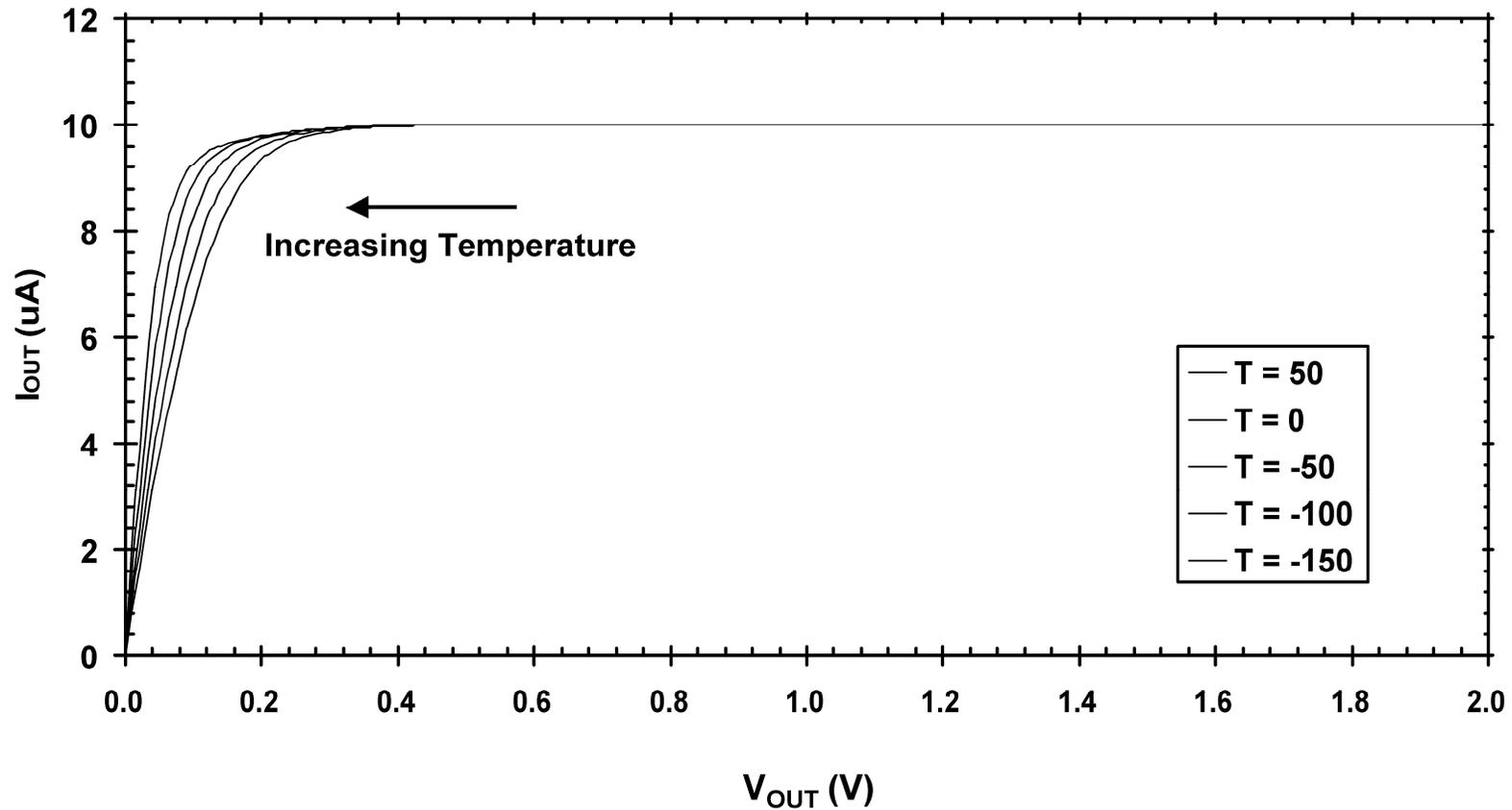


Transistor Level V_{GS} -Multiplier



LVCCM Biasing for Extreme Env.

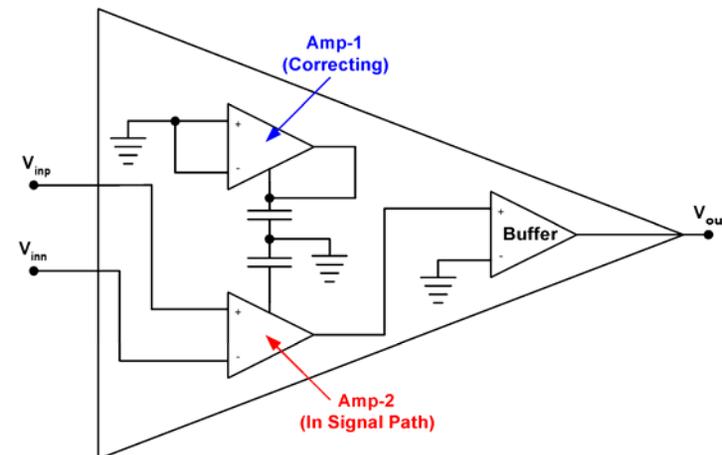
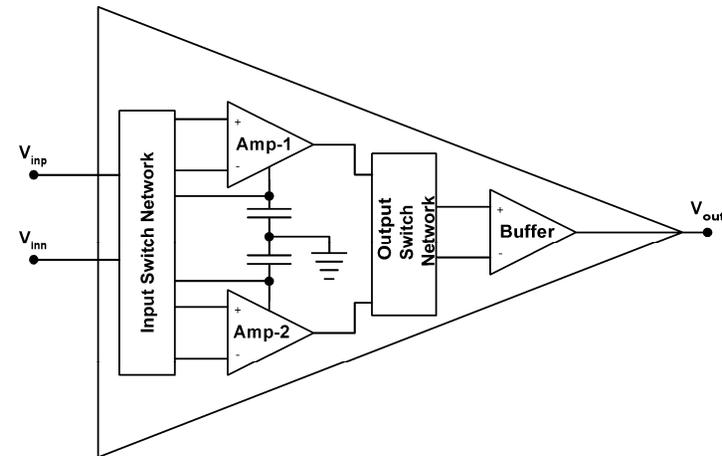
- Simulated performance over broad temperature range





Ping-Pong Op-Amp

- White noise is reduced at low temperatures, however $1/f$ noise is only weakly dependent on temperature, therefore the noise corner will increase with reduced temperature
- Ping-pong op-amps reduce $1/f$ noise by using auto-zeroing – thus they can increase dynamic range for systems with a high noise corner

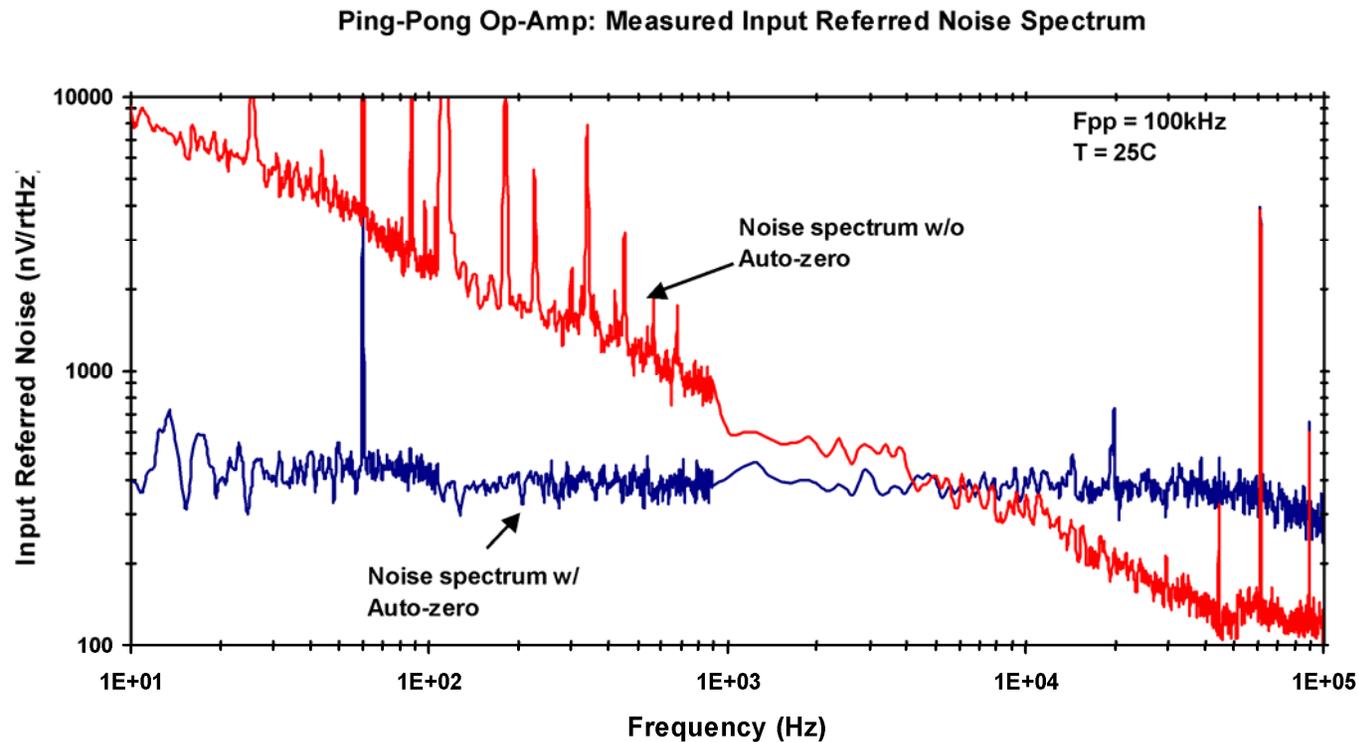




Ping-Pong Op-Amp

- **Plot showing measured noise-shaping of ping-pong op-amp**

- Ping-pong correction reduces the $1/f$ noise power because $1/f$ noise is correlated, however low frequency white noise is increased because of noise folding
- Net effect: Dynamic range is increased for systems where low-frequency noise dominates dynamic range (e.g. gated-integrator)

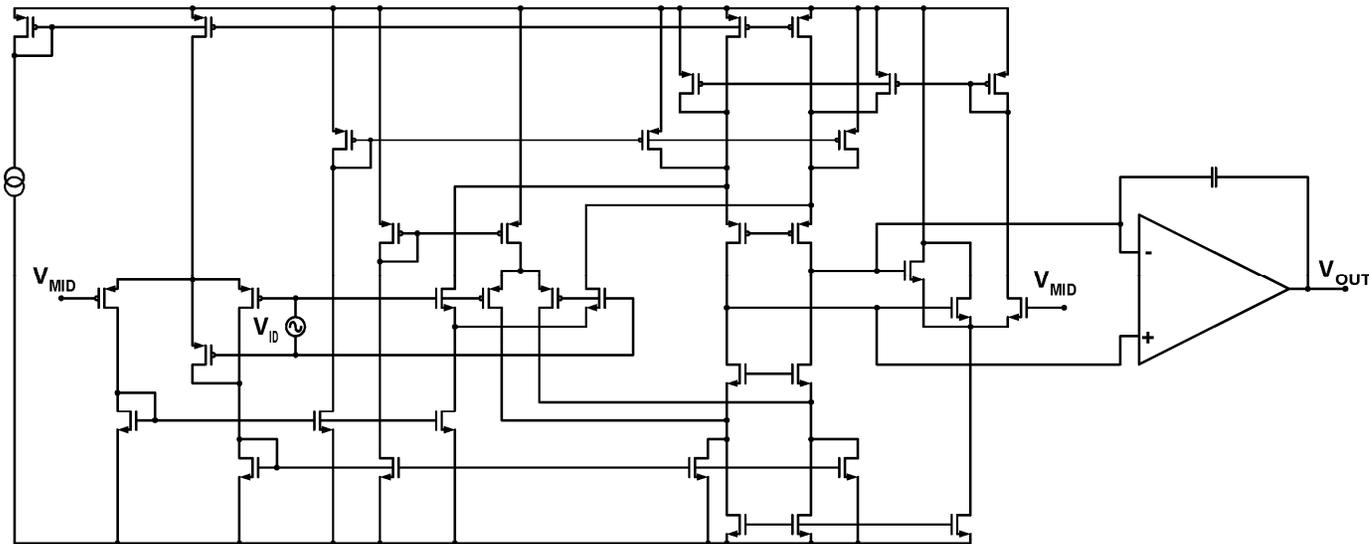




Rail-to-Rail I/O Op-Amp

- **Design Highlights**

- 1st stage is fully differential, rail-to-rail ICMR w/ regulated g_m and constant slew rate, CT CMFB
- 2nd stage is a Class-AB driver with low quiescent current for good power efficiency

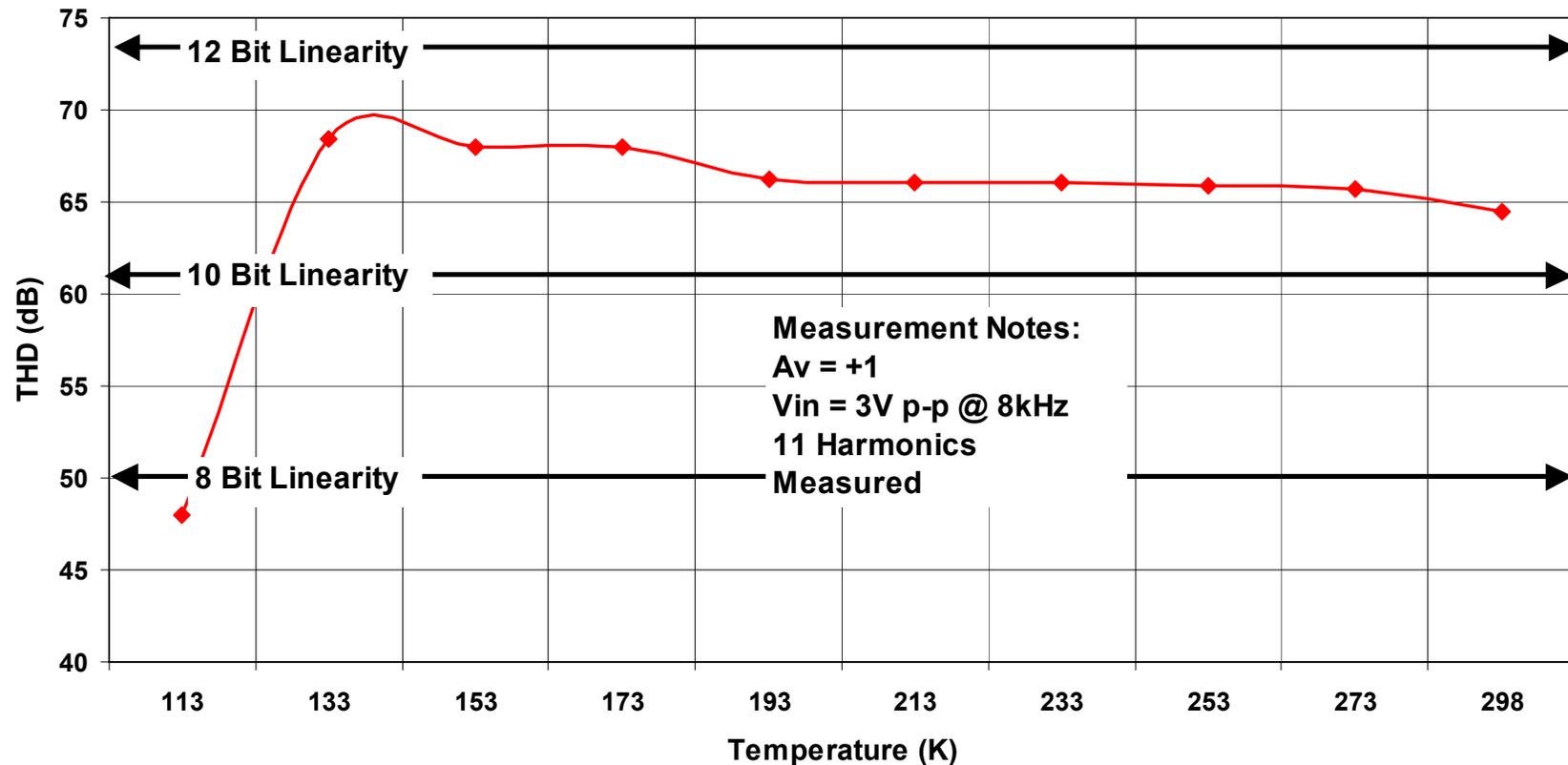


MOI5 Op-Amp Schematic (LVCCM biasing not shown)



Rail-to-Rail I/O Op-Amp

MOI5 Op-Amp : Measured THD vs. Temperature





Commercial Electronics For Extr. Env. Summary



- **COTS can provide functionality for a wider range of temperature, from 27°C to –175°C in the cold side. Mars and other NASA missions to cold environments may be able to use these COTS.**
- **Commercial foundries such as Honeywell PD SOI 0.35um technology + Cold temperature design rules can produce cold temperature specific mixed signal electronics**
- **Honeywell HT SOI CMOS offers integrated electronics solutions that work to > 200C**
- **For higher temperature environments, mass of the mission life is defined by the performance of the thermal system defines the life of the missions**