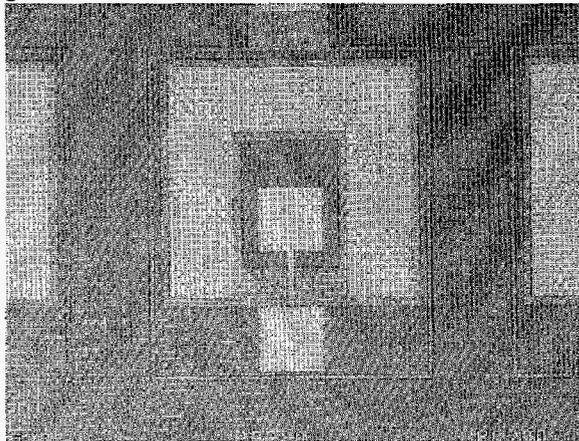


**A RADIATION-TOLERANT, LOW-POWER NON-VOLATILE MEMORY BASED ON SILICON NANOCRYSTAL QUANTUM DOTS.** L.D. Bell<sup>1</sup>, E. Boer<sup>2</sup>, M. Ostraat<sup>2</sup>, M. L. Brongersma<sup>2</sup>, R. C. Flagan<sup>2</sup>, H. A. Atwater<sup>2</sup>, J. deBlauwe<sup>3</sup>, and M. L. Green<sup>3</sup>, <sup>1</sup>Jet Propulsion Laboratory, 4800 Oak Grove Dr, Pasadena, CA 91109, <sup>2</sup>Caltech, Pasadena, CA 91125, <sup>3</sup>Lucent Technologies, Murray Hill, NJ 07974.

**Introduction:** Nanocrystal nonvolatile floating-gate memories are a good candidate for space applications - initial results suggest they are fast, more reliable and consume less power than conventional floating gate memories.[1,2] In the nanocrystal based NVM device, charge is not stored on a continuous polysilicon layer (so-called floating gate), but instead on a layer of discrete nanocrystals. Charge injection and storage in dense arrays of silicon nanocrystals in SiO<sub>2</sub> is a critical aspect of the performance of potential nanocrystal flash memory structures. The ultimate goal for this class of devices is few- or single-electron storage in a small number of nanocrystal elements. In addition, the nanocrystal layer fabrication technique should be simple, 8-inch wafer compatible and well controlled.

**Technical Products:** Formation of a nanocrystal aerosol is via the decomposition of silane at 950 C in an inert carrier gas, followed by an in-situ, pre-deposition thermal oxidation. This "discrete" method for aerosol synthesis allows unprecedented control of nanocrystal size and vertical positioning within the element gate stack. Dense ( $5 \times 10^{11} \text{ cm}^{-2}$ ), nearly coplanar nanocrystal layers have been obtained. We have then integrated nanocrystal layers in 0.20 micron nMOS-FETs to produce the first aerosol-nanocrystal floating-gate memory devices (Fig. 1). These devices exhibit threshold voltages of less than 5V with large threshold voltage shifts ( $\sim 2 \text{ V}$ ), sub-microsecond program times and millisecond erase times. No decrease



**Figure 1:** Scanning electron micrograph image of a nanocrystal floating gate memory test device.

in program/erase threshold voltage swing was seen during 100,000 program and erase cycles. Additional near-term goals for this project include extensive testing for radiation hardness and the development of artificial layered tunnel barrier heterostructures [3] which have the potential for large speed enhancements for read/write of nanocrystal memory elements, compared with conventional flash devices.

**NASA Relevance:** NASA deep-space missions will require increased autonomy and capability without increased mass and power. Breakthrough small, low-power memory technologies are required to address this requirement. Nanocrystal-based flash memories are based on few- or single-electron storage per nanocrystal, offering the ultimate in low-power, ultrasmall storage. Moreover, many deep-space missions will demand radiation-tolerant electronics; high-radiation environments are especially demanding for memory technologies, often requiring massive shielding. Missions to the Jovian system, such as the Europa Lander or Titan Explorer, will require breakthroughs in memory radiation tolerance. The discreteness of charge storage in isolated nanocrystals instead of large, continuous floating gate offers an intrinsic tolerance to total-dose radiation damage. Thus, the implementation of flash memory designs using nanocrystal charge storage is extremely promising as an inexpensive and reliable way to address these challenges.

Nanocrystal-based flash memory elements, combined with layered tunnel barriers, can also be combined to produce wavelength-tunable imaging elements. The novel properties of these tunnel barriers enable voltage-tunable control of detected wavelength, combined with monolithic storage of multiple image frames (using nanocrystal storage) within the same microdevice. The end product is an autonomous, versatile imager/memory array which approaches the absolute limits of miniaturization.

**References:** [1] Yano K., Ishii T., Hashimoto T., Murai F., and Seki K. (1994) *IEEE Trans. Electron. Devices*, 41, 1628-1638. [2] Tiwari S., Rana F., Hanafi H., Hartstein A., Crabbe E. F., and Chan K. (1996) *Appl. Phys. Lett.* 68, 1377-1379. [3] Likharev K. K. (1998) *Appl. Phys. Lett.* 73, 2137-2139.