



Jet Propulsion Laboratory
National Aeronautics & Space Administration
California Institute of Technology



Package Qualification and Reliability for Extreme Environment

by
Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
(818) 354-2059
Reza.Ghaffarian@JPL.NASA.Gov

JPL Outline

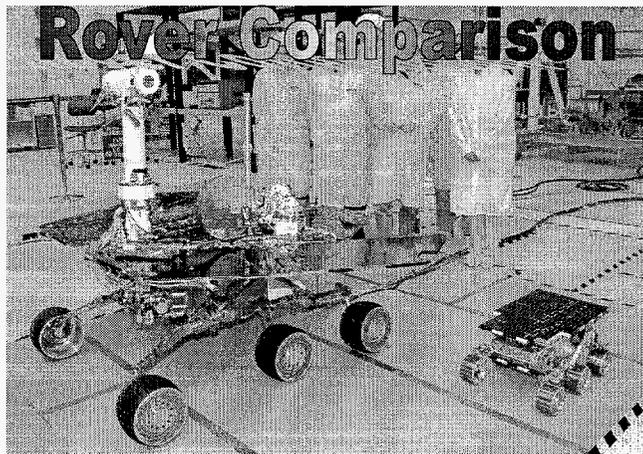


- Electronic Package Trend/Qual
 - Package shrink trends
 - Stack package trends
 - IPC 9701-9706, NASA Qual
- Why Cold
 - NASA needs
 - Package materials characteristics at cold
- Examples
 - PBGA/CCGA at hot/cold
 - Thermal cycle failure examples
- Conclusions

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Rover Comparison



Mars Exploration Rover
175 kg (385 lbs)
157 cm (5 ft) tall
9 cameras
3 spectrometers
4 magnets, 1 rock grinder

Sojourner Rover
11 kg (24 lbs)
32 cm (1 ft) tall
3 cameras
1 spectrometer

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Density Increase Approaches



- Bare die staking
 - Peripheral: wire bond, edge conductor connection
 - Area array, flip chip, stack with wafer using filled via
 - Systems on chip (SOC)
- Multi-chip Module (package)
- Conventional stack package
 - Peripheral lead
 - Wire-bond die stack (SIP)
- Area Array Package (SIP)
 - Peripheral
 - Bare die stack in CSP
 - Package stack
- Device density increase
- Package shrink (WLP)

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JPL 1st SiP Conf in Japan



Tessera Announces First Annual SiP Symposium In Japan

(November 24, 2004) San Jose, Calif.—Building on its successful second annual Technology Symposium held in San Jose, Calif. earlier this year, Tessera Technologies announces that it will take the first annual SiP Symposium to Tokyo, Japan.

Tessera's inaugural Technology Symposium in Japan will feature U.S.- and Japan-based semiconductor companies focused on achieving greater electronics miniaturization through the use of SiP technologies. The symposium will take place on January 18, 2005, the day before the opening of the IC Packaging Technology Expo in Japan

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IPC Qual Specs-I



- IPC 9701, Released Jan 2002
“Performance Test Methods and Qual Requirements for SMT”
 - Details on Thermal cycle test and acceptance
 - IPC 9701A- Lead free requirement

- IPC-JEDEC 9702- Released July 2004
“Monotonic Bend Characterization of Board-Level Interconnects”
 - Details on bend test to detect failure due handling, probe test, etc.

- IPC 9703, Draft August 2004
“Mechanical Shock Test Methods and Qual Req for SMT”
 - Details on mechanical shock and drop tests
 - Increase load/drop levels to failure
 - Use specific requirement

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IPC Qual Specs-II



- IPC 9704, Final Draft Feb 2005
“PWB Strain Gage Test Guidelines”
 - Solder joint failure due to mechanical loading during probe test
 - Limited to static load, dynamic will be covered later

- IPC 9705, Initial Draft Feb 2005
“Area Array Connector Testing and Reliability”
 - IPC 9701 and additional specific requirement for connectors

- IPC 9706, Initiated Oct 2004- Approved
“Guidelines on Lead-free Implementation for High Reliability Applications”
 - Data being generated by NASA-DOD-Industry on lead-free
 - Reliability data by industry

Roger Hoffmann



Qualification- IPC 9701



- IPC 9701, Released Jan 2002
 - IPC SM785- Guideline
 - No answer to the question of data for product application
 - Data comparison
 - IPC 9701
 - Details on thermal cycle test and acceptance

- Key Controls
 - Surface finish (OSP, HASL), thickness, 93 mil, NSMD, continuous monitoring, etc.

- Five Cycle Conditions
 - Preference 0/100°C

- Five number of thermal cycles
 - Preference 6,000 cycles

IPC 9701- “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments”

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IPC 9701 Temp Cycle Req



Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

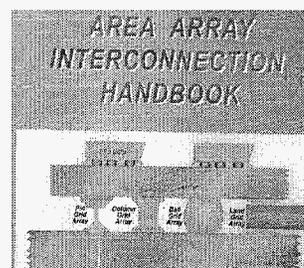
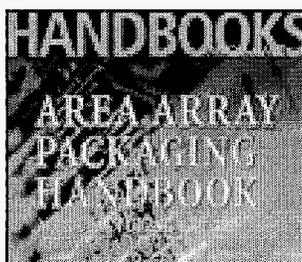
Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: TC1 TC2 TC3 TC4 TC 5	0°C ↔ +100°C (Preferred Reference) -25°C ↔ +100°C -40°C ↔ +125°C -55°C ↔ +125°C -55 °C ↔ 100°C
Test Duration Number of Thermal Cycle (NTC) Requirement: NTC-A NTC-B NTC-C NTC-D NTC-E	Whichever condition occurs FIRST: 50% (preferred 63.2%) cumulative failure (Preferred Reference Test Duration) or 200 cycles 500 cycles 1,000 cycles (Preferred for TC2, TC3, and TC4) 3,000 cycles 6,000 cycles (Preferred Reference TC1)
Low Temperature Dwell Temp. tolerance (preferred)	10 minutes +0/-10°C (+0/-5°C) [+0/-18°F (+0/-9°F)]
High Temperature Dwell Temp. tolerance (preferred)	10 minutes +10/-0°C (+5/-0°C) [+18/-0°F(+9/-0°F)]

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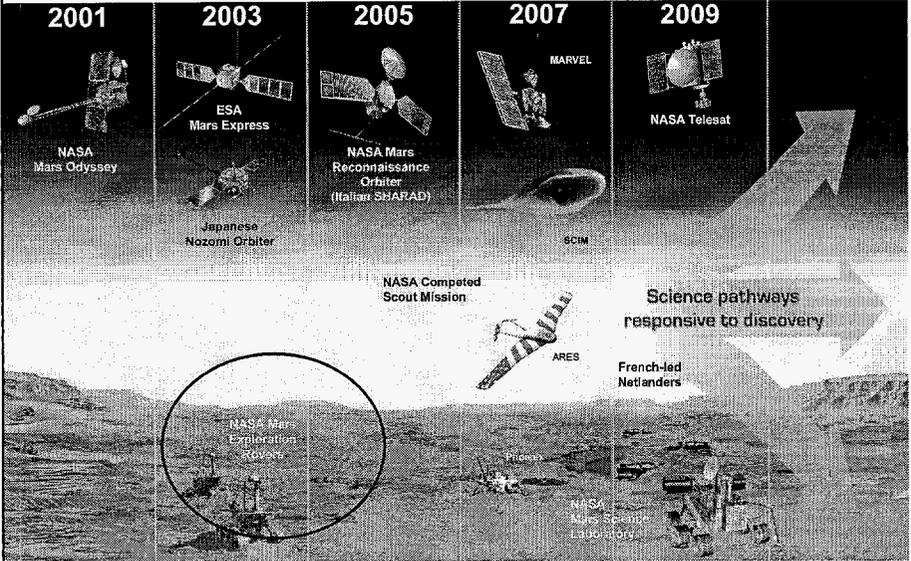
References



CHIP SCALE PACKAGING FOR MODERN ELECTRONICS



JPL **Mars Missions** 



2001: NASA Mars Odyssey

2003: ESA Mars Express, Japanese Nozomi Orbiter

2005: NASA Mars Reconnaissance Orbiter (Italiani SPARAD)

2007: MARVEL, SCIM

2009: NASA Telesat

Science pathways responsive to discovery

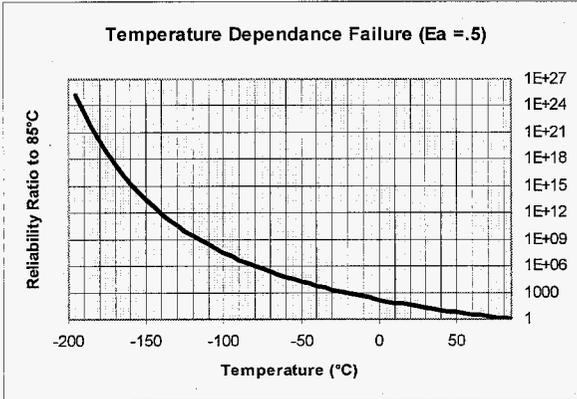
NASA Competed Scout Mission, ARES, French-led Netlanders, NASA Mars Exploration Rovers, NASA Mars Science Laboratory

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JPL **Effect of Temp** 

MTBF ~ Exp (Ea /K T)

- Ea Activation energy, 0.3-1.2 eV
- K is Boltzman's constant
- T is absolute temp



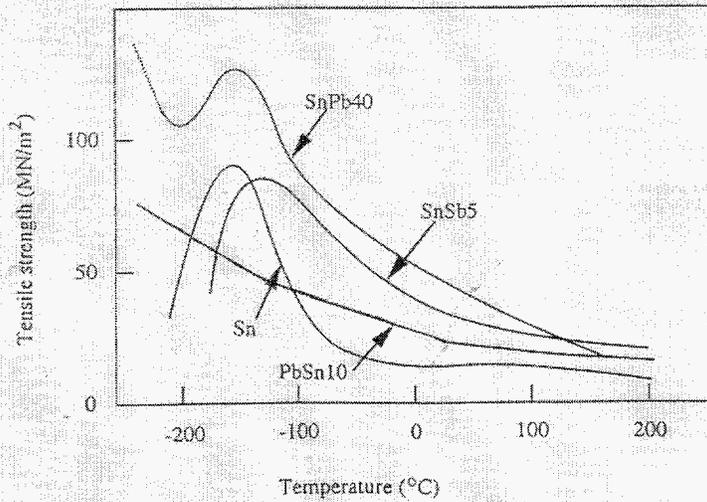
Temperature Dependence Failure (Ea =.5)

Reliability Ratio to 85°C

Temperature (°C)

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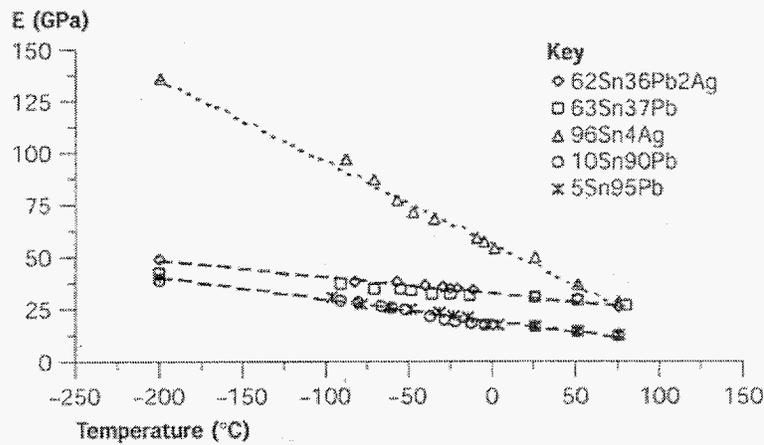
Solder Tensile strength Vs Temp



Source: Vianco 1993, Dasgupta 1991

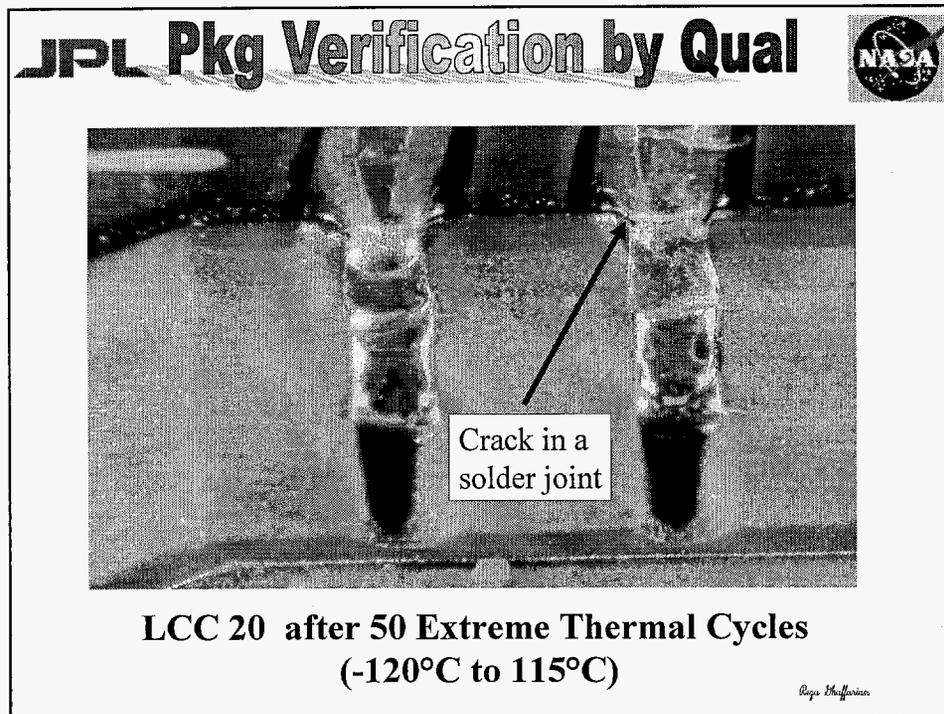
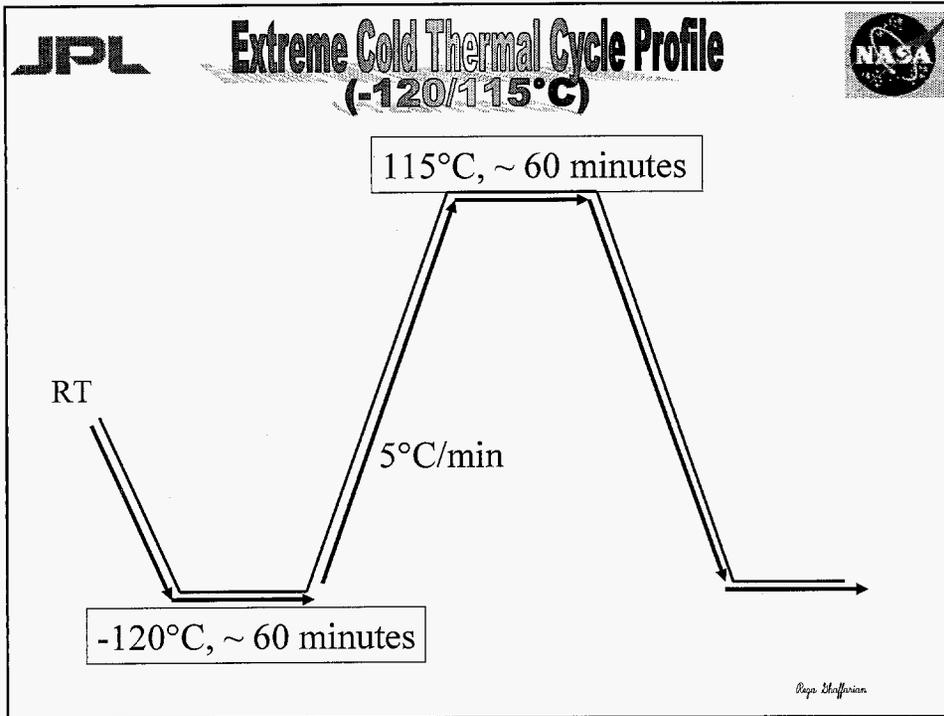
Raja Maffucci

Solder Yield Strength Vs Temp



Source: Jones, et al, International Symposium on Advanced Packaging

Raja Maffucci



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Summary



- **Electronic Pkg Miniaturization Continue!**
 - Area array packages, higher I/Os, lower pitches
 - SIP- Stack die packages are easier to implement
 - WLP, SOC, bare die still lag
- **Qualification for Thermal and Mechanical Shock**
 - IPC 9701- Thermal cycle now widely used, revision for lead free
 - IPC-JEDEC 9702 released and IPC 9703-9706 being developed
- **PQV to Address Benign and Harsh Mars Env.**
 - A large number of packages were qualified for Martian extreme cold environment (-120°C to 85°C)
 - Additional qualification for MSL
- **Lack cold data for NASA needs**
- **Need Efficient Qual/Insp Approaches to Detect New Failures for Advanced Packages & at Cold**

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Acknowledgments



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(NEPP)**



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Peter Hoffmann