Package Qualification and Reliability for Extreme Environment

by

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- Electronic Package Trend/Qual
  - Package shrink trends
  - Stack package trends
  - IPC 9701-9706, NASA Qual
- Why Cold
  - NASA needs
  - Package materials characteristics at cold
- Examples
  - PBGA/CCGA at hot/cold
  - Thermal cycle failure examples
- Conclusions
Mars Exploration Rover
175 kg (385 lbs)
157 cm (5 ft) tall
9 cameras
3 spectrometers
4 magnets, 1 rock grinder

Sojourner Rover
11 kg (24 lbs)
32 cm (1 ft) tall
3 cameras
1 spectrometer

- Bare die stacking
  - Peripheral: wire bond, edge conductor connection
  - Area array, flip chip, stack with wafer using filled via
  - Systems on chip (SOC)
- Multi-chip Module (package)
- Conventional stack package
  - Peripheral lead
  - Wire-bond die stack (SIP)
- Area Array Package (SIP)
  - Peripheral
  - Bare die stack in CSP
  - Package stack
- Device density increase
- Package shrink (WLP)
Tessera Announces First Annual SiP Symposium In Japan

(November 24, 2004) San Jose, Calif.—Building on its successful second annual Technology Symposium held in San Jose, Calif. earlier this year, Tessera Technologies announces that it will take the first annual SiP Symposium to Tokyo, Japan.

Tessera's inaugural Technology Symposium in Japan will feature U.S.- and Japan-based semiconductor companies focused on achieving greater electronics miniaturization through the use of SiP technologies. The symposium will take place on January 18, 2005, the day before the opening of the IC Packaging Technology Expo in Japan.
IPC 9704, Final Draft Feb 2005
“PWB Strain Gage Test Guidelines”
- Solder joint failure due to mechanical loading during probe test
- Limited to static load, dynamic will be covered later

IPC 9705, Initial Draft Feb 2005
“Area Array Connector Testing and Reliability”
- IPC 9701 and additional specific requirement for connectors

IPC 9706, Initiated Oct 2004- Approved
“Guidelines on Lead-free Implementation for High Reliability Applications”
- Data being generated by NASA-DOD-Industry on lead-free
- Reliability data by industry

IPC 9701, Released Jan 2002
- IPC SM785- Guideline
  - No answer to the question of data for product application
  - Data comparison
  - IPC 9701
    - Details on thermal cycle test and acceptance

Key Controls
- Surface finish (OSP, HASL), thickness, 93 mil, NSMD, continuous monitoring, etc.

Five Cycle Conditions
- Preference 0/100°C

Five number of thermal cycles
- Preference 6,000 cycles

IPC 9701- “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments”
<table>
<thead>
<tr>
<th>Test Condition</th>
<th>Mandated Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycle (TC) Condition:</td>
<td>TC1 0°C ↔ +100°C (Preferred Reference)</td>
</tr>
<tr>
<td>TC2</td>
<td>-25°C ↔ +100°C</td>
</tr>
<tr>
<td>TC3</td>
<td>-40°C ↔ +125°C</td>
</tr>
<tr>
<td>TC4</td>
<td>-55°C ↔ +125°C</td>
</tr>
<tr>
<td>TC5</td>
<td>-55°C ↔ 100°C</td>
</tr>
<tr>
<td>Test Duration</td>
<td>Whichever condition occurs FIRST: 50% (preferred 63.2%) cumulative failure (Preferred Reference Test Duration) or</td>
</tr>
<tr>
<td>Number of Thermal Cycle (NTC) Requirement:</td>
<td></td>
</tr>
<tr>
<td>NTC-A</td>
<td>200 cycles</td>
</tr>
<tr>
<td>NTC-B</td>
<td>500 cycles</td>
</tr>
<tr>
<td>NTC-C</td>
<td>1,000 cycles (Preferred for TC2, TC3, and TC4)</td>
</tr>
<tr>
<td>NTC-D</td>
<td>3,000 cycles</td>
</tr>
<tr>
<td>NTC-E</td>
<td>6,000 cycles (Preferred Reference TC1)</td>
</tr>
<tr>
<td>Low Temperature Dwell</td>
<td>10 minutes</td>
</tr>
<tr>
<td>Temp. tolerance (preferred)</td>
<td>+10/-10°C (+18/-18°F)</td>
</tr>
<tr>
<td>High Temperature Dwell</td>
<td>10 minutes</td>
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</table>

CHIP SCALE PACKAGING
FOR MODERN ELECTRONICS
MTBF ~ Exp (Ea /K T)

- Ea Activation energy, 0.3-1.2 eV
- K is Boltzmann’s constant
- T is absolute temp

Temperature Dependence Failure (Ea = .5)

Reliability Ratio to 85°C

Temperature (°C)
**Solder Tensile Strength Vs Temp**

Tensile strength (MN/m²) vs Temperature (°C)

Source: Vianco 1993, Dasgupta 1991

**Solder Yield Strength Vs Temp**

E (GPa) vs Temperature (°C)

Key:
- ▲ 62Sn36Pb2Ag
- □ 63Sn37Pb
- △ 96Sn4Ag
- ◊ 105Sn90Pb
- X 5Sn95Pb

Source: Jones, et al, International Symposium on Advanced Packaging
LCC 20 after 50 Extreme Thermal Cycles
(-120°C to 115°C)
Summary

- Electronic Pkg Miniaturization Continue!
  - Area array packages, higher I/Os, lower pitches
  - SIP- Stack die packages are easier to implement
  - WLP, SOC, bare die still lag
- Qualification for Thermal and Mechanical Shock
  - IPC 9701- Thermal cycle now widely used, revision for lead free
  - IPC-JEDEC 9702 released and IPC 9703-9706 being developed
- PQV to Address Benign and Harsh Mars Env.
  - A large number of packages were qualified for Martian extreme cold environment (-120°C to 85°C)
  - Additional qualification for MSL
- Lack cold data for NASA needs
- Need Efficient Qual/Insp Approaches to Detect New Failures for Advanced Packages & at Cold

Acknowledgments

NASA Electronic Part and Packaging (NEPP)

In-kind contributions of JPL Consortia team members

Support of MSL TCRE Team