

# Lead Free 0201 Assembly and Thermal Cycle/Aging Reliability

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## 1. Abstract

The many challenges with 0201 passive component assembly can be attributed to the solder paste volume, pad design, aperture design, board finish, type of solder paste, pick-and-place, and reflow profile. A Design-of-Experiment (DOE) study was carried out to investigate the effects of these parameters on assembly defects and reliability.

The test vehicles consist of pad layouts for 2000-0201 components. Five different test vehicles were used, with the same pad layout and non-solder mask defined pads, with HASL, ENIG, Pure Tin, Immersion Silver and OSP finish. Four different pad shapes are designed on each of the test vehicles (rectangular, oval, modified home plate and double trapezoid). The pad areas for all four shapes are maintained the same. Pads were oriented both in the horizontal and vertical directions. Electroformed 3-mil and 4.65 mil thick stencils were used for printing the solder paste. The stencil was designed to obtain two distinct aperture-pad combinations (matched and unmatched). Three solder paste types (tin-lead and anti-tombstoning and lead free) were used in this investigation.

Two test vehicles assembled for each experimental run, one with resistors and the other with capacitors, provided an understanding of the difference in the process for these two common passive devices. This paper discusses in detail the influence of a few key parameters and defects associated with the 0201 component using both leaded and lead-free solder alloys. A large number of these assemblies were subjected to isothermal aging at 150°C and thermal cycling in the range of -55 to 100°C to establish their reliability. Shear tests were carried out at various aging intervals up to 500 hours to determine the effects of aging damage on strength relative to virgin assemblies. Similarly, shear test data generated before and after 1500 cycles and data for ENIG and ImAg are compared. Weibull plots are given for reliability to establish solder joint fatigue behavior for the lead free assemblies compared to lead-based solder as well as data correlation for various sets of data. In addition, photomicrographs taken using an optical microscope at intervals during thermal cycling to establish damage progress are given. Scanning electron microscopy (SEM) analysis before and after cross-sectioning are also performed to reveal microstructural changes and intermetallic formation at 1500 thermal cycles are also included.

Key words: 0201 assembly, lead-free process, lead-free surface finish, modified apertures, thermal aging, thermal cycle, isothermal aging, shear load

## 2. Background

### 2.1 Discrete Passive Shrink Trends

Passives are used throughout electronic systems to provide the functions of resistance, capacitance and inductance. There are more than 10 discrete passives used for every active component in a typical system. Passives account for 90 percent of components, 40 percent of board area and 30 percent of solder joints in typical systems. The majority of passives is still discrete ceramic based and of standard outline. The subject of manufacturing issue and reliability of recently introduced tiny 0201s passive components have been the subject of many papers including a comprehensive paper by these authors and to be published in Microelectronic Reliability Journal[1-4]. Figure 1 compares sizes of previous types of passive relative to each other and also include a comparison of the 0201 component to a ball point pen. Figure 2 shows the market project for use of this and its previous generation indication that the market share for this component size is rapidly increasing.

In 1977, a typical passive component measured 3.2 mm x 1.6 mm (1206) in size. Ten years later in 1987, 0805 passives had become the most common with a size of 2.0 mm x 1.25 mm. The end of the millennium saw the 0603 passive measuring 1.6 mm x 0.80 mm claiming the largest usage; and 0402 passives, at 1.0 mm x 0.50 mm, were becoming the most popular size until recently. The 0201 passives, which until recently were the smallest passives in production, have dimensions of only 0.60 mm x 0.30 mm. Compared to 0402s, 0201s are about four times smaller in area and nearly five times lighter, which makes them attractive particularly for small portable systems. The newly introduced 01005 passives [5] are even smaller than 0201 and have 0.4mm x 0.2mm, respectively.

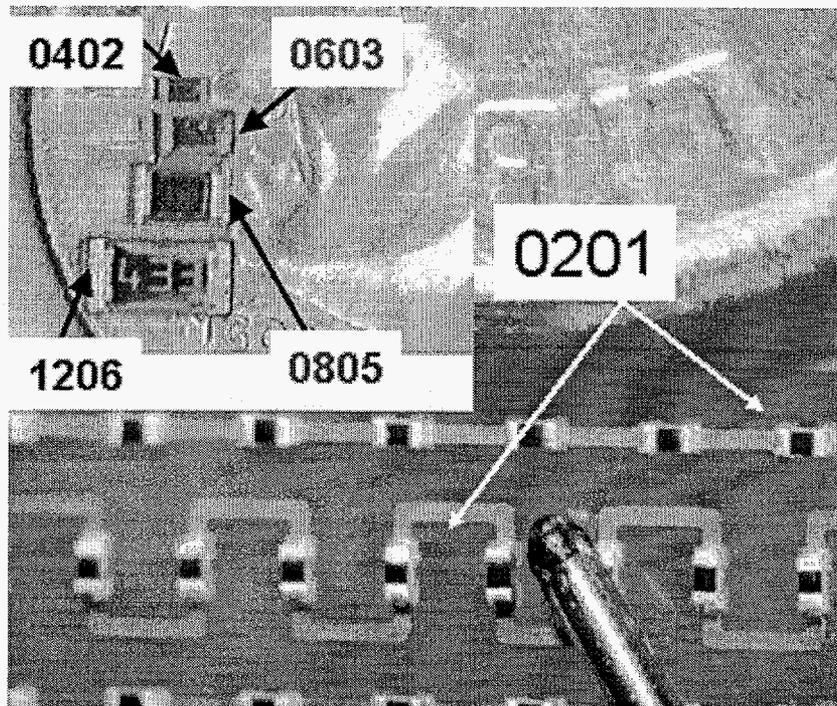


Figure 1 Size comparison of tiny 0201 discrete passive with a dime and pen tip

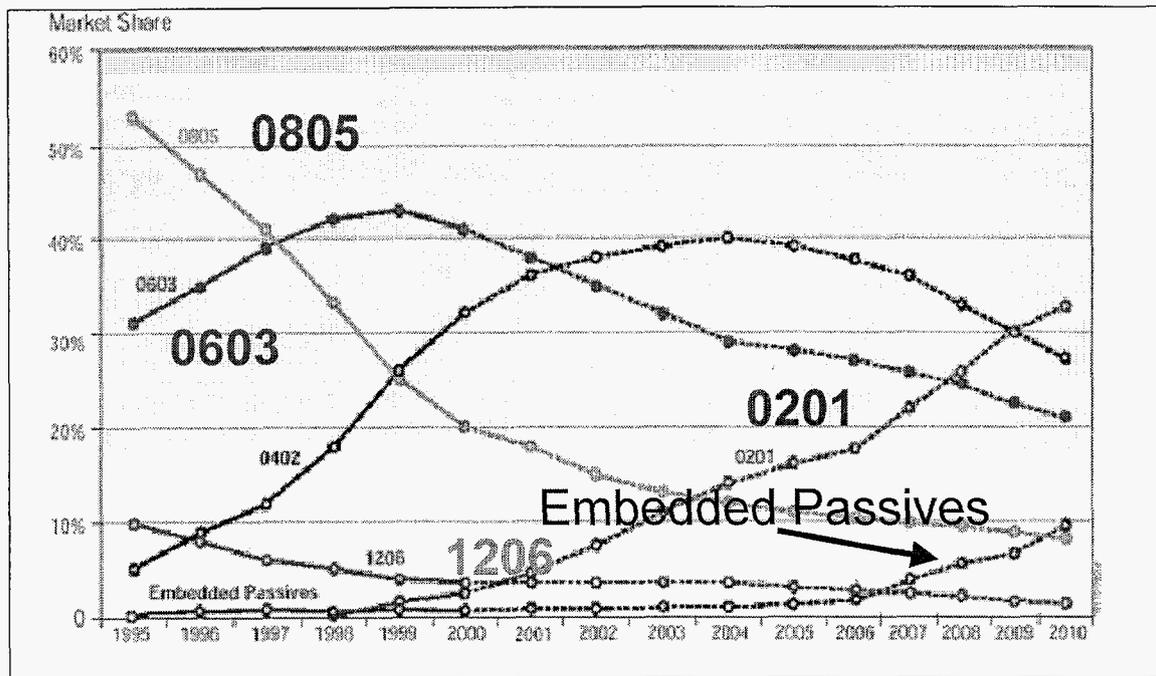
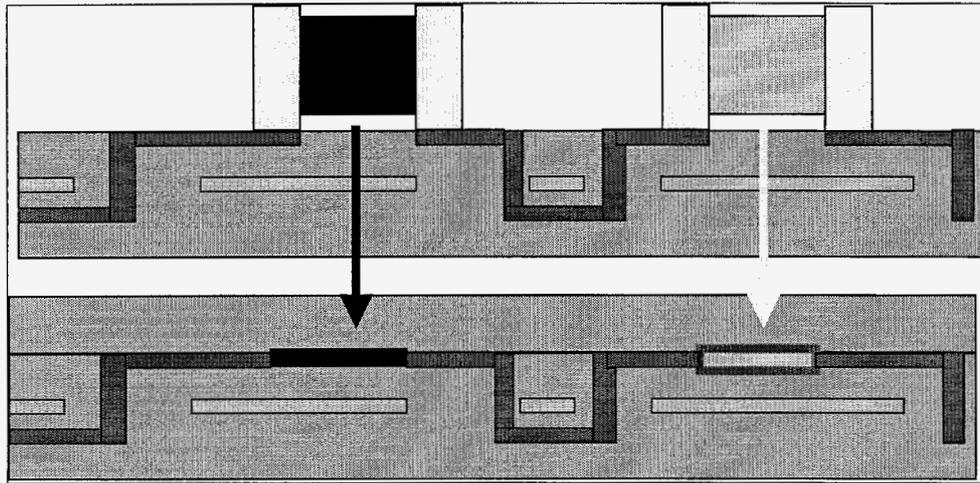


Figure 2 Market share of passives, growth of 0201 and embedded passives (Source: Prismark)

All electronic systems continue to be subjected to the trend of added functionality in a shrinking package technology. This trend is enabled for the most part by the shrinking evolution in feature size of silicon integrated circuits (ICs). Unfortunately, passive components have not kept up with ICs in this regard. Peripheral passive components are not as functionally space efficient as ICs and are seen as one of the major roadblocks in increasing the functional density of electronic systems. Clearly, the need for functional density will force designers to look at creative packaging alternatives. If the historical rate of passive component density continues, by 2010 it is reasonable to expect passive component densities of 20 to 30 passives/cm<sup>2</sup>.

## 2.2 Passive Embedded into Package

Integrated passive devices, where arrays of resistors or capacitors are swept into a component (or a board), have also gained in popularity. Figure 3 shows schematically discrete passives on the surface and between the build up layers [6]. These devices have been used by the computer industry for some time as an effective way to implement resistors at a high I/O port interface. However, these devices are only available for arrays of standard values or commonly used functional blocks. Customized designs are expensive and offer a limited supply base. Still, the resistor, capacitor or inductor value of a discrete is very much a function of physical size. The inability to create high value embedded devices in a space efficient manner puts limitations on the amount of integration possible. Also, most embedded advances will continue to suffer, primarily due to component density and tolerance limitations when compared to discrete passives. The tolerance of most discrete chip resistors is in the range of 1%, so designing to a possible 15% or more variation is not an attractive proposition.



**Figure 3 Schematic demonstration of discrete and embedded passives**

### **2.3 Embedded Passive into Printed Wiring Board (PWB)**

Embedded passive (EP) technologies introduce new materials and processes into PWB fabrication with the goal of reducing component part count through the removal of surface mount components. This is accomplished by embedding equivalently functional resistors, capacitors and inductors within the inner-layers of the PWB in place of traditionally surface-mounted passive components. Since the internalized, embedded devices require no solder joints, the principal failure mode of assemblies, solder joint failure, is reduced. Other advantages include:

- Improved electrical properties through additional termination and filtering opportunities and reduced length of electrical connections
- Reduced cost through decrease in board assembly operations
- Increased product quality through the elimination of incorrectly attached devices
- Decreased board area due to reduction in the number of discrete passives
- Decreased wiring requirements due to the integration of resistors and bypass capacitors into the board
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size

However, there are also disadvantages such as:

- Decrease in reliability because of emerging technology and difficulties with inspection
- Decrease in assembly level rework
- Decrease in overall assembly yield and increase in board cost per unit area

### **3. Literature Survey on Key 0201 Assembly/Reliability**

For implementation of 0201, assembly processes must be evaluated and optimized for several key parameters including the following:

- Pad design and surface finish for PWB
- Solder paste selection
- Stencil design and solder paste print parameters
- 0201 placement
- Reflow profile for selected solder

- Defect characterization
- Inspection
- Rework
- Reliability evaluation

A number of investigators [2-4, 7] have studied one or more of these parameters and recommend methods for SMT assembly process improvement, but none have a comprehensive investigation that also cover extensive reliability data comparison. In what follows, a brief literature review is given both for manufacturing and their associated defects as well as environment test results.

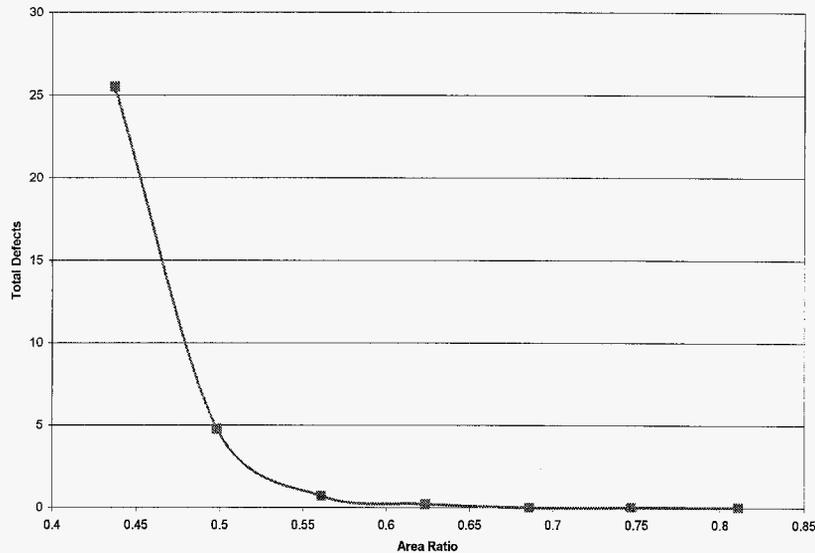
### **3.1 Pad Design**

At this time, there is no universally accepted PWB pad design for 0201 discrete components. Pad distance is another parameter that is critical and needs to be considered. The commonly used pad designs are: square, rectangle, extended half circle, oval, and trapezoid. A few of these pad designs were considered in an experimental evaluation in order to determine the pad design that induces minimum manufacturing defects. The PWB surface finish is another factor that needs to be considered during manufacturing process optimization.

### **3.2 Solder Paste Type and Stencil Design**

Solder paste type and stencil design are two other key printed factors in creating a robust 0201 assembly process. The correct amount of solder and its consistency can help significantly to minimize the production of the most common defects such as “tombstoning”. Consistency in the amount of paste is critical since tombstoning occurs due to the introduction of an imbalance in surface tension forces during the reflow process. If the solder paste volumes deposited on two pads differ, then the solder paste will reflow at different rates inducing two different surface tensions at the time of reflow when the part is floating on molten solder. This imbalance in forces causes the 0201 component to stand up or tombstone. Because the 0201 component has extremely small mass, even a small amount of variation in solder paste volume can bring about enough surface tension force to pull the part upward. The other major cause of tombstoning is a component that is placed off center so that more of the component is on one pad than the other.

Stencil design, and its corresponding solder paste transfer efficiency, is the next critical parameter on printing the correct amount of paste onto a PWB through a small stencil aperture (orifice). Transfer efficiency is a measure of the amount of paste in the aperture that transfers onto the PWB pads. Stencil design and type are important factors in determining the transfer efficiency of a particular solder paste. Smaller stencil apertures require the highest possible solder paste transfer efficiency. The stencil area ratio is shown to be an even more critical parameter for paste efficiency because of the small opening. Area ratio is the ratio between the areas of the stencil opening to the area of the wall of the stencil aperture (aperture area/wall area). Figure 4 shows [7] that the number of total defects remains relatively constant for an area ratio of 0.65 and greater. There is a sharp increase in the number of defects for the ratios of 0.5 and 0.45.



**Figure 4 Total defects as a function of area ratio [7]**

### 3.3 Common Defects

The most common defects for the 0201 assembly process in addition to missing components are:

- Tombstones
- Solder Bridges
- Solder Beads

As noted in the previous section, tombstoning defects become prevalent with inconsistent solder paste volume on each of the 0201 pads. Stencil design and solder paste selection are critical as well as the component placement.

Solder bridging is a common defect in fine pitch assembly process including 0201. The 0201 is a small component and it is generally a requirement to assemble them in a densely packed area on a PWB in order to take advantage of less board real state.

Several of the same factors that influence tombstoning and solder bridging also influence the creation of solder beads. Key factors in reducing solder beading are to print the solder paste accurately, evenly, and consistently and to place the component squarely and evenly onto the printed paste. This can also be reduced by minimizing the amount of solder under the device.

### 3.4 Reliability

Most literature data concerns reducing manufacturing defects in order to increase yield rather than providing data on reliability. Reliability data represented by cycles-to-failures of assembled 0201 parts fabricated under several design and process conditions were presented by Baldwin, et al [7] and are shown in Figure 5. In this Figure, the x-axis is the number of cycles while the y-axis is the percent of the 0201 devices that have failed. The thermal cycle was over the range of -40 to 125°C with a 20 minute cycle. The first failure was found to occur between 1500 and 2000 cycles.

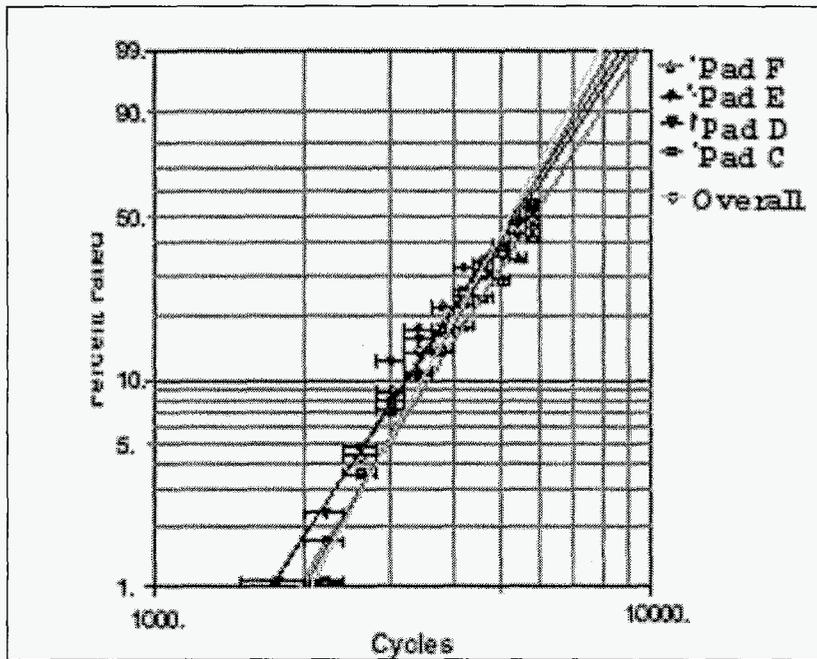


Figure 5 Cycles to failure for passives with different pad configurations [7]

#### 4. 0201 Process and Defects

This section discusses a summary of the effect of the type of solder paste, board finish and pad-aperture shape on 0201 assembly process defects, including both tin-lead and lead-free solder pastes and lead-free surface finishes. A design of experiment (DOE) test matrix was used to investigate the effects of various parameters on defect formation and reliability. Emphasis, however, is placed on environmental test results including thermal aging and thermal cycling represented by microstructural changes as well as shear testing.

##### 4.1 DOE Manufacturing Parameters

Based on the literature survey, the parameters considered for this experimental study were:

- Five surface finishes, hot air solder leveling (HASL), organic solder preservative (OSP), ENIG, immersion Ag, and Sn
- Tin-lead, lead-free and anti-tombstoning solder pastes
- Stencil thickness of 3 and 4.65 mils and three modified aperture shapes

Table 1 summarizes the DOE with variables considered in this investigation. The process parameters were kept constant for all the experimental runs. The experimental runs were executed in three groups, based on the solder paste type, in order to minimize the changeover time for the experiment. For each experiment run, a total of 30 test vehicles (TVs) were fabricated. Ten TVs were solder paste print only for paste quality and inspection, 10 were assembled with the 0201 resistors, and another 10 with capacitors.

Each TV had 240 non-solder mask defined (NSMD) rectangular pads with dimensions and spacing as shown in Table 2. The pads were equally distributed in the horizontal and vertical orientations. Five different types of test vehicles, with the same pad layout, with varying pad finishes (HASL, ENIG, pure Sn, immersion Ag and OSP) were used to investigate the effect of varying surface

finishes. Two test vehicles were assembled for each experimental run, one with zero-ohm lead-free resistors and the other with lead-free capacitors. The components had tin surface finish.

**Table 1. Phase 1 DOE Parameters**

<b>Factors</b>	<b>Levels</b>				
<b>Surface Finish</b>	HASL	ENIG	ImSn	ImAg	OSP
<b>Pad shape</b>	MHP	DT	Oval	Rectangular	
<b>Aperture Shape</b>	MHP	DT	Oval	Rectangular	
<b>Aperture size</b>	80%		90%		100%
<b>Stencil Thickness</b>	3mils (75 $\mu$ m)			4.65mils (116.25 $\mu$ m)	
<b>Solder Paste</b>	Anti-tombstone		Lead-free	Tin-Lead (Sn/Pb)	
<b>Orientation</b>	Vertical			Horizontal	
<b>Component</b>	Resistor			Capacitor	
MHP- Modified Home Plate Design					
DT- Double Trapezoid Design					

#### 4.2 Stencil Design, Printing, and Placement

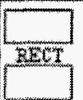
Electroformed 3 mil and 4.65 mil thick stencils were used in this experiment. The stencil design had four different aperture shapes, with constant print area, irrespective of the stencil thickness (see Table 2). This means that for a given stencil thickness, the ideal theoretical volume was designed to be constant for the four aperture shapes. Three different no-clean solder pastes were used in this experiment. These included the anti-tombstoning (62.6Sn37Pb0.4Ag), tin-lead (63Sn37Pb) and lead-free (95.5Sn3.8Ag0.7Cu) solder pastes with Type 4 solder particles (20-38 $\mu$ m). The percent metal content in the pastes ranged from 89-90.

Optimum print process parameters were obtained after carrying out trial runs for each paste. Visual inspection was performed to determine signs of film formation on the stencil and how solder paste was deposited on the center of pads. Then, these two parameters were considered as indicators for process optimization.

#### 4.3 Solder Reflow Process

As per the recommendations of the solder paste manufacturer, ramp-to-spike profiles were used for all three pastes. A seven-zone forced convection oven under atmospheric air condition was used. Table 3 provides details of the reflow profile stages temperature and time for the tin-lead and lead free solder pastes.

**Table 2. Pad/Aperture Shape and Dimension**

Shape	Pad Dimensions			Aperture Characteristics											
				100%				90%				80%			
	L	W	S	L	W	S	AAR for 3mils 4.65mils	L	W	S	AAR for 3mils 4.65mils	L	W	S	AAR for 3mils 4.65mils
 MHP	13	9	11	12	8	12	0.76 0.49	10.8	7.2	12.8	0.68 0.44	9.6	6.4	13.6	0.6 0.39
 DT	13	10.5	11	12.5	8	13.5	0.64 0.41	11.3	7.2	14.3	0.57 0.37	10	6.4	15.1	0.51 0.33
 OVAL	13.4	9	10.4	12.8	8	12	0.8 0.52	11.6	7.2	12.8	0.72 0.46	10.2	6.4	13.6	0.64 0.41
 RECT	12.5	8	11	11.4	7	11	0.72 0.47	10.3	6.3	12.7	0.65 0.42	9.1	5.6	13.4	0.58 0.37
L-Length, W-Width, S-Spacing			(All units are in mils (0.001") unless otherwise mentioned.)												

**Table 3 Reflow process parameters**

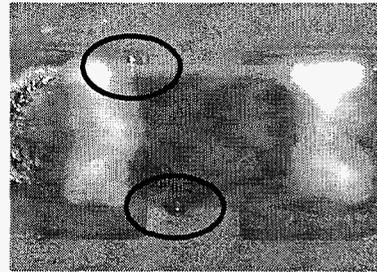
Reflow Process Parameters	Anti-Tombstoning & Lead Based Paste	Lead Free Paste (SAC alloy)
Peak Temperature	219°C	244.7°C
Time above Liquidus	59.16 sec	56.87 sec
Ramp Rate	1.97°C/sec	1.88°C/sec

#### 4.4 Manufacturing Defect Types

The assembled boards were inspected for workmanship defects using a manual vision inspection system. The various defects that were expected to occur include tombstoning, draw bridging, solder beading, component skewing, and insufficient solder (missing components). The number of defects and types was recorded for each experimental run (one test vehicle for resistors and one for capacitors), each having various pad-aperture combinations, pad surface finish, stencil thickness, and paste type. The number of defects was converted into percent defects based on the total number of component occurrences on each test vehicle. This percent defect data was used to analyze the test results. Figure 6 shows typical optical photomicrographs of defects observed after assembly.



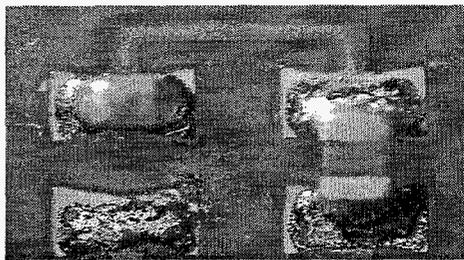
**Insufficient solder joint**



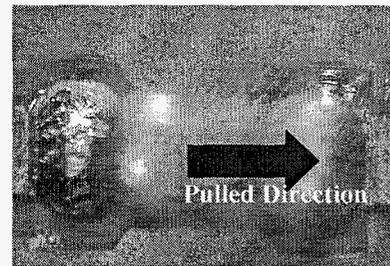
**Solder Beading  
(solder ball)**



**Component Skewing**



**Tombstoning**



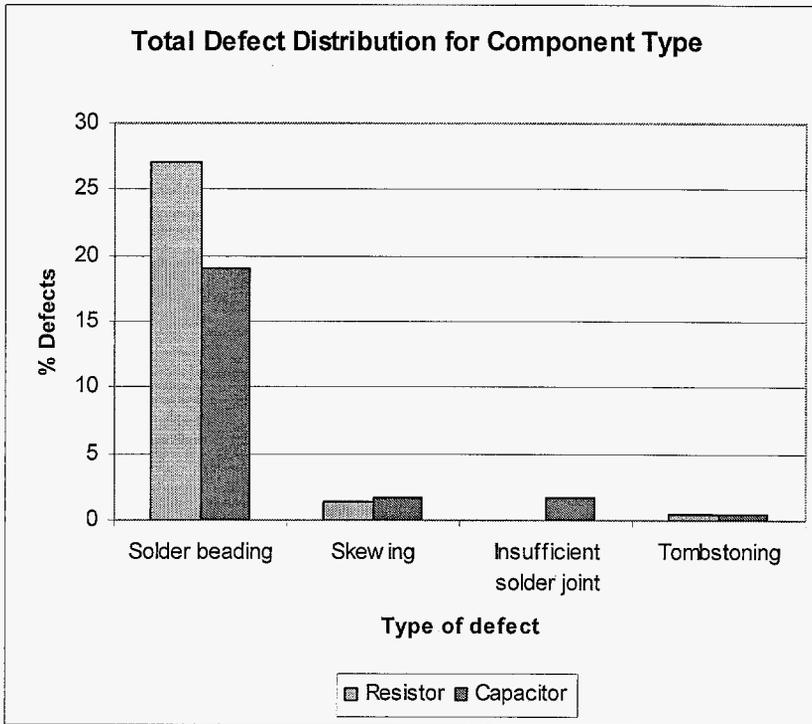
**Draw Bridging**

**Figure 6 Optical photomicrographs of typical defects after assembly**

#### 4.5 Defects and distribution

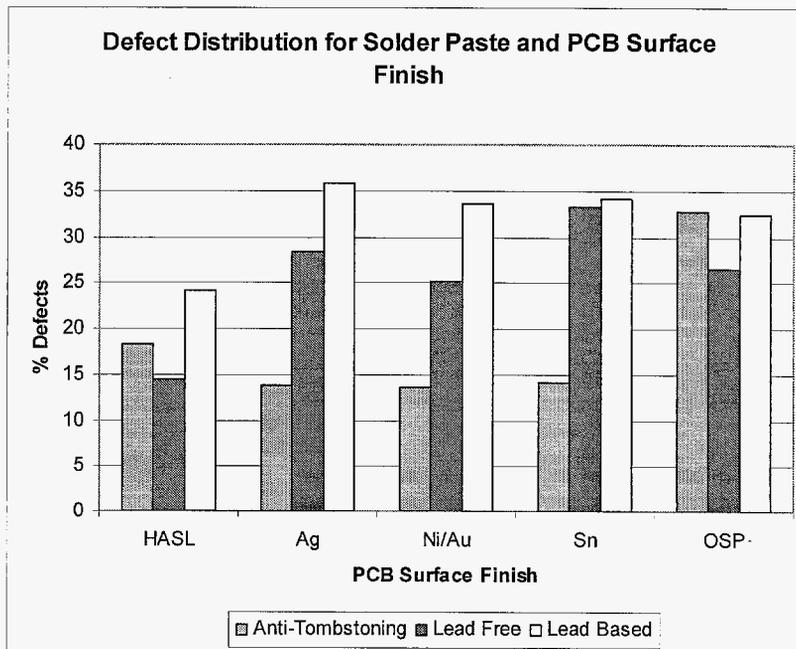
The total percentage of defects and their types for the entire DOE study are shown in Figure 7. It is evident that solder beading dominates the percentage of defects by an order of magnitude compared to the other defects. Insufficient solder joint (missing components) for capacitors was due to an error in one of the experimental runs which was immediately corrected to avoid further recurrence. Since this was a mishap in process, this defect was not considered in the analyses.

One significant outcome of the experiment was the considerable reduction in the occurrence of tombstoning. Lack of significant tombstoning clearly indicates that most of the solder paste and surface finish combinations considered in the study were in relatively optimized conditions, especially selection of stencil thickness, which plays a critical role. Data reveal that the few occurrences of tombstone defects were for PWBs with immersion silver finish when using anti-tombstoning or tin-lead solder paste. No occurrence was detected with the lead-free paste.



**Figure 7 Total defect distribution for component type**

Figure 8 shows the total defect distributions based on the combination of solder paste and surface finishes. The chart clearly reveals that the Sn/Pb paste provided the maximum percentage defects for all surface finishes. The anti-tombstoning paste gave higher defect percentage than the lead-free solder paste, when used with HASL and OSP finish. For all other lead-free finishes (Ag, ENIG, and Sn), anti-tombstoning paste resulted in the least percentages of defects. The lead-free paste gave lower percentage defects when compared to Sn/Pb paste for all surface finishes. For the case of Sn surface finish, the lead-free and Sn/Pb pastes gave similar defect percentages.



**Figure 8 Defect distributions for solder paste and PWB surface finish type**

A considerable difference is observed for the lead-free solder paste and the lead-free surface finish combinations. It can be clearly seen that the ENIG finish had a lower percentage of total defects followed by immersion Ag and Sn finishes.

## **5. Environmental Tests and Results**

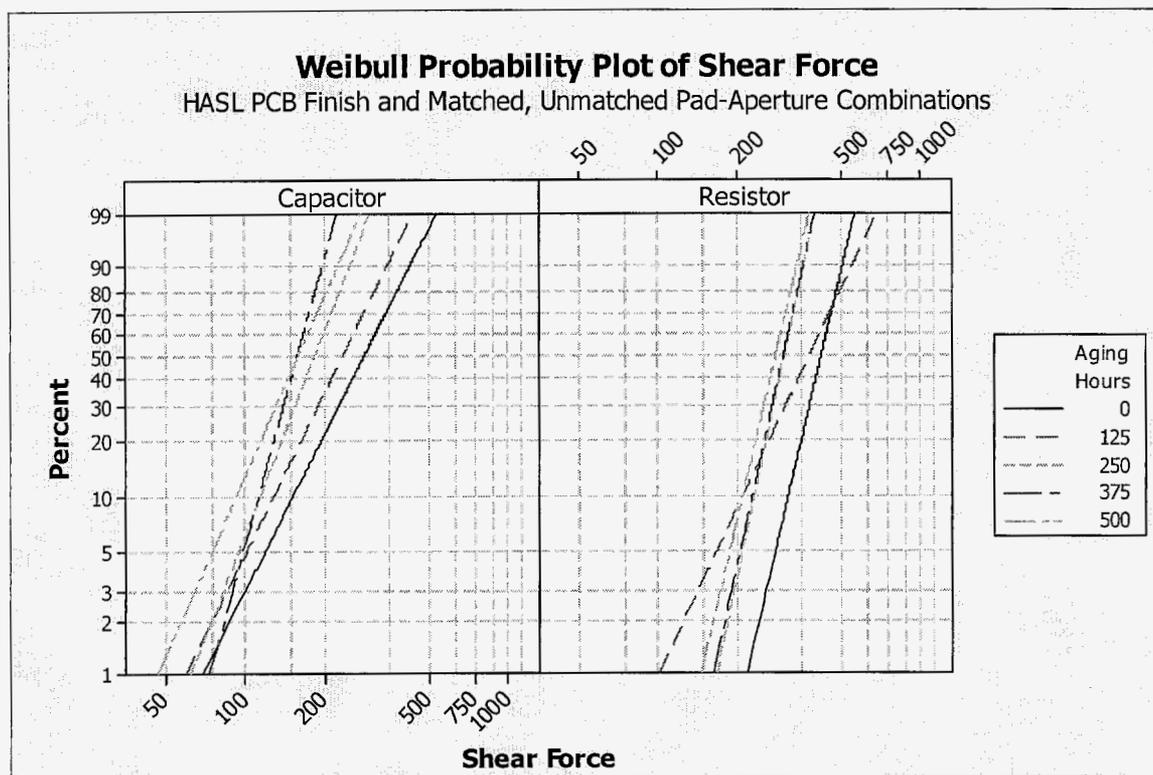
### **5.1 Assembly Isothermal Aging Test**

Some of the test vehicles were subjected to isothermal aging in order to determine their mechanical degradation and microstructural changes with exposure. Isothermal aging was carried out at 150°C for periods to 500 hours. Even though this temperature is relatively much higher than most applications, it was chosen to shorten experiment time while achieving some measurable mechanical and microstructural changes. Microstructural changes – including intermetallic growth and metallurgy – were examined by cross-sectioning exposed samples and evaluation visually or by scanning electron microscopy (SEM). The mechanical degradation was characterized by shear testing of assemblies at 125 hour intervals. The shear test was performed at a height of 6mils (150µm) from the board surface with a rate of 300µm/s. Five components were sheared for each run combination of the experimental design. These data are presented elsewhere [1].

### **5.2 Assembly Isothermal Aging Test Results**

Figures 9-11 depict the Weibull plots showing variation in solder joint shear strength for all surface finishes at various thermal aging intervals for the matched and unmated pad-aperture combinations. Resistors and capacitors with horizontal orientation printed using a 4.65 mil thick stencil, 90% aperture size, and lead-free paste. This includes all pad-aperture combinations and PWB surface finishes.

Figure 9, shows the shear force Weibull plots for the tin-lead with HASL surface finish for capacitors and resistor. Shear tests were performed at 125, 250, 375, and 500 hour intervals. It is apparent that shear force for the resistors are much higher than capacitor, ranging from 280 to 418 grams and from 158 to 284 grams, respectively. One possible reason for higher strength may be due to resistors having only 3-sided solderable whereas capacitors have 5-sided solderable surfaces. Lower solderable surfaces for the same amount of paste will have higher solder joint volume; therefore; higher shear force. It is also noticeable from this and other plots (not shown here) that the generally distributions for the 125 aging-hour interval were different form the rest. This is apparent for resistors, shear forces have much wider variations with its distribution crossing the Weibull distributions for as build and after 500 aging hours. Abnormality for shear behavior after the early stage of aging has also been shown for other packages [11]. To better define trend, data for this aging interval was intentionally removed from the other plots.



**Figure 9 Shear force Weibull plots for HASL surface finish, tin-lead paste, matched and unmatched pad aperture combination**

Figures 10 and 11 show shear force Weibull plots for lead-free PWB surface finish assembled using lead-free solder paste. A 4.65 thick stencil with a 90% aperture size and different pad-aperture combination were used in the assembly process. Passive devices with horizontal orientation were considered for shear testing.

It is evident from these figures that except for ENIG finish, shear forces for resistors on different surface finishes are better than capacitors. Generally, the 50 percentile shear forces decrease with aging time for capacitor and resistor assemblies on all surface finishes. For the lower percentile shear forces; however, the trend is not as distinguishable as those for the higher percentiles. This is clearly apparent for capacitors assembled on ENIG pad surface finish showing narrower distribution for those aged. The intermetallic growth aspect of microstructure features are discussed in another paper [3]. Purely from Weibull distribution, it can be inferred that intermetallic formed for this surface becomes more brittle and causes much narrower distribution as isothermal aging progress.

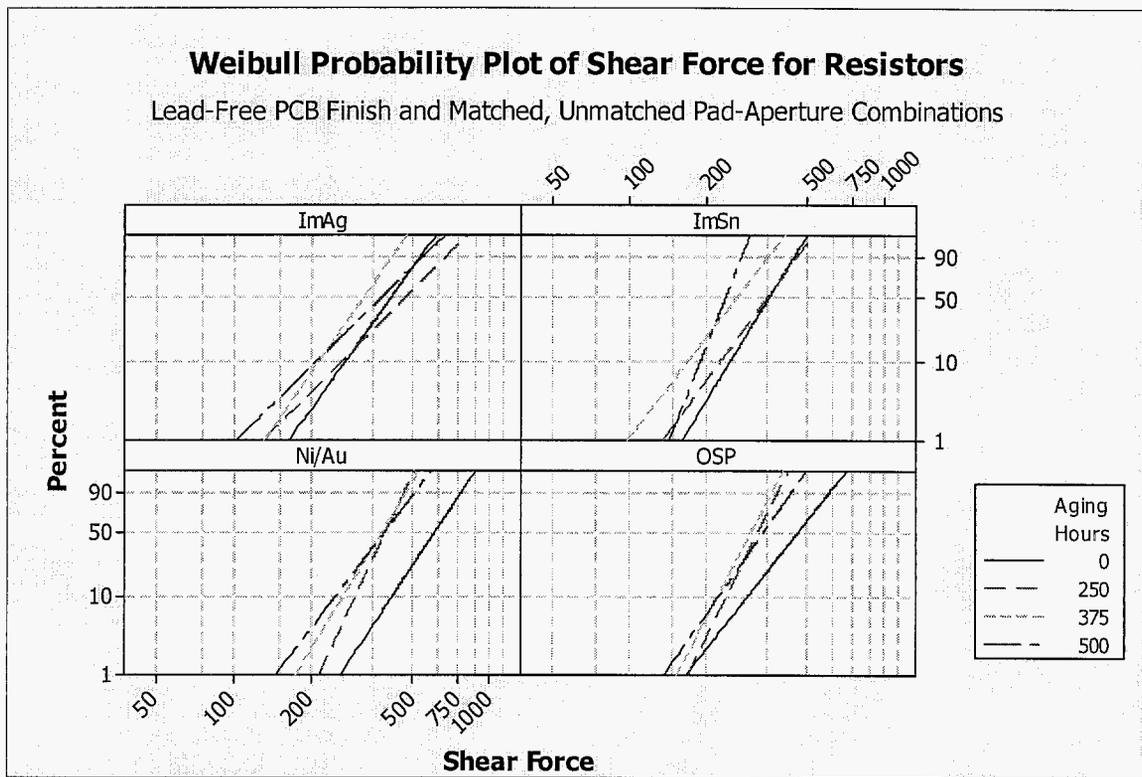


Figure 10 Shear force Weibull plots for lead-free solder resistor assembly and various surface finishes

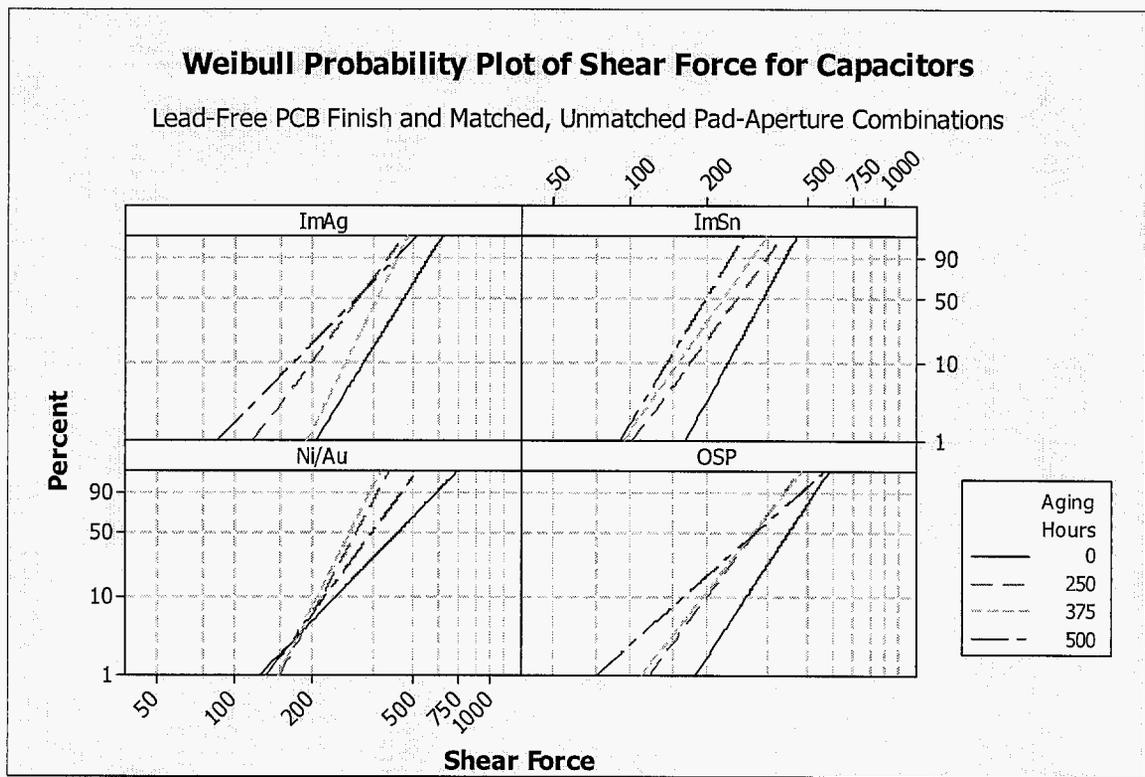
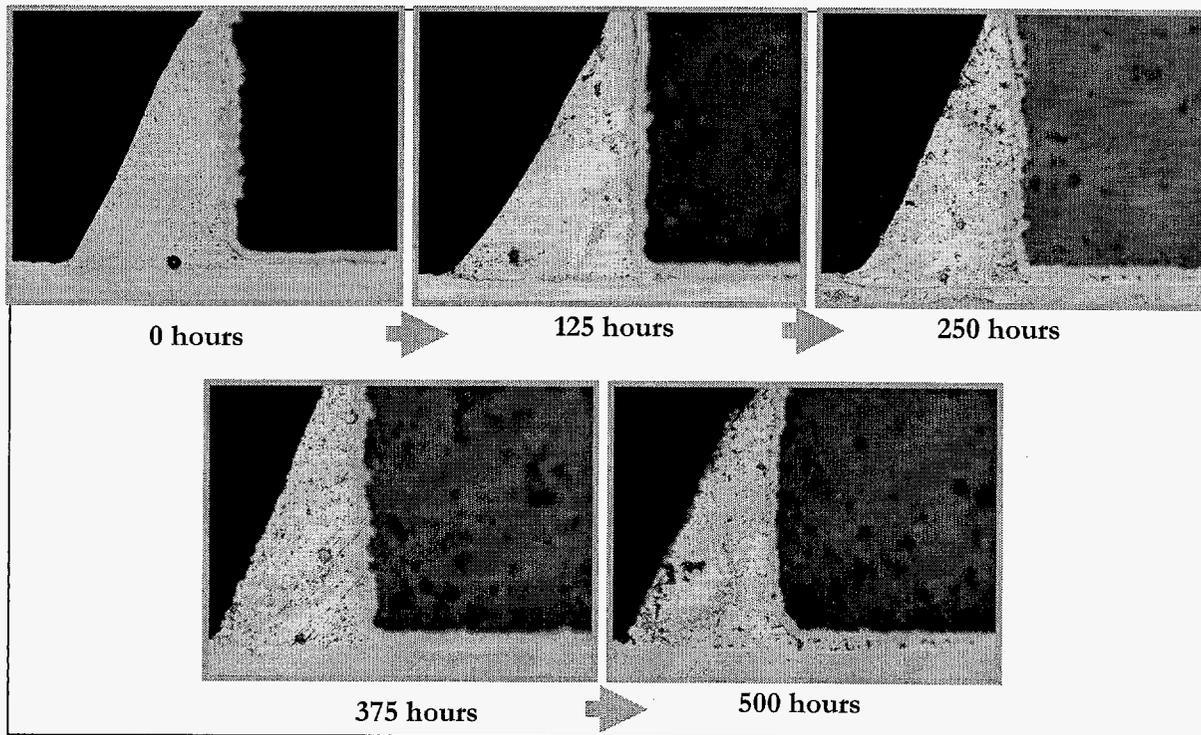
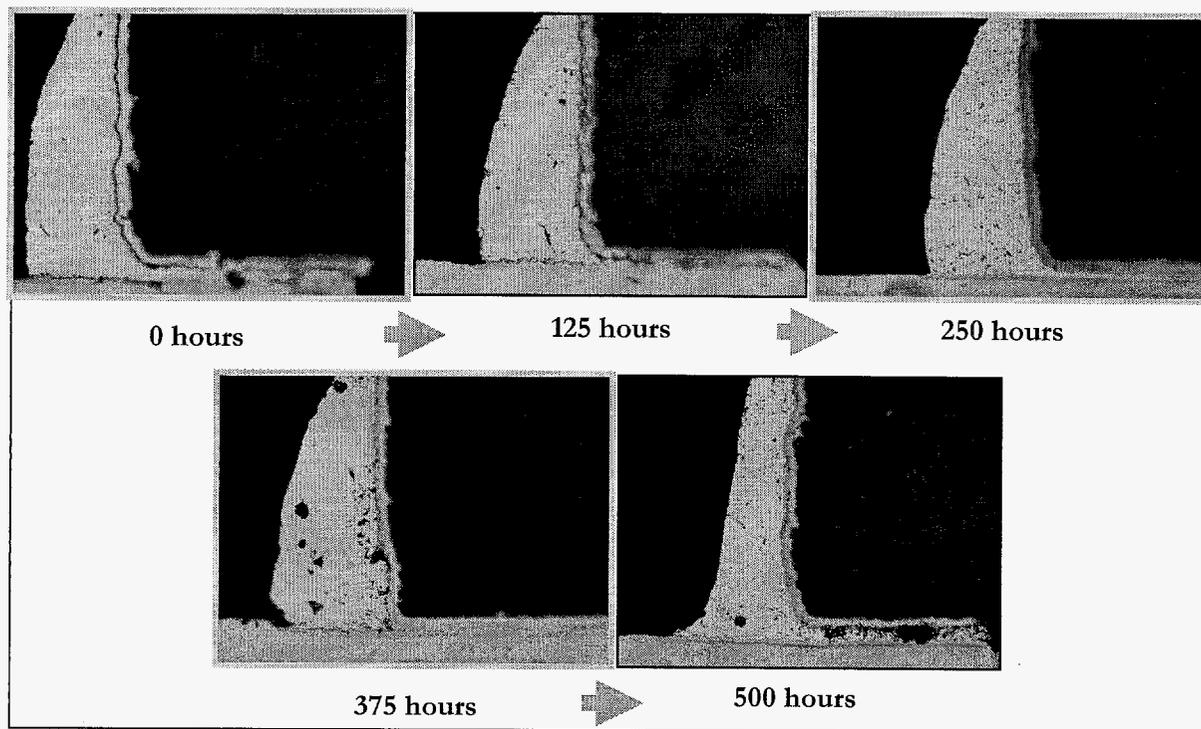


Figure 11 Shear force Weibull plots for lead-free solder resistor assembly and various surface finishes

Representative of microstructural changes with aging progress for two key surface finishes, ENIG and ImAg for resistors are shown in Figures 12 and 13. Both surface finishes show severe microstructural damage with increase in aging. More cracking with voids were observed starting under the package for the assemblies with ENIG surface finish.

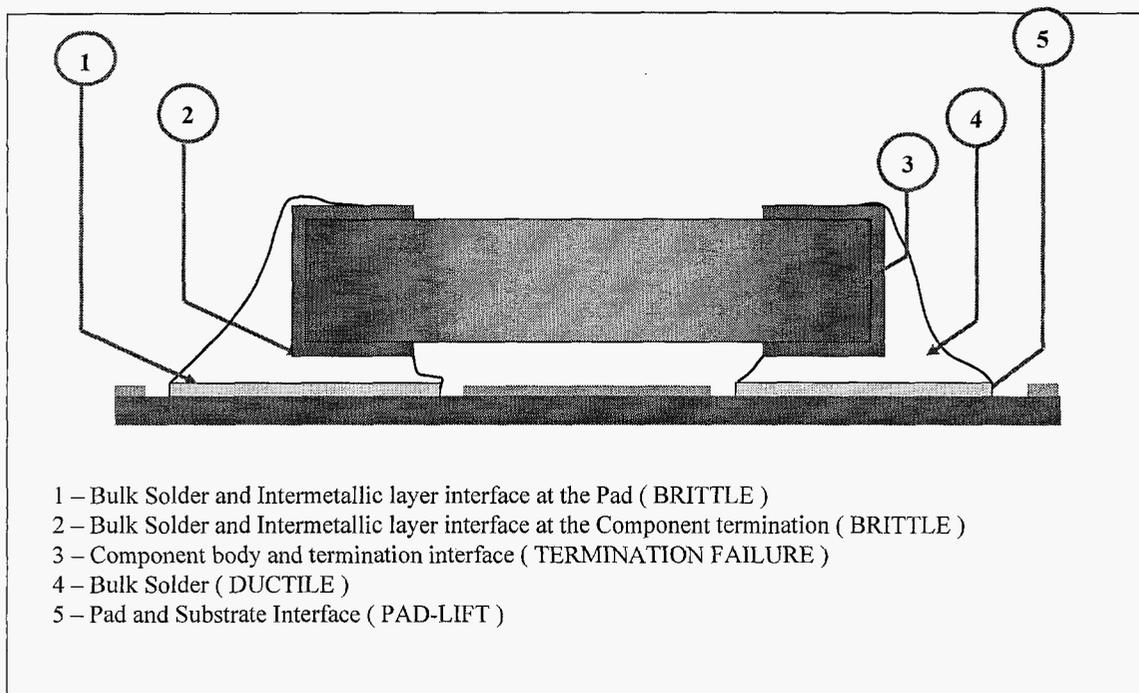


**Figure 12** Microstructural changes with aging time at 150°C for the 0201 assemblies on pads with ImAg surface finish

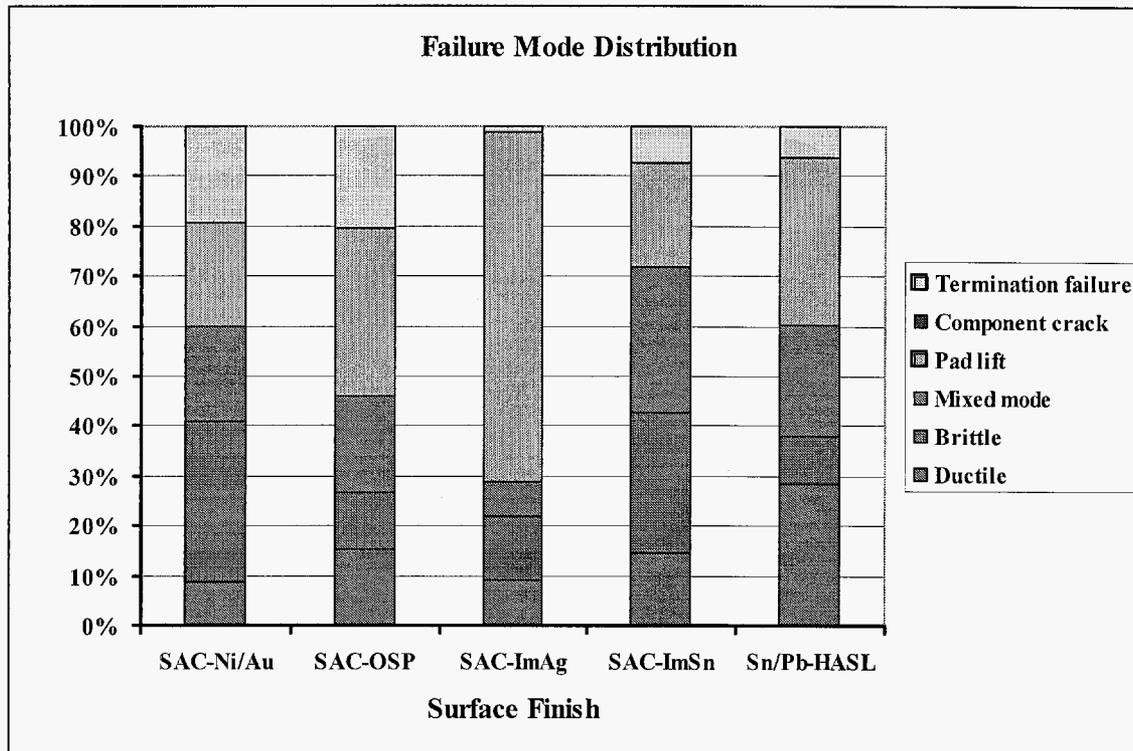


**Figure 13** Microstructural changes with aging time at 150° for the 0201 assemblies on pads with ENIG surface finish

The modes of fractures were also recorded for all assemblies after shear tests. Fractures were categorized into five modes as shown in Figure 14. Relative failure modes for all surface finishes including ENIG and ImAg for all aging intervals are shown in Figure 15. Solder joints of horizontal resistors formed using a 4.65 thick stencil with a 90% aperture size, including both matched and unmatched pad-aperture combination are considered for failure modes study. This figure clearly illustrates the different failure modes for the solder joints formed for each PWB finish. It reveals that HASL surface finish is the most ductile having higher ductile failure and lowest brittle failure whereas ENIG had the highest brittle failure modes. The ENIG brittle failure modes further confirm the narrowing Weibull distribution with aging as discussed. It is interesting to note that ImAg, had the highest pad lifting, therefore, the shear distribution may be more representative of pad adhesion behavior with aging. This failure mode can not be projected from the Weibull distributions for shear force however.



**Figure 14 Possible sites for failure during shear testing**



**Figure 15 Shear testing failure modes for assemblies with tin-lead and lead-free solder alloys and different surface finishes**

### 5.3 Thermal Cycling Approach

An industry-wide guideline document, IPC-SM785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, for accelerated reliability testing of solder attachment has been around for more than a decade. Only recently, the industry has agreed to release an industry-wide specification, IPC-9701 [9], in response to area array technology implementation and to provide a standard procedure, failure analysis, and data report for solder joint reliability testing. The newest revision, IPC-9701A, includes guidelines for lead-free solder alloys.

A few of the test vehicles from this experiment were subjected to the thermal cycle range commonly used by NASA and also specified in IPC 9701. The cycling was done at the NASA-JPL facility and the author has documented the test results under this thermal cycling condition for area array packages [10, 11]. The 0201 assembled test vehicles were those that have ImAg and ENIG surface finishes and have lead-free solder interconnects. The cycling condition ranged from -55 to 100°C with 3-10°C/min heating/cooling rate and dwell of at least 10 minutes at extreme temperatures.

Because of the lack of daisy chaining, especially for capacitors, the assemblies were not continuously monitored as specified by IPC-9701. However, they were removed at intervals and visually inspected by an optical microscope. Assemblies with 0201 resistors were selectively monitored for resistance changes. These – as well as microstructural characterization after 1500 thermal cycles – were documented. In addition, a number of assemblies were subjected to shear test both along the width and length to characterize behavior. For correlation of thermal cycle shear data to isothermal aging, it was needed to correlate the shear test results between the two facilities. The

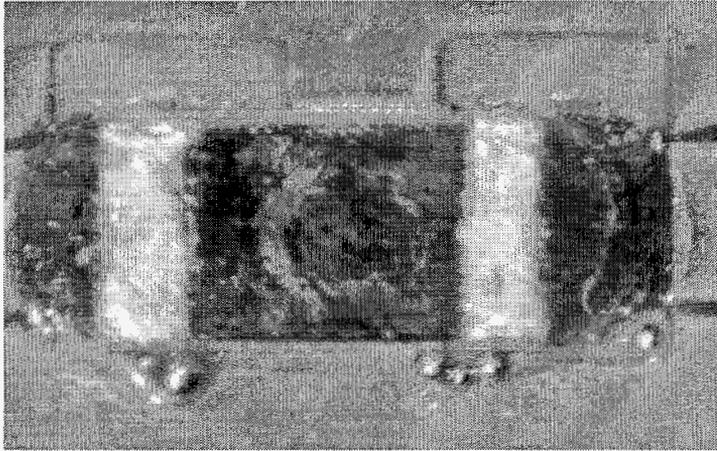
remainder of test vehicles was sent to Rochester Institute of Technology (RIT) for additional shear tests.

#### **5.4 Thermal Cycle Test Results**

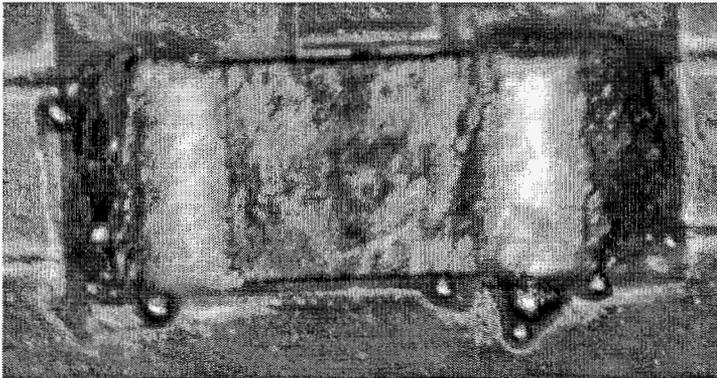
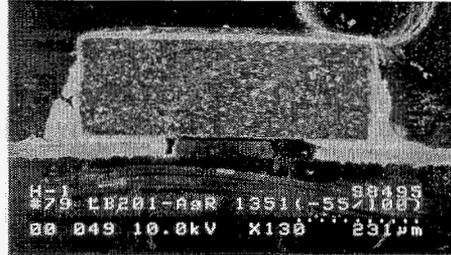
A solder joint has three primary layers of attachment, namely, (1) intermetallic layer at component metallization, (2) the solder bulk, and (3) intermetallic layer at the copper pad. The intermetallic layers are brittle and have the least chance for plastic deformation when the joint is sheared. The only layer of attachment undergoing plastic deformation is therefore the solder bulk. Plastic deformation here pertains to the thermo-mechanical fatigue experienced by solder joints subjected to thermal cycling. The growth in the intermetallic layers reduces the solder bulk component of the joint and leads to areas of stress concentration. As a result, the bulk solder standoff providing compliance to thermo mechanical fatigue is reduced, affecting the fatigue resistance of the joint.

Figures 16 and 17 show the optical microscopy photographs taken at various thermal cycling stages for a capacitor and resistor assembly, respectively. This figure also includes the SEM photomicrographs of the same assemblies prior to and after cross-section at 1500 cycles. Except for solder balls that are clearly apparent, because of small feature of 0201, it is difficult to capture the details of microstructural changes by optical microscopy. When assemblies were removed for visual inspection, a limited number of daisy-chain resistors were also manually measured for resistance changes. Out of a total of 8 daisy chains for the three test vehicles, only one failed at about 1200 thermal cycles. The failed daisy chain was for the test vehicle with modified home plate pad design, ENIG surface finish, lead-free paste, and 80% aperture. Since test vehicles were not built for thermal cycling and monitoring, there might have been other failures that were not included in the monitoring. SEM photomicrographs of the same assemblies clearly show that for the acceptable condition, minimum degradation are induced due to 1500 thermal cycles in the range of -55/100°C.

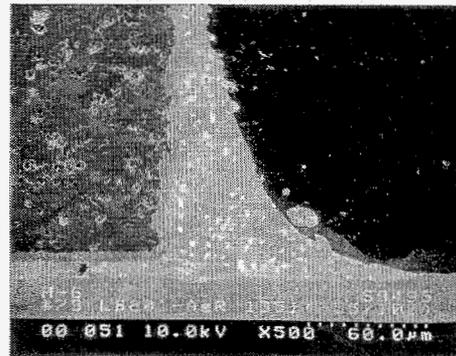
Figure 18 shows SEM photomicrograph of assemblies taken after 1500 thermal for the lead-free solder joints on ENIG or ImAg pads surface finishes. There are signs of sporadic microcracks from the outer surface and under package with no one single being significant. A portion of the assemblies that were subjected to thermal cycling were also shear tested. The results before after 1500 thermal cycles for ENIG and ImAg surface finishes are shown in Figure 19. Significant drops in shear force shown in this figure can not be verified by microstructural changes shown in previous figures. The shear force trend before and after 1500 thermal cycle; however, remain unchanged with ENIG surface finish show higher force than ImAg.



a) Resistor with tin-lead solder joint As fabricated (ID 79)

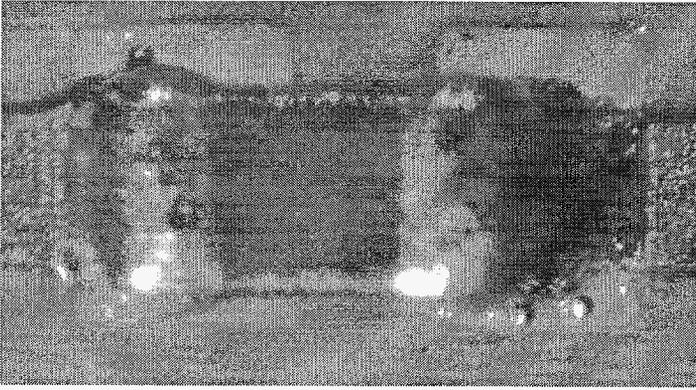


b) 400 thermal Cycles (-55/100°C)

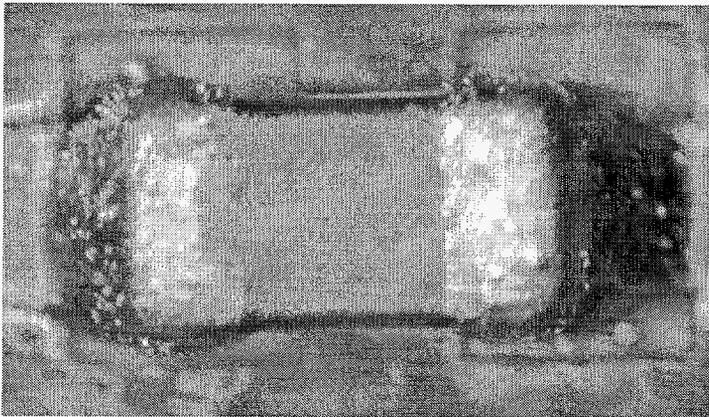
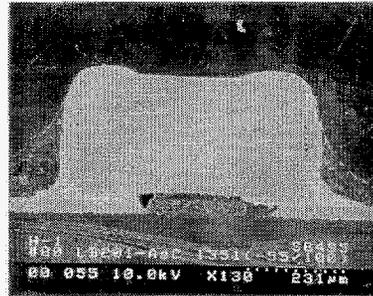


c) 1500 Thermal Cycles

**Figure 16 Optical and SEM photomicrographs of a resistors assemblies taken at various thermal cycle intervals (-55/100°C)**



a) Capacitor with tin-lead solder joint  
As fabricated (ID 80)

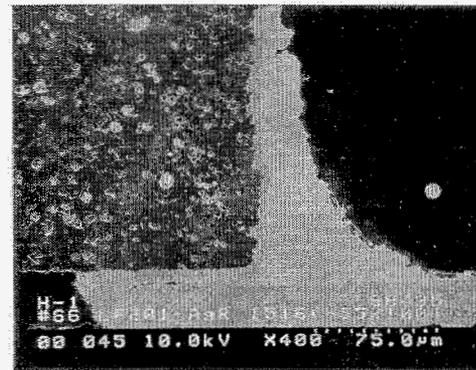
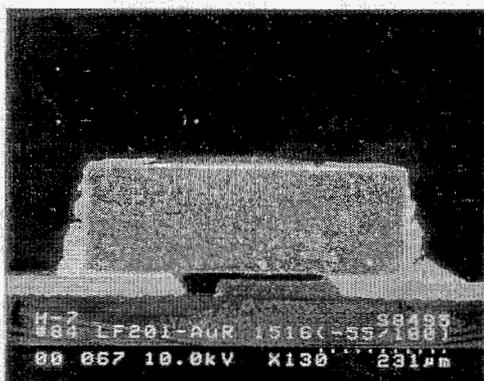
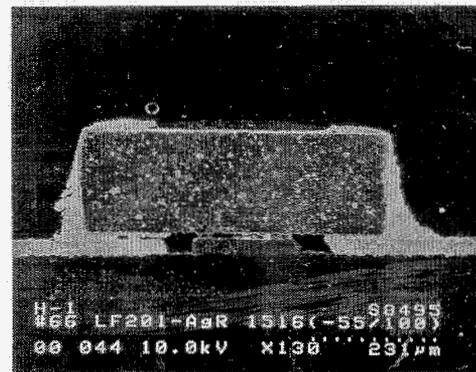
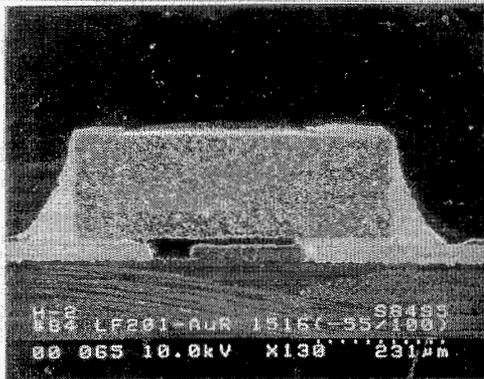


b) 400 thermal Cycles (-55/100°C)



c) 1500 Thermal Cycles

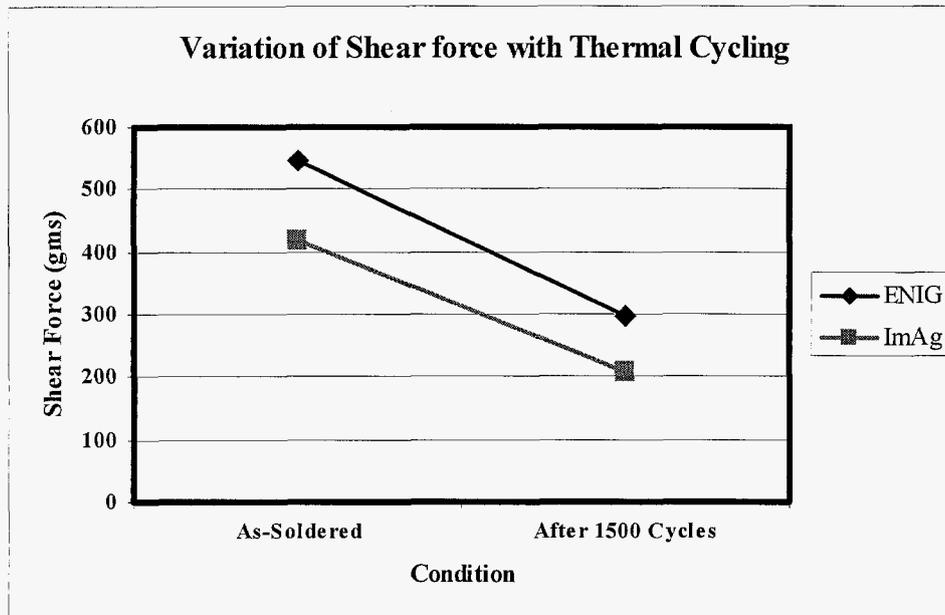
**Figure 17 Optical and SEM photomicrographs of a capacitor assemblies with ImAg surface finish taken at various thermal cycle intervals (-55/100°C)**



a) LF ENIG (ID 84)

b) LF ImAg (ID 66)

Figure 18 SEM photomicrographs of resistors assembled with ENIG and ImAg surface finishes at 15000 cycles (-55/100°C)



**Figure 19 Shear force variation for thermally cycled assemblies on pads with ENIG and ImAg finishes**

## 6. Conclusions

This investigation identified a number of key factors pertaining to manufacturing parameters and behavior under isothermal and thermal cycling for environmental tests. Only a few key findings are given below.

- Solder beading is the most prominent defect. The 80% aperture size provides a low percentage of the solder beading defect, whereas 100% aperture size provides a low percentage of the skewing defect.
- Shear testing of thermally-aged assemblies reveals that SAC paste with ENIG finish requires the highest shear force, followed by ImAg and OSP. ImSn finish required the least shear force. For ENIG surface finish, Weibull distribution trends with aging somewhat different from the other assemblies.
- Shear testing of thermally-cycled assemblies reveals that SAC with ENIG finish outperforms SAC with ImAg finish.
- For an acceptable assembly condition, minimum damage occurs due to thermal cycling in the range of -55 to 100°C based on microstructural change somewhat in contrast with shear force reduction trend.

## 7. Acknowledgement

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## Lead Free 0201 Assembly and Thermal Cycle/Aging Reliability

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### 1. Abstract

The many challenges with 0201 assembly can be attributed to the solder paste volume, pad design, aperture design, board finish, type of solder paste, pick-and-place, and reflow profile. A Design-of-Experiment (DOE) study was carried out to investigate the effects of these parameters on assembly defects and reliability.

The test vehicles for the investigation consists of pad layouts for 2000-0201 components. Five different test vehicles were used, with the same pad layout and non-solder mask defined pads, with HASL, ENIG, Pure Tin, Immersion Silver and OSP finish. Four different pad shapes are designed on each of the test vehicles (rectangular, oval, modified home plate and double trapezoid). The pad areas for all four shapes are maintained the same. Pads were oriented both in the horizontal and vertical directions. Electroformed 3-mil and 4.65 mil thick stencils were used for printing the solder paste. The stencil was designed to obtain two distinct aperture-pad combinations (matched and unmatched). Three solder paste types (tin-lead and anti-tombstoning and lead free) were used in this investigation.

Two test vehicles assembled for each experimental run, one with resistors and the other with capacitors, provided an understanding of the difference in the process for these two common passive devices. This paper discusses in detail the influence of a few key parameters and defects associated with the 0201 component using both leaded and lead-free solder alloys. A large number of these assemblies were subjected to isothermal aging at 150°C and thermal cycling in the range of -55 to 100°C to establish their reliability. Shear tests were carried out at various aging intervals up to 500 hours to determine the effects of aging damage on strength were compared to virgin assemblies. Similarly, shear test data generated before after 1500 cycles and data for ENIG and ImAg are compared. Weibull plots will be given for reliability to establish solder joint fatigue behavior for the lead free assemblies compared to lead based solder as well as data correlation for various sets of data. In addition, photomicrographs taken by optical microscope at intervals during thermal cycling to establish damage progress are given. Scanning electron microscopy (SEM) analysis before and after cross-sectioning are also performed to reveal microstructural changes and intermetallic formation at 1,500 thermal cycles are also included.

Key words: 0201 assembly, lead-free process, lead-free surface finish, modified apertures, thermal aging, thermal cycle, isothermal aging, shear load

## **2. Background**

### **2.1 Discrete Passive Shrink Trends**

Passives are used throughout electronic systems to provide the functions of resistance, capacitance and inductance. There are more than 10 discrete passives used for every active component in a typical system. Passives account for 90 percent of components, 40 percent of board area and 30 percent of solder joints in typical systems. The majority of passives is still discrete ceramic based and of standard outline. The subject of manufacturing issue and reliability of recently introduced tiny 0201s passive components have been the subject of many papers including a comprehensive paper by these authors and to be published in *Microelectronic Reliability Journal*[1-4]. Figure 1 compares sizes of previous types of passive relative to each other and also include a comparison of the 0201 component to a ball point pen. Figure 2 shows the market project for use of this and its previous generation indication that the market share for this component size is rapidly increasing.

In 1977, a typical passive component measured 3.2 mm x 1.6 mm (1206) in size. Ten years later in 1987, 0805 passives had become the most common with a size of 2.0 mm x 1.25 mm. The end of the millennium saw the 0603 passive measuring 1.6 mm x 0.80 mm claiming the largest usage; and 0402 passives, at 1.0 mm x 0.50 mm, were becoming the most popular size until recently. The 0201 passives, which until recently were the smallest passives in production, have dimensions of only 0.60 mm x 0.30 mm. Compared to 0402s, 0201s are about four times smaller in area and nearly five times lighter, which makes them attractive particularly for small portable systems. The newly introduced 01005 passives [5] are even smaller than 0201 and have of 0.4mm x 0.2mm respectively.

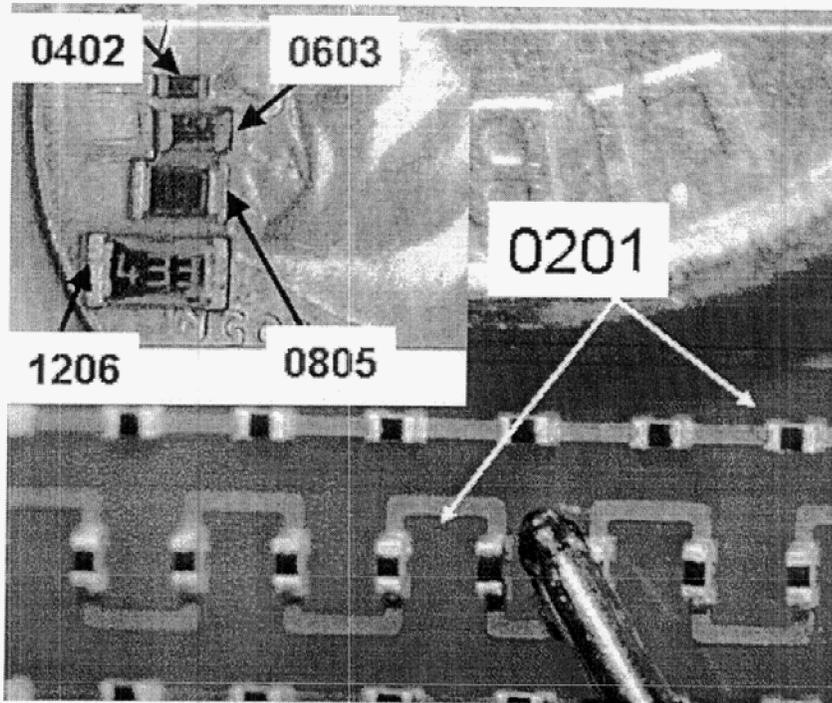


Figure 1 Size comparison of tiny 0201 discrete passive with a dime and pen tip

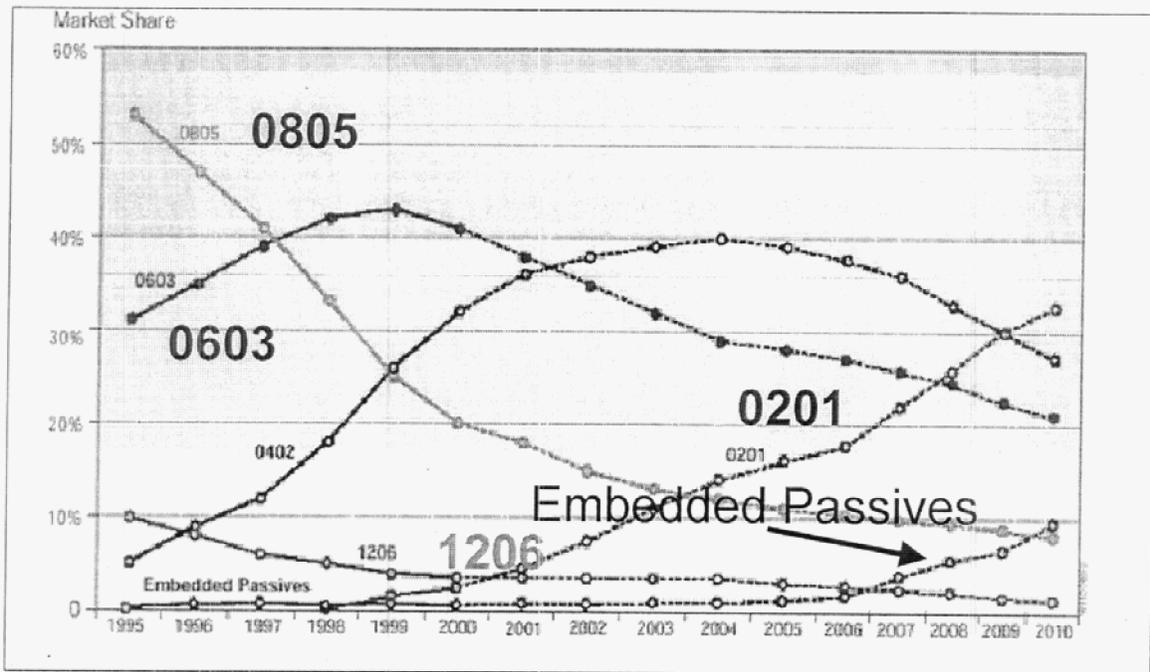


Figure 2 Market share of passives, growth of 0201 and embedded passives (Source: Prismark)

All electronic systems continue to be subjected to the trend of added functionality in a shrinking package technology. This trend is enabled for the most part by the shrinking evolution in feature size of silicon integrated circuits (ICs). Unfortunately, passive components have not kept up with ICs in this regard. Peripheral passive components are not as functionally space efficient as ICs and are seen as one of the major roadblocks in increasing the functional density of electronic systems. Clearly, the need for functional density will force designers to look at creative packaging alternatives. If the historical rate of passive component density continues, by 2010 it is reasonable to expect passive component densities of 20 to 30 passives/cm<sup>2</sup>.

## 2.2 Passive Embedded into Package

Integrated passive devices, where arrays of resistors or capacitors are swept into a component (or a board), have also gained in popularity. Figure 3 shows schematically discrete passives on the surface and between the build up layers [6]. These devices have been used by the computer industry for some time as an effective way to implement resistors at a high I/O port interface. However, these devices are only available for arrays of standard values or commonly used functional blocks. Customized designs are expensive and offer a limited supply base. Still, the resistor, capacitor or inductor value of a discrete is very much a function of physical size. The inability to create high value embedded devices in a space efficient manner puts limitations on the amount of integration possible. Also, most embedded advances will continue to suffer, primarily due to component density and tolerance limitations when compared to discrete passives. The tolerance of most discrete chip resistors is in the range of 1%, so designing to a possible 15% or more variation is not an attractive proposition.

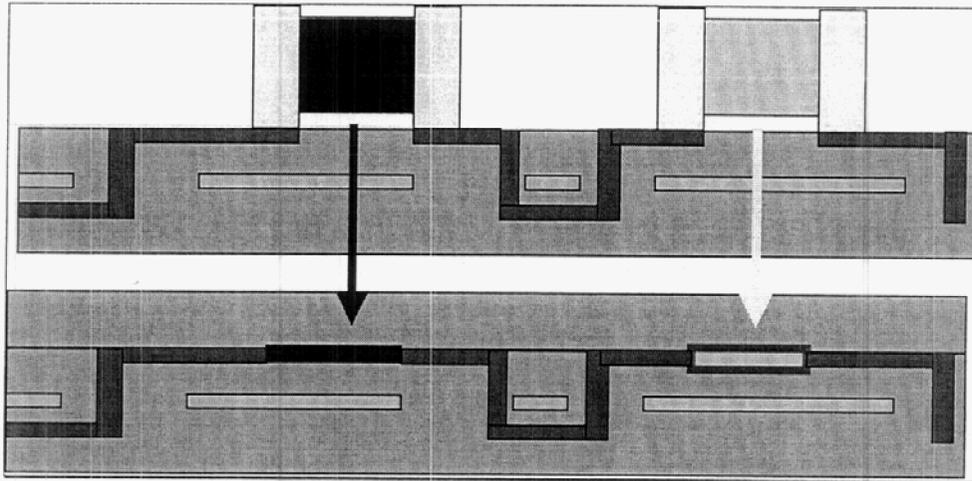


Figure 3 Schematic demonstration of discrete and embedded passives

### **2.3 Embedded Passive into Printed Wiring Board (PWB)**

Embedded passive (EP) technologies introduce new materials and processes into PWB fabrication with the goal of reducing component part count through the removal of surface mount components. This is accomplished by embedding equivalently functional resistors, capacitors and inductors within the inner-layers of the PWB in place of traditionally surface-mounted passive components. Since the internalized, embedded devices require no solder joints, the principal failure mode of assemblies, solder joint failure, is reduced. Other advantages include:

- Improved electrical properties through additional termination and filtering opportunities and reduced length of electrical connections
- Reduced cost through decrease in board assembly operations
- Increased product quality through the elimination of incorrectly attached devices
- Decreased board area due to reduction in the number of discrete passives
- Decreased wiring requirements due to the integration of resistors and bypass capacitors into the board
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size

However, there are also disadvantages such as:

- Decrease in reliability because of emerging technology and difficulties with inspection
- Decrease in assembly level rework
- Decrease in overall assembly yield and increase in board cost per unit area

### **3. Literature Survey on Key 0201 Assembly/Reliability**

For implementation of 0201, assembly processes must be evaluated and optimized for several key parameters including the following:

- Pad design and surface finish for PWB
- Solder paste selection
- Stencil design and solder paste print parameters
- 0201 placement
- Reflow profile for selected solder
- Defect characterization
- Inspection
- Rework
- Reliability evaluation

A number of investigators [2-4, 7] have studied one or more of these parameters and recommend methods for SMT assembly process improvement, but none have a comprehensive investigation that also cover extensive reliability data comparison. In what follows, a brief literature review is given both for manufacturing and their associated defects as well as environment test results.

### **3.1 Pad Design**

At this time, there is no universally accepted PWB pad design for 0201 discrete components. Pad distance is another parameter that is critical and needs to be considered. The commonly used pad designs are: square, rectangle, extended half circle, oval, and trapezoid. A few of these pad designs were considered in an experimental evaluation in order to determine the pad design that induces minimum manufacturing defects. The PWB surface finish is another factor that needs to be considered during manufacturing process optimization.

### **3.2 Solder Paste Type and Stencil Design**

Solder paste type and stencil design are two other key printed factors in creating a robust 0201 assembly process. The correct amount of solder and its consistency can help significantly to minimize the production of the most common defects such as “tombstoning”. Consistency in the amount of paste is critical since tombstoning occurs due to the introduction of an imbalance in surface tension forces during the reflow process. If the solder paste volumes deposited on two pads differ, then the solder paste will reflow at different rates inducing two different surface tensions at the time of reflow when the part is floating on molten solder. This imbalance in forces causes the 0201 component to stand up or tombstone. Because the 0201 component has extremely small mass, even a small amount of variation in solder paste volume can bring about enough surface tension force to pull the part upward. The other major cause of tombstoning is a component that is placed off center so that more of the component is on one pad than the other.

Stencil design, and its corresponding solder paste transfer efficiency, is the next critical parameter on printing the correct amount of paste onto a PWB through a small stencil aperture (orifice). Transfer efficiency is a measure of the amount of paste in the aperture that transfers onto the PWB pads. Stencil design and type are important factors in determining the transfer efficiency of a particular solder paste. Smaller stencil apertures require the highest possible solder paste transfer efficiency. The stencil area ratio is shown to be an even more critical parameter for paste efficiency because of the small opening. Area ratio is the ratio between the areas of the stencil opening to the area of the wall of the stencil aperture (aperture area/wall area). Figure 4 shows [7] that the number of total defects remains relatively constant for an area ratio of 0.65 and greater. There is a sharp increase in the number of defects for the ratios of 0.5 and 0.45.

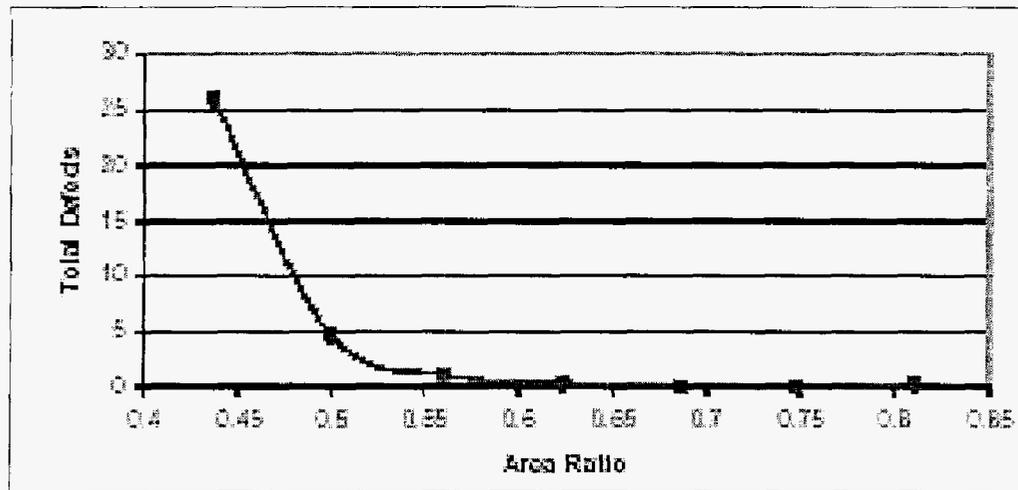


Figure 4 Total defects as a function of area ratio [7]

### 3.3 Common Defects

The most common defects for the 0201 assembly process in addition to missing components are:

- Tombstones
- Solder Bridges
- Solder Beads

As noted in the previous section, tombstoning defects become prevalent with inconsistent solder paste volume on each of the 0201 pads. Stencil design and solder paste selection are critical as well as the component placement.

Solder bridging is a common defect in fine pitch assembly process including 0201. The 0201 is a small component and it is generally a requirement to assemble them in a densely packed area on a PWB in order to take advantage of less board real state.

Several of the same factors that influence tombstoning and solder bridging also influence the creation of solder beads. Key factors in reducing solder beadig are to print the solder paste accurately, evenly, and consistently and to place the component squarely and evenly onto the printed paste. This can also be reduced by minimizing the amount of solder under the device.

### 3.4 Reliability

Most literature data concerns reducing manufacturing defects in order to increase yield rather than providing data on reliability. Reliability data represented by cycles-to-failures of assembled 0201 parts fabricated under several design and process conditions were presented by Baldwin, et al [7]. Failure plots from these authors are shown in Figure 5. In this Figure, the x-axis is the number of cycles while the y-axis is the percent of the 0201 devices that have failed. The thermal cycle was over the range of  $-40$  to  $125^{\circ}\text{C}$  with a 20 minute cycle. The first failure was found to occur between 1500 and 2000 cycles.

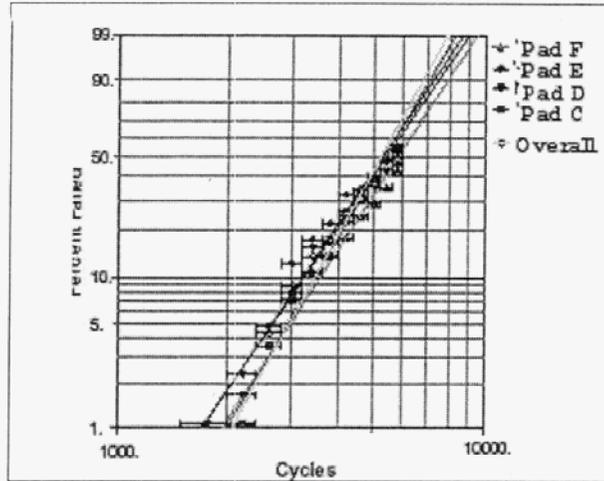


Figure 5 Cycles-to-failure for passives with different pad configurations [7]

#### 4. 0201 Process and Defects

This section discusses a summary of the effect of the type of solder paste, board finish and pad-aperture shape on 0201 assembly process defects, including both tin-lead and lead-free solder pastes and lead-free surface finishes. A design of experiment (DOE) test matrix was used to investigate the effects of various parameters on defect formation and reliability. Emphasis, however, is placed on environmental test results including thermal aging and thermal cycling represented by microstructural changes as well as shear testing.

##### 4.1 DOE Manufacturing Parameters

Based on the literature survey, the parameters considered for this experimental study were:

- Five surface finishes, hot air solder leveling (HASL), organic solder preservative (OSP), ENIG, immersion Ag, and Sn
- Tin-lead, lead-free and anti-tombstoning solder pastes
- Stencil thickness of 3 and 4.65 mils and three modified aperture shapes

Table 1 summarizes the DOE with variables considered in this investigation. The process parameters were kept constant for all the experimental runs. The experimental runs were executed in three groups, based on the solder paste type, in order to minimize the changeover time for the experiment. For each experiment run, a total of 30 test vehicles (TVs) were fabricated. Ten TVs were solder paste print only for paste quality and inspection, 10 were assembled with the 0201 resistors and another 10 with capacitors.

Table 1. Phase 1 DOE Parameters

Factors	Levels				
	HASL	ENIG	ImSn	ImAg	OSP
Surface Finish	HASL	ENIG	ImSn	ImAg	OSP
Pad shape	MHP	DT	Oval	Rectangular	

<b>Aperture Shape</b>	MHP	DT	Oval	Rectangular
<b>Aperture size</b>	80%		90%	100%
<b>Stencil Thickness</b>	3mils (75 $\mu$ m)		4.65mils (116.25 $\mu$ m)	
<b>Solder Paste</b>	Anti-tombstone	Lead-free		Tin-Lead (Sn/Pb)
<b>Orientation</b>	Vertical		Horizontal	
<b>Component</b>	Resistor		Capacitor	
MHP- Modified Home Plate Design DT- Double Trapezoid Design				

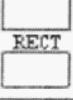
Each TV had 240 non-solder mask defined (NSMD) rectangular pads with dimensions and spacing as shown in Table 2. The pads were equally distributed in the horizontal and vertical orientations. Five different types of test vehicles, with the same pad layout, with varying pad finishes (HASL, ENIG, pure Sn, immersion Ag and OSP) were used to investigate the effect of varying surface finishes. Two test vehicles were assembled for each experimental run, one with zero-ohm lead-free resistors and the other with lead-free capacitors. The components had tin surface finish.

#### 4.2 Stencil Design, Printing, and Placement

Electroformed 3 mil and 4.65 mil thick stencils were used in this experiment. The stencil design had four different aperture shapes, with constant print area, irrespective of the stencil thickness (see Table 2). This means that for a given stencil thickness, the ideal theoretical volume was designed to be constant for the four aperture shapes. Three different no-clean solder pastes were used in this experiment. These included the anti-tombstoning (62.6Sn37Pb0.4Ag), tin-lead (63Sn37Pb) and lead-free (95.5Sn3.8Ag0.7Cu) solder pastes with Type 4 solder particles (20-38 $\mu$ m). The percent metal content in the pastes ranged from 89-90.

Optimum print process parameters were obtained after carrying out trial runs for each paste. Visual inspection was performed to determine signs of film formation on the stencil and how solder paste was deposited on the center of pads. Then, these two parameters were considered as indicators for process optimization.

**Table 2. Pad/Aperture Shape and Dimension**

Shape	Pad Dimensions			Aperture Characteristics											
				100%				90%				80%			
	L	W	S	L	W	S	AAR for 3mils 4.65mils	L	W	S	AAR for 3mils 4.65mils	L	W	S	AAR for 3mils 4.65mils
 MHP	13	9	11	12	8	12	0.76 0.49	10.8	7.2	12.8	0.68 0.44	9.6	6.4	13.6	0.6 0.39
 DT	13	10.5	11	12.5	8	13.5	0.64 0.41	11.3	7.2	14.3	0.57 0.37	10	6.4	15.1	0.51 0.33
 OVAL	13.4	9	10.4	12.8	8	12	0.8 0.52	11.6	7.2	12.8	0.72 0.46	10.2	6.4	13.6	0.64 0.41
 RECT	12.5	8	11	11.4	7	11	0.72 0.47	10.3	6.3	12.7	0.65 0.42	9.1	5.6	13.4	0.58 0.37
L-Length, W-Width, S-Spacing			(All units are in mils (0.001") unless otherwise mentioned.)												

### 4.3 Solder Reflow Process

As per the recommendations of the solder paste manufacturer, ramp-to-spike profiles were used for all three pastes. A seven-zone forced convection oven under atmospheric air condition was used. Table 3 provides details of the reflow profile stages temperature and time for the tin-lead and lead free solder pastes.

Table 3 Reflow process parameters

Reflow Process Parameters	Anti-Tombstoning & Lead Based Paste	Lead Free Paste (SAC alloy)
Peak Temperature	219°C	244.7°C
Time above Liquidus	59.16 sec	56.87 sec
Ramp Rate	1.97°C/sec	1.88°C/sec

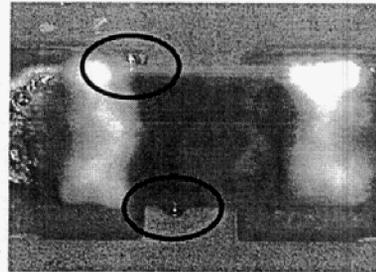
### 4.4 Manufacturing Defect Types

The assembled boards were inspected for workmanship defects using a manual vision inspection system. The various defects that were expected to occur include tombstoning, draw bridging, solder beading, component skewing, and insufficient solder (missing components). The number of defects and types was recorded for each experimental run (one test vehicle for resistors and one for capacitors), each having various pad-aperture combinations, pad surface finish, stencil thickness, and paste type. The number of defects

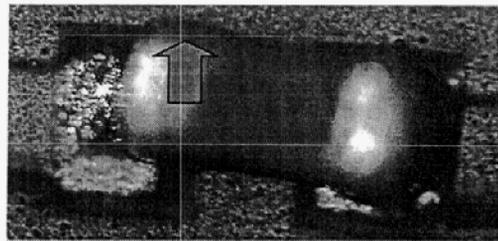
was converted into percent defects based on the total number of component occurrences on each test vehicle. This percent defect data was used to analyze the test results. Figure 6 shows typical optical photomicrographs of defects observed after assembly.



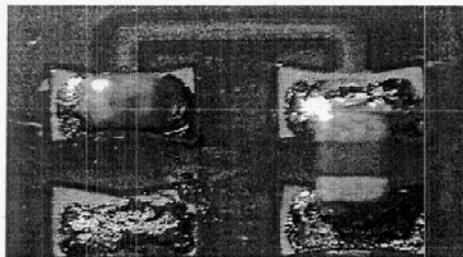
**Insufficient solder joint**



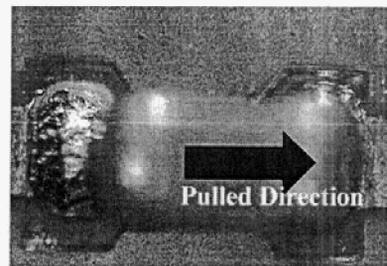
**Solder Beading  
(solder ball)**



**Component Skewing**



**Tombstoning**



**Draw Bridging**

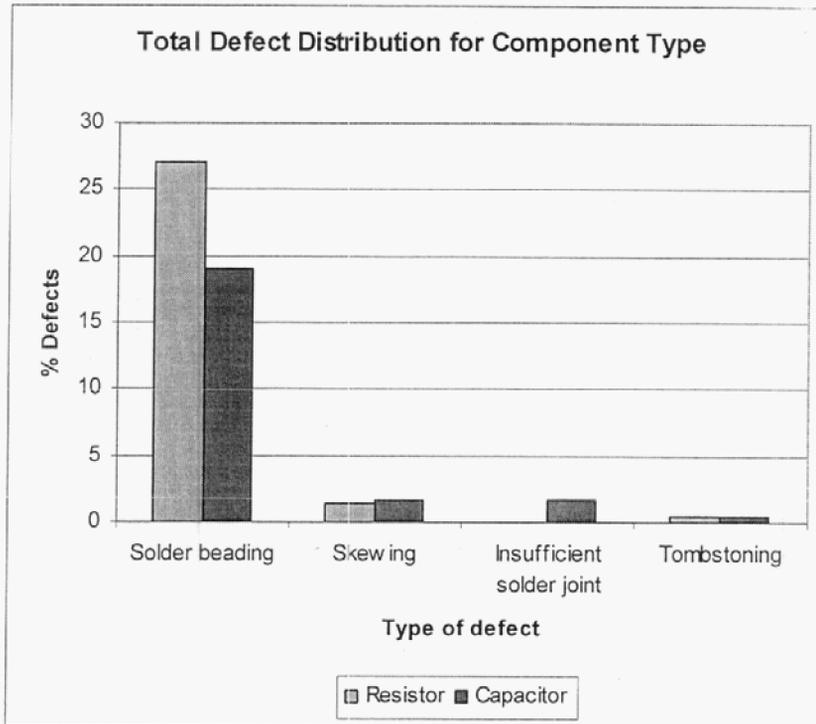
**Figure 6 Optical photomicrographs of typical defects after assembly**

#### **4.5 Defects and distribution**

The total percentage of defects and their types for the entire DOE study are shown in Figure 7. It is evident that solder beading dominates the percentage of defects by an order of magnitude compared to the other defects. Insufficient solder joint (missing components) for capacitors was due to an error in one of the experimental runs which was immediately corrected to avoid further recurrence. Since this was a mishap in process, this defect was not considered in the analyses.

One significant outcome of the experiment was the considerable reduction in the occurrence of tombstoning. Lack of significant tombstoning clearly indicates that most of the solder paste and surface finish combinations considered in the study were in relatively optimized

conditions, especially selection of stencil thickness, which plays a critical role. Data reveal that the few occurrences of tombstone defects were for PWBs with immersion silver finish when using anti-tombstoning or tin-lead solder paste. No occurrence was detected with the lead-free paste.



**Figure 7 Total defect distribution for component type**

Figure 8 shows the total defect distributions based on the combination of solder paste and surface finishes. The chart clearly reveals that the Sn/Pb paste provided the maximum percentage defects for all surface finishes. The anti-tombstoning paste gave higher defect percentage than the lead-free solder paste, when used with HASL and OSP finish. For all other lead-free finishes (Ag, ENIG, and Sn), anti-tombstoning paste resulted in the least percentages of defects. The lead-free paste gave lower percentage defects when compared to Sn/Pb paste for all surface finishes. For the case of Sn surface finish, the lead-free and Sn/Pb pastes gave similar defect percentages.

A considerable difference is observed for the lead-free solder paste and the lead-free surface finish combinations. It can be clearly seen that the ENIG finish had a lower percentage of total defects followed by immersion Ag and Sn finishes.

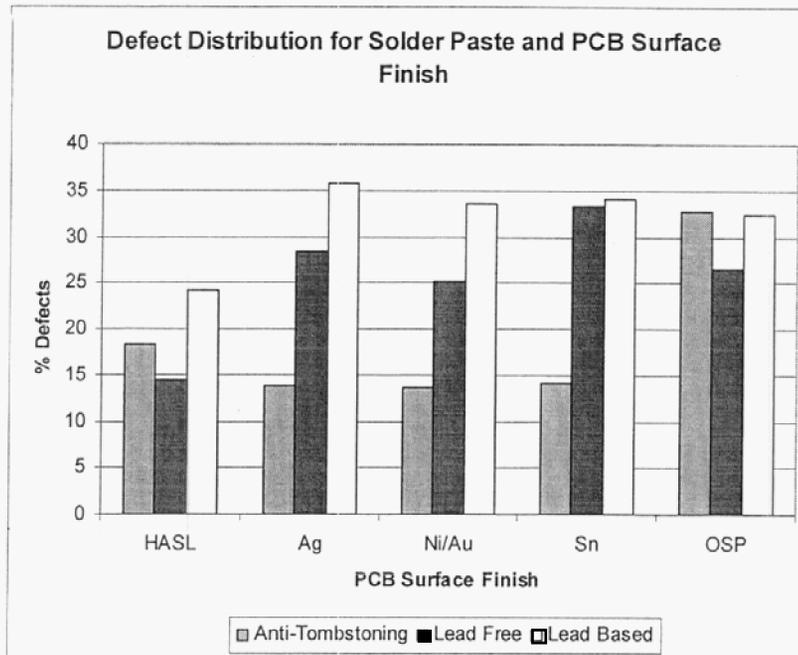


Figure 8 Defect distributions for solder paste and PWB surface finish type

## 5. Environmental Tests and Results

### 5.1 Assembly Isothermal aging Test

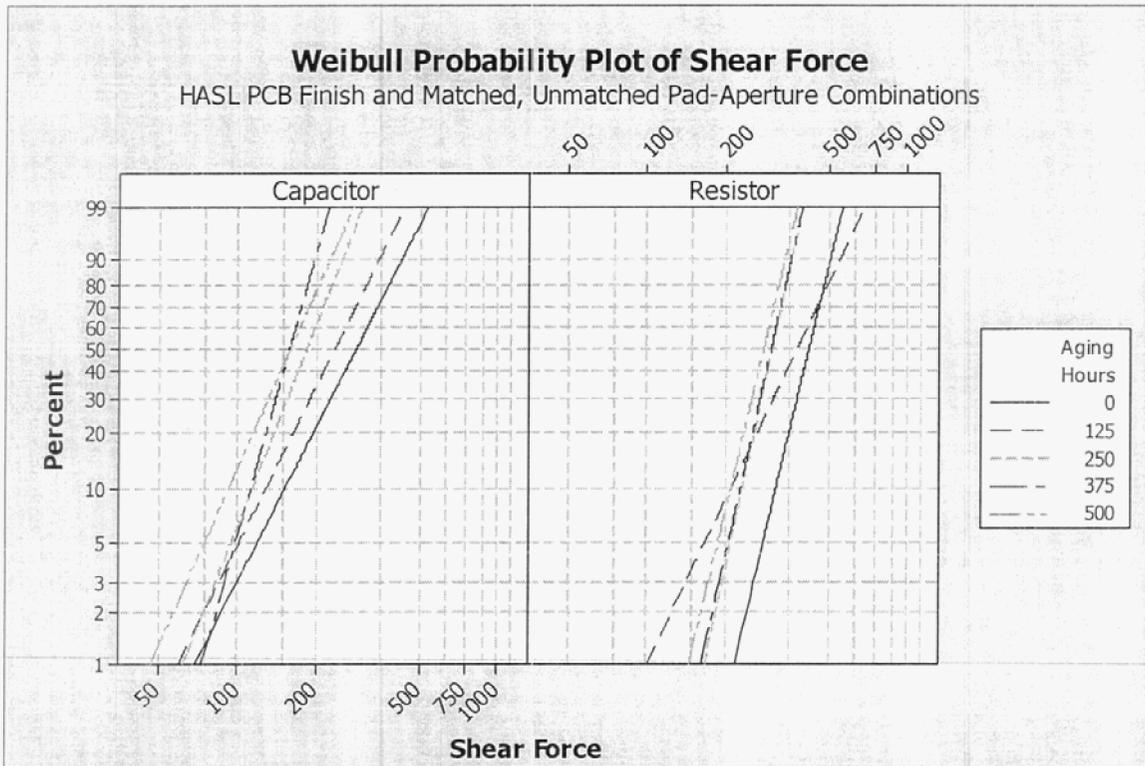
Some of the test vehicles were subjected to isothermal aging in order to determine their mechanical degradation and microstructural changes with exposure. Isothermal aging was carried out at 150°C for periods to 500 hours. Even though this temperature is relatively much higher than most applications, it was chosen to shorten experiment time while achieving some measurable mechanical and microstructural changes. Microstructural changes – including intermetallic growth and metallurgy – were examined by cross-sectioning exposed samples and evaluation visually or by scanning electron microscopy (SEM). The mechanical degradation was characterized by shear testing of assemblies at 125 hour intervals. The shear test was performed at a height of 6mils (150 $\mu$ m) from the board surface with a rate of 300 $\mu$ m/s. Five components were sheared for each run combination of the experimental design. These data are presented elsewhere [1].

### 5.2 Assembly Isothermal aging Test Results

Figures 9-11 depict the Weibull plots showing variation in solder joint shear strength for all surface finishes at various thermal aging intervals for the matched and unmatched pad-aperture combinations. Resistors and capacitors with horizontal orientation printed using a 4.65 mil thick stencil, 90% aperture size, and lead-free paste. This includes all pad-aperture combinations and PWB surface finishes.

Figure 9, shows the shear force Weibull plots for the tin-lead with HASL surface finish for capacitors and resistor. Shear tests were performed at 125, 250, 375, and 500 hour intervals. It is apparent that shear force for the resistors are much higher than capacitor,

ranging from 280 to 418 grams and from 158 to 284 grams, respectively. One possible reason for higher strength may be due to resistors having only 3-sided solderable whereas capacitors have 5-sided solderable surfaces. Lower solderable surfaces for the same amount of paste will have higher solder joint volume; therefore; higher shear force. It is also noticeable from this and other plots (not shown here) that the distributions for the 125 aging-hour interval were different from the rest. This is apparent for resistors, shear forces have much wider variations with its distribution crossing the Weibull distributions for as build and after 500 aging hours. Abnormality for shear behavior after the early stage of aging has also been shown for other packages [11]. To better define trend, data for this aging interval was intentionally removed from the other plots.



**Figure 9 Shear force Weibull plots for HASL surface finish, tin-lead paste, matched and unmatched pad aperture combination**

Figures 10 and 11 show shear force Weibull plots for lead-free PWB surface finish assembled using lead-free solder paste. A 4.65 thick stencil with a 90% aperture size and different pad-aperture combination were used in the assembly process. Passive devices with horizontal orientation were considered for shear testing.

It is evident from these figures that except for ENIG finish, shear force for resistor on different surface finishes are better than capacitors. Generally, the 50 percentile shear forces decrease with aging time for capacitor and resistor assemblies on all surface finishes. For the lower percentile shear forces; however, the trend is not as distinguishable as those for the higher percentiles. This is clearly apparent for capacitors

assembled on ENIG pad surface finish showing narrower distribution for those aged. The intermetallic growth aspect of microstructure features are discussed in another paper [3]. Purely from Weibull distribution, it can be inferred that intermetallic formed for this surface becomes more brittle and causes much narrower distribution as isothermal aging progress.

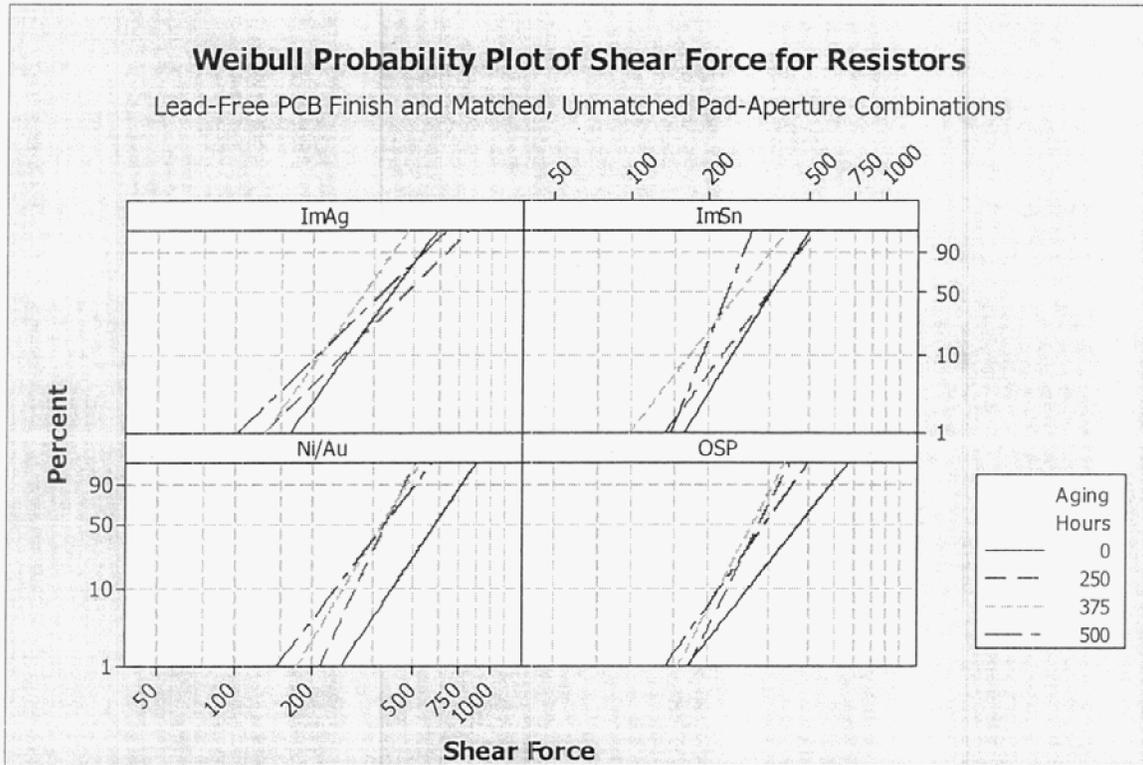
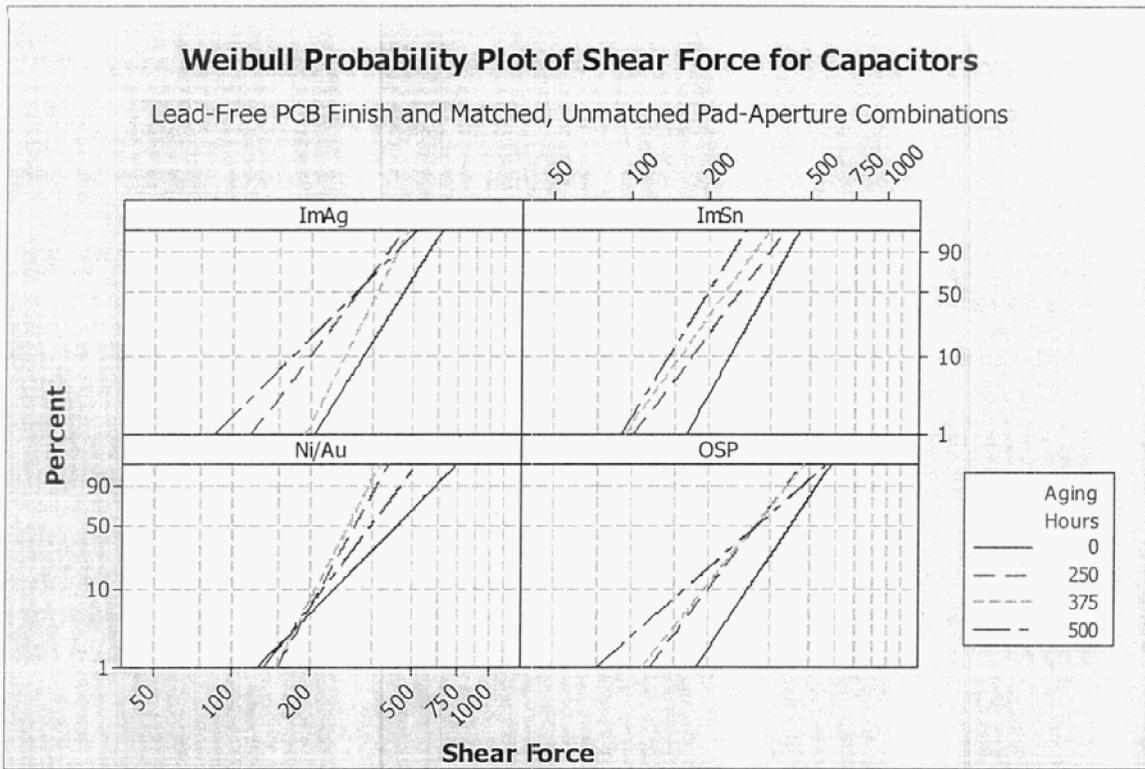


Figure 10 Shear force Weibull plots for lead-free solder resistor assembly and various surface finishes



**Figure 11 Shear force Weibull plots for lead-free solder resistor assembly and various surface finishes**

Representative of microstructural changes with aging progress for two key surface finishes, ENIG and ImAg for resistors are shown in Figures 12 and 13. Both surface finishes show severe microstructural damage with increase in aging. More cracking with voids were observe starting under the package for the assemblies with ENIG surface finish.

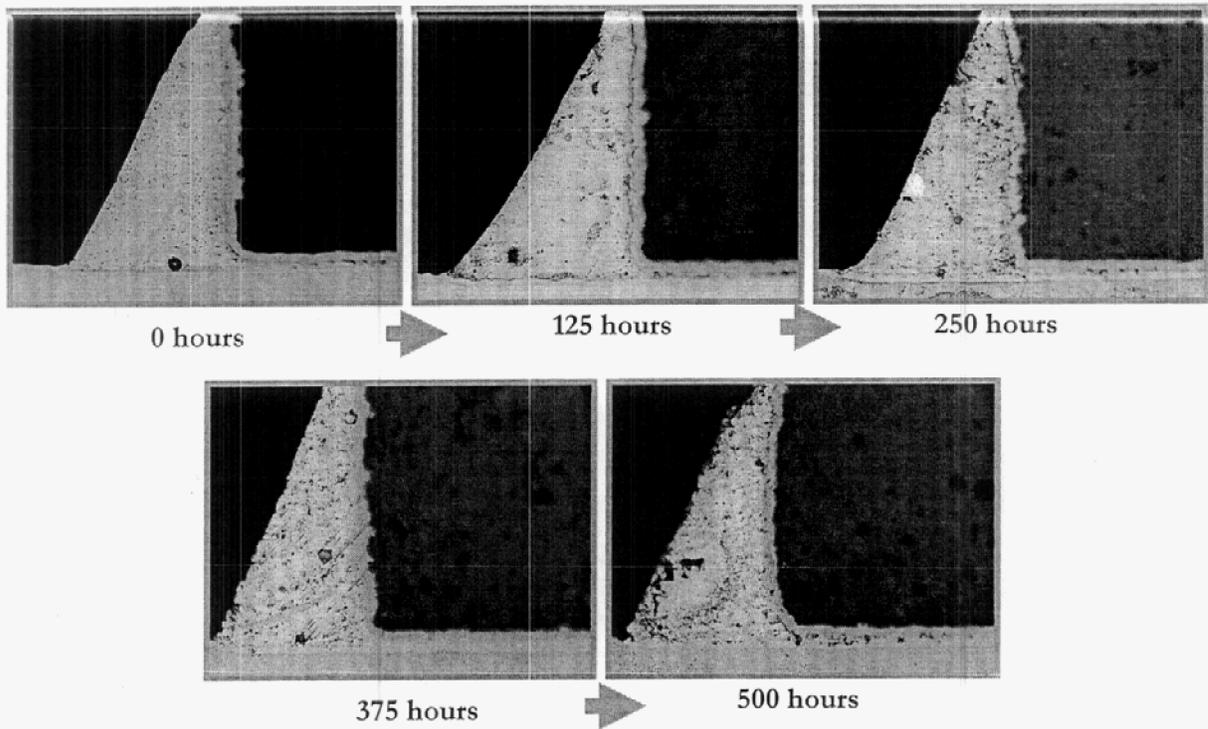


Figure 12 Microstructural changes with aging time at 150° for the 0201 assemblies on pads with ImAg surface finish

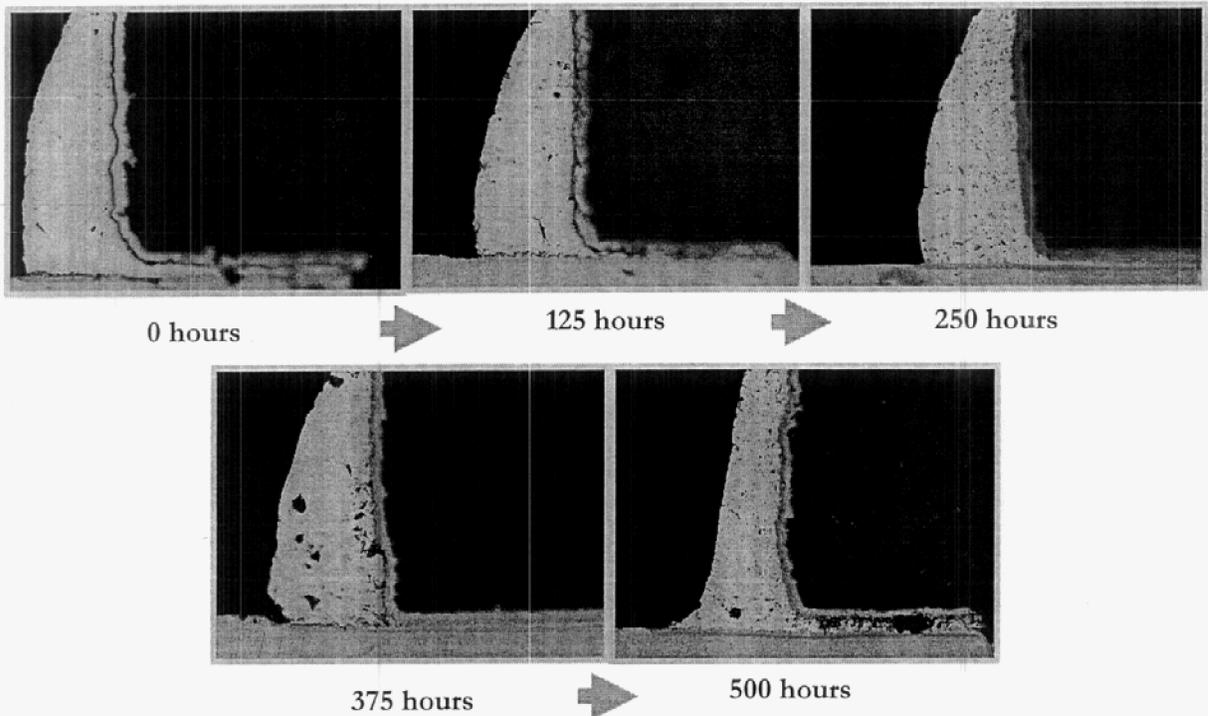
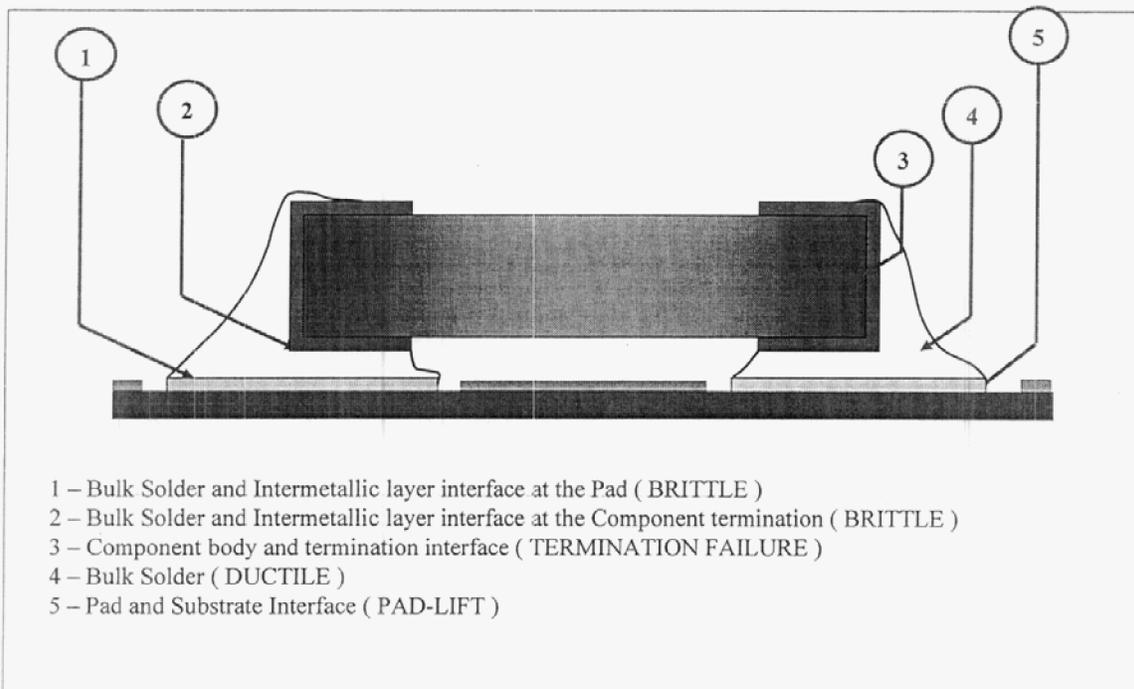


Figure 13 Microstructural changes with aging time at 150° for the 0201 assemblies on pads with ENIG surface finish

The modes of fractures were also recorded for all assemblies after shear tests. Fractures were categorized into five modes as shown in Figure 14. Relative failure modes for all surface finishes including ENIG and ImAg for all aging intervals are shown in Figure 15. Solder joints of horizontal resistors formed using a 4.65 thick stencil with a 90% aperture size, including both matched and unmatched pad-aperture combination are considered for failure modes study. This figure clearly illustrates the different failure modes for the solder joints formed for each PWB finish. It reveals that HASL surface finish is the most ductile having higher ductile failure and lowest brittle failure whereas ENIG had the highest brittle failure modes. The ENIG brittle failure modes further confirm the narrowing Weibull distribution with aging as discussed. It is interesting to note that ImAg, had the highest pad lifting, therefore, the shear distribution may be more representative of pad adhesion behavior with aging. This failure mode can not be projected from the Weibull distributions for shear force however.



**Figure 14 Possible sites for failure during shear testing**

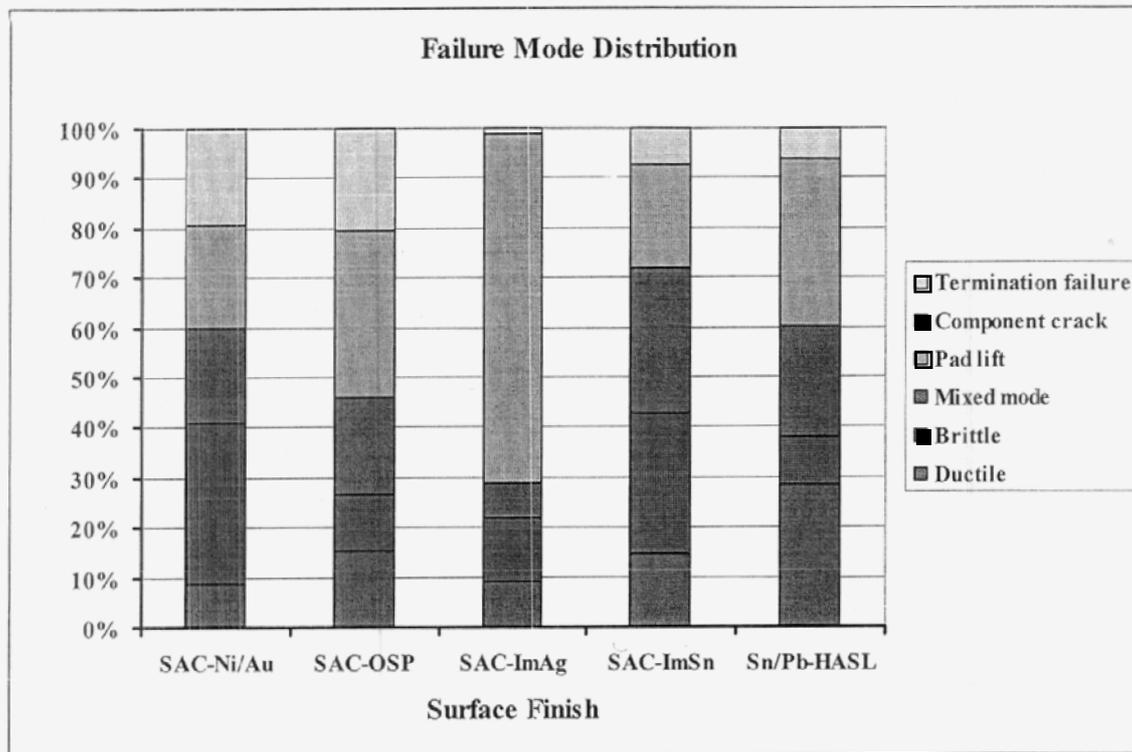


Figure 15 Shear testing failure modes for assemblies with tin-lead and lead-free solder alloys and different surface finishes

### 5.3 Thermal Cycling Approach

An industry-wide guideline document, IPC SM785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, for accelerated reliability testing of solder attachment has been around for more than a decade. Only recently, the industry has agreed to release an industry-wide specification, IPC 9701 [9], in response to area array technology implementation and to provide a standard procedure, failure analysis, and data report for solder joint reliability testing. The newest revision, IPC9701A, includes guidelines for lead-free solder alloys.

A few of the test vehicles from this experiment were subjected to the thermal cycle range commonly used by NASA and also specified in IPC 9701. The cycling was done at the NASA-JPL facility and the author has documented the test results under this thermal cycling condition for area array packages [10, 11]. The 0201 assembled test vehicles were those that have ImAg and ENIG surface finishes and have lead-free solder interconnects. The cycling condition ranged from  $-55$  to  $100^{\circ}\text{C}$  with  $3\text{-}10^{\circ}\text{C}/\text{min}$  heating/cooling rate and dwell of at least 10 minutes at extreme temperatures.

Because of the lack of daisy chaining, especially for capacitors, the assemblies were not continuously monitored as specified by IPC-9701. However, they were removed at intervals and visually inspected by an optical microscope. Assemblies with 0201 resistors

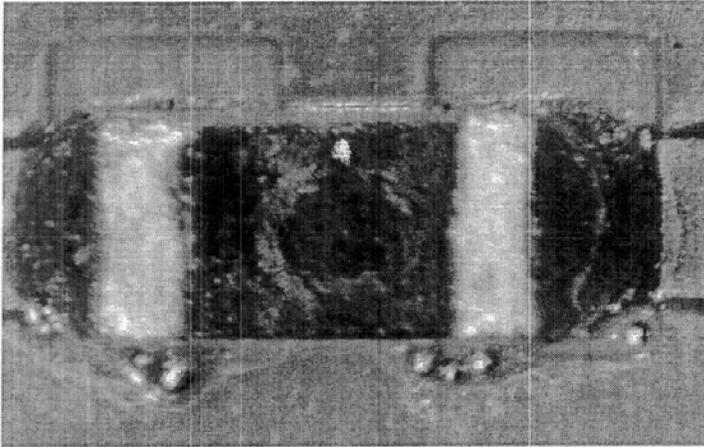
were selectively monitored for resistance changes. These – as well as microstructural characterization after 1500 thermal cycles – were documented. In addition, a number of assemblies were subjected to shear test both along the width and length to characterize behavior. For correlation of thermal cycle shear data to isothermal aging, it was needed to correlate the shear test results between the two facilities. The remainder of test vehicles was sent to Rochester Institute of Technology (RIT) for additional shear tests.

#### **5.4 Thermal Cycle Test Results**

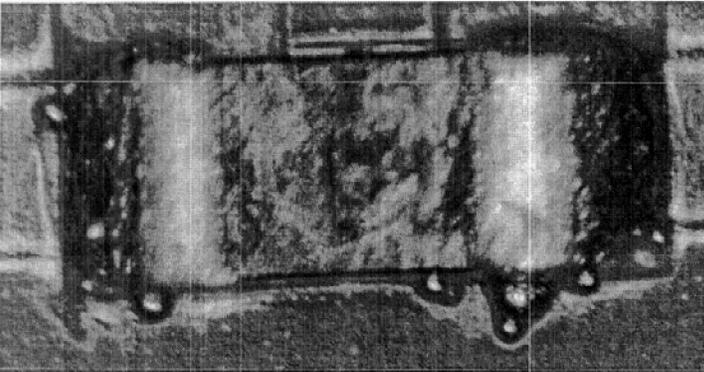
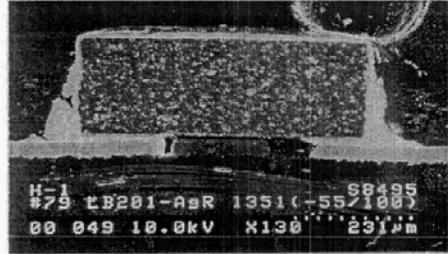
A solder joint has three primary layers of attachment, namely, (1) intermetallic layer at component metallization, (2) the solder bulk, and (3) intermetallic layer at the copper pad. The intermetallic layers are brittle and have the least chance for plastic deformation when the joint is sheared. The only layer of attachment undergoing plastic deformation is therefore the solder bulk. Plastic deformation here pertains to the thermo-mechanical fatigue experienced by solder joints subjected to thermal cycling. The growth in the intermetallic layers reduces the solder bulk component of the joint and leads to areas of stress concentration. As a result, the bulk solder standoff providing compliance to thermo mechanical fatigue is reduced, affecting the fatigue resistance of the joint.

Figures 16 and 17 show the optical microscopy photographs taken at various thermal cycling stages for a capacitor and resistor assembly, respectively. This figure also includes the SEM photomicrographs of the same assemblies prior to and after cross-section at 1500 cycles. Except for solder balls that are clearly apparent, because of small feature of 0201, it is difficult to capture the details of microstructural changes by optical microscopy. When assemblies were removed for visual inspection, a limited number of daisy-chain resistors were also manually measured for resistance changes. Out of a total of 8 daisy chains for the three test vehicles, only one failed at about 1200 thermal cycles. The failed daisy chain was for the test vehicle with modified home plate pad design, ENIG surface finish, lead-free paste, and 80% aperture. Since test vehicles were not built for thermal cycling and monitoring, there might have been other failures that were not included in the monitoring. SEM photographs of the same assemblies clearly show that for the acceptable condition, minimum degradation are induced due to 1500 thermal cycles in the range of -55/100°C.

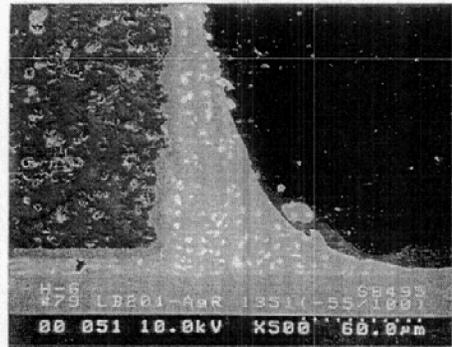
Figure 18 shows SEM photomicrograph of assemblies taken after 1500 thermal for the lead-free solder joints on ENIG or ImAg pads surface finishes. There are signs of sporadic microcracks from the outer surface and under package with no one single being significant. A portion of the assemblies that were subjected to thermal cycling were also shear tested. The results before after 1500 thermal cycles for ENIG and ImAg surface finishes are shown in Figure 19. Significant drops in shear force shown in this figure can not be verified by microstructural changes shown in previous figures. The shear force trend before and after 1500 thermal cycle; however, remain unchanged with ENIG surface finish show higher force than ImAg.



a) Resistor with tin-lead solder joint As fabricated (ID 79)

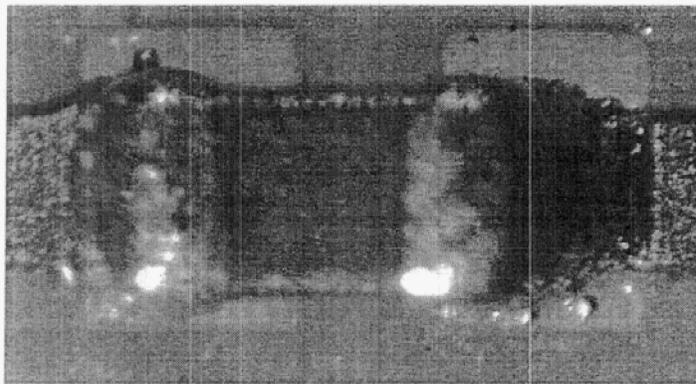


b) 400 thermal Cycles (-55/100°C)

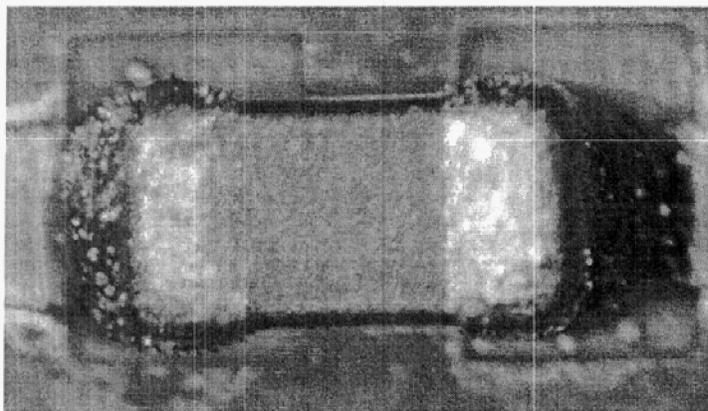
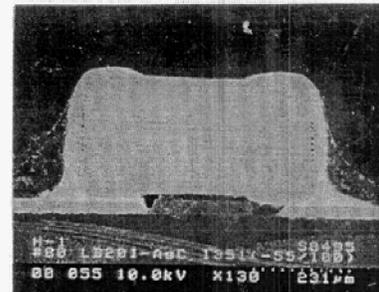


c) 1500 Thermal Cycles

Figure 16 Optical and SEM photomicrographs of a resistors assemblies taken at various thermal cycle intervals (-55/100°C)



a) capacitor with tin-lead solder joint  
As fabricated (ID 80)

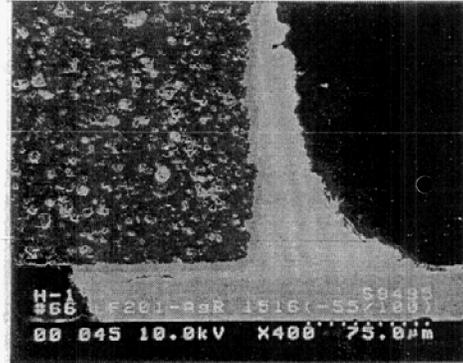
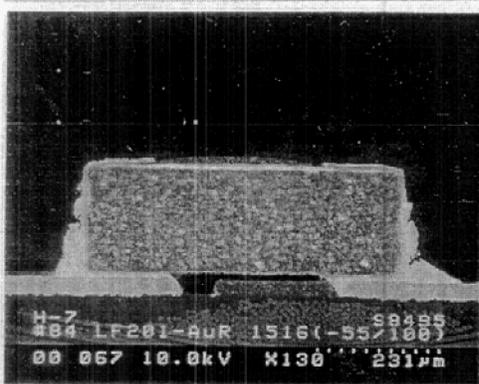
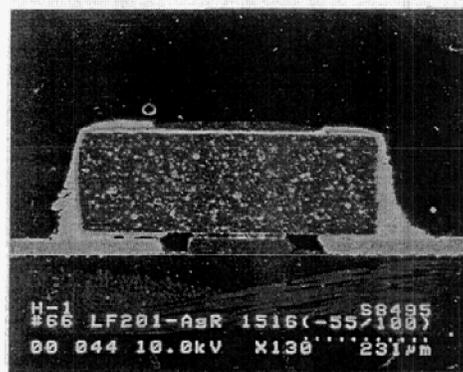
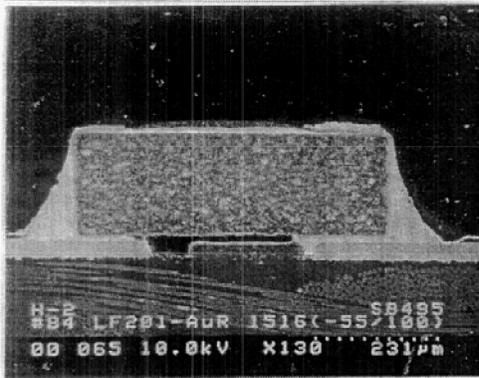


b) 400 thermal Cycles (-55/100°C)



c) 1500 Thermal Cycles

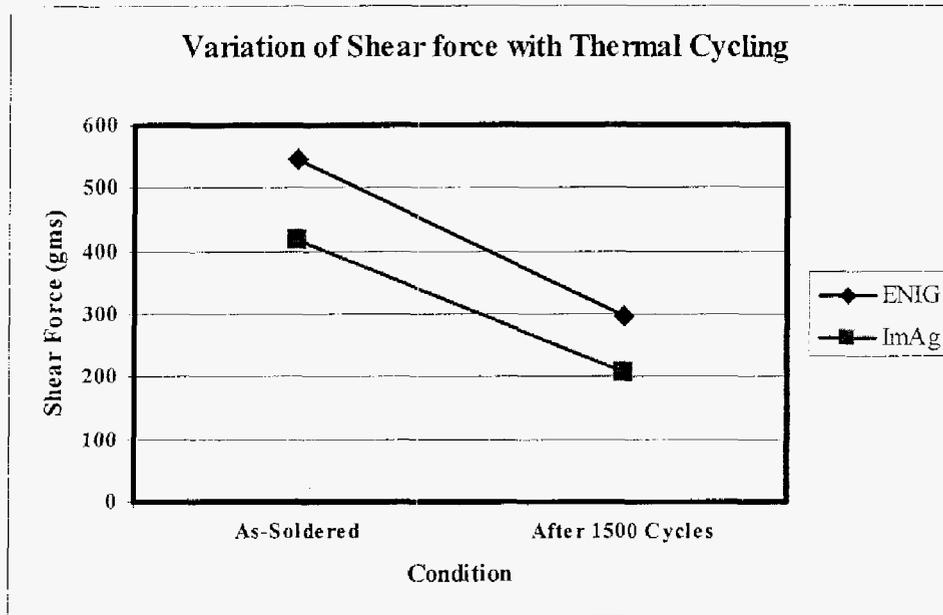
Figure 17 Optical and SEM photomicrographs of a capacitor assemblies with ImAg surface finish taken at various thermal cycle intervals (-55/100°C)



a) LF ENIG (ID 84)

b) LF ImAg (ID 66)

Figure 18 SEM photomicrographs of resistors assembled with ENIG and ImAg surface finishes at 15000 cycles (-55/100°C)



**Figure 19 Shear force variation for thermally cycled assemblies on pads with ENIG and ImAg finishes**

## 6. Conclusions

This investigation identified a number of key factors pertaining to manufacturing parameters and behavior under isothermal and thermal cycling for environmental tests. Only a few key ones are given below.

- Solder beading is the most prominent defect. The 80% aperture size provides a low percentage of the solder beading defect, whereas 100% aperture size provides a low percentage of the skewing defect.
- Shear testing of thermally-aged assemblies reveals that SAC paste with ENIG finish requires the highest shear force, followed by ImAg and OSP. ImSn finish required the least shear force. For ENIG surface finish, Weibull distribution trends with aging somewhat different from the other assemblies.
- Shear testing of thermally-cycled assemblies reveals that SAC with ENIG finish outperforms SAC with ImAg finish.
- For an acceptable assembly condition, minimum damage occurs due to thermal cycling in the range of -55 to 100°C based on microstructural change somewhat in contrast with shear force reduction trend.

## 7. Acknowledgement

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