

Design for ASIC Reliability for Low-Temperature Applications

Yuan Chen,¹ Mohammad Mojaradi,¹ Lynett Westergard,² Curtis Billman,²
Scott Cozy,¹ Gary Burke,¹ and Elizabeth Kolawa¹

¹Jet Propulsion Laboratory, California Institute of Technology

4800 Oak Grove Drive, Mail Stop 303-230, Pasadena, CA 91109

Phone : 818-393-0940, Fax: 818-393-4559, Email: yuan.chen@jpl.nasa.gov

²AMI Semiconductors, 2300 Buckskin Rd, Pocatello, ID 83201

INTRODUCTION

Electronics in automotive, military and space applications are often required to operate in low-temperature environments. It is well-known that at low temperatures, hot carrier aging is the primary intrinsic reliability concern [16]. A transistor designed for a temperature range of 27°C to 125°C with a 10-year carrier lifetime has a decreased lifetime at low temperatures; therefore, may not meet the 10-year lifetime requirement when operated below room temperature (RT).

Generally, worst-case hot carrier analysis has been used during process and technology qualification as well as product qualification. This worst-case analysis usually only considers the N-channel metal-oxide semiconductor (NMOS) transistor hot carrier aging lifetime estimated under worst-case condition, i.e., maximum substrate current and minimum operating temperature. However, the worst-case hot carrier aging analysis approach typically gives a very conservative or, in some cases, a too pessimistic prediction of NMOS lifetime. Therefore, a new methodology is desired and required to ensure the long-term reliability of electronics in low-temperature ranges.

In this paper, we present a methodology to design for reliability for low temperature applications without requiring process improvement. The developed hot carrier aging lifetime projection model takes into account both the transistor substrate current profile and temperature profile to determine the minimum transistor size needed in order to meet reliability requirements. The methodology is applicable for automotive, military, and space applications, where there can be varying temperature ranges. A case study utilizing this methodology is given to design for reliability into a custom application-specific integrated circuit (ASIC) for a Mars exploration mission.

DESIGN-FOR-RELIABILITY METHODOLOGY

There are several proposed techniques of designing for hot carrier reliability [7-12], either from the process or circuit design point of view. Generally, altering the process is not feasible and circuit design changes should be kept to a minimum as well. Therefore, evaluating the hot carrier aging impact on existing technology and choosing the most applicable size transistors becomes the most cost-efficient way to design for reliability under low temperature applications.

To determine the size of the transistors, extrapolation of hot carrier aging lifetime from testing conditions to use condition is required. We argue that temperature dependence of both substrate current and hot carrier aging lifetime need to be considered. The worst-case analysis approach, basically depends on the lowest

temperature and maximum substrate current, is not realistic or appropriate.

The assumptions for the proposed methodology are that (1) the degradation resulting from hot carrier aging is cumulative and (2) there is negligible annealing effect at higher temperatures. The input information to be determined is I_{sub} temperature dependence, I_{sub} profile, and operation temperature profile.

I_{sub} temperature dependence

Substrate current is temperature dependent and since hot carrier aging lifetime is a function of substrate current, substrate-current temperature dependence is one of the most important factors needed, and is normally determined from experiments.

I_{sub} profile

Typically, the expected hot carrier aging lifetime t_{50} is a function of substrate current I_{sub} .

During digital circuit switching and analog circuit operation, I_{sub} is not a constant value but changes over time. During circuit switching or clock time, I_{sub} versus time is defined as an I_{sub} profile and can be determined by circuit simulation and/or experiments. Each I_{sub} profile can be divided into j small time intervals, where a constant substrate current I_{sub} is assumed during each time interval t_j .

During each time interval t_j , the NMOS transistor should have an expected lifetime, t_{50} , under a certain I_{sub} ; however, the transistor is biased under this I_{sub} only for a period of t_j . Therefore, a small percentage of the NMOS transistor lifetime is consumed during the time interval t_j and the percentage can be then expressed as

$$\% \text{ life consumed in } t_j = \frac{t_j}{t_{50}(I_{sub})} * 100\% \quad (1)$$

t_{50} is the expected device hot carrier aging lifetime under the I_{sub} in the time interval t_j . The percentage of the device hot carrier aging lifetime consumed during one I_{sub} cycle is given by

$$\% \text{ life consumed in one } I_{sub} \text{ cycle} = \sum_{m=1}^j \frac{t_m}{t_{50}(I_{sub,m})} * 100\% \quad (2)$$

Operating temperature profile

The operating temperature profile shows the expected temperature changes over time under use conditions. The profile

can be the temperature change over a day, a month, a year, or any time span.

Similar to the I_{sub} profile, the operating-temperature profile is divided into k intervals, where each interval is one I_{sub} profile cycle, assuming the I_{sub} cycle is typically very small since I_{sub} is a function of temperature. Again, a constant temperature can be assumed for each I_{sub} cycle and the percentage of the device hot carrier aging lifetime consumed during one operating temperature profile is as follows:

$$\% \text{ life consumed in one Temp profile} = \sum_{n=1}^k \sum_{m=1}^j \frac{t_{m,n}}{t_{50}(I_{sub,m}, T_n)} * 100\% \quad (3)$$

Assume the operating temperature profile is the temperature changes over a day and the reliability requirement of a circuit is D days; then the percentage of device hot carrier aging lifetime taken during D days is given by:

$$\% \text{ life consumed in } D \text{ days} = D * \left(\sum_{n=1}^k \sum_{m=1}^j \frac{t_{m,n}}{t_{50}(I_{sub,m}, T_n)} \right) * 100\% \quad (4)$$

Minimum channel length

By setting (4) equal to one, we can determine the number days, given by (5), that the device can survive from the hot carrier aging point of view. Therefore, the design rule is to choose an NMOS transistor channel length to satisfy the following expression with any desirable margin:

$$D > \left(1 / \sum_{n=1}^k \sum_{m=1}^j \frac{t_{m,n}}{t_{50}(I_{sub,m}, T_n)} \right) \quad (5)$$

CASE STUDY

Future Mars exploration missions can expose NASA spacecraft or probes to a local environment with temperatures from -135°C to $+90^{\circ}\text{C}$. NASA's traditional solution in extreme environments has been to keep the electronics operating in a limited temperature range by housing them in a "warm-electronics-box"; however, this is not viable for next-generation robotics and rovers, where electronics are placed at the point of use or next to loads directly exposed to the environment.

One future Mars mission requires an ASIC design that uses $0.6\text{-}\mu\text{m}$ commercial complementary metal-oxide semiconductor (CMOS) technology with 5.0 V nominal V_{dd} and a 5-year lifetime on its critical path under a temperature range of -120°C to $+80^{\circ}\text{C}$.

Experiment details

First, hot carrier aging tests were performed on the $0.6\text{-}\mu\text{m}$ NMOS and PMOS transistors at RT, -100°C , and -150°C . At -100°C and -150°C , the bias conditions include $V_{ds} = 6.5\text{ V}$, 6.0 V and 5.5 V , with $V_{gs} = 2.0\text{ V}$, 2.2 V , 2.4 V , 3.5 V , and 5.0 V to cover both maximum and non-maximum I_{sub} conditions. It was observed that PMOS hot carrier aging lifetime was two orders of magnitude greater than NMOS lifetime; therefore, the minimum channel length determination was focused on NMOS.

During hot carrier aging tests, the parametric characteristics, i.e., saturation current I_{dsat} , linear current I_{dlin} , threshold voltage V_{th} , and transconductance g_m , were extracted from the I_{ds} versus V_{ds} and V_{gs} curves. Figures 1(a), (b) and (c) show the change of I_V curves and parametric shift during the hot carrier aging tests under $V_{ds} = 6.5\text{ V}$ at -150°C .

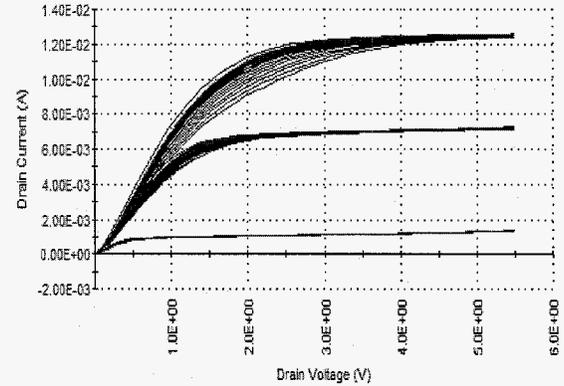


Figure 1(a). I_{ds} versus V_{ds} curves during HCA at -150°C .

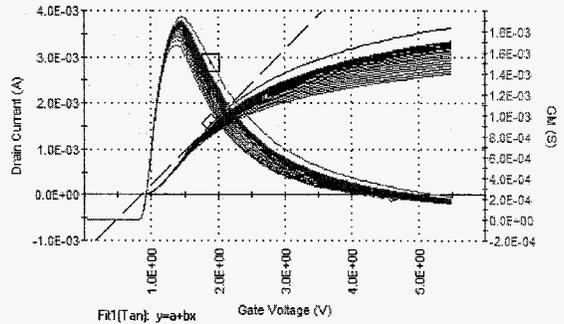


Figure 1(b). I_{ds} versus V_{gs} curves during hot carrier aging at -150°C .

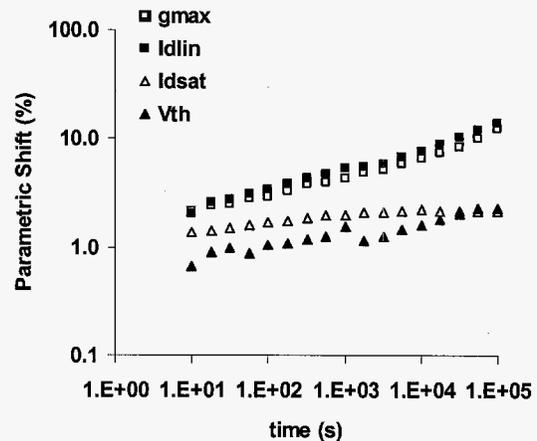


Figure 1(c). Parametric shift during hot carrier aging at -150°C .

The hot carrier aging tests performed at -150°C showed that I_{dlin} and g_{max} degraded faster than the other parameters, and that I_{dsat} saturated around 1.3 to 1.4 %. This indicated that the digital portion of the ASIC circuitry was not the limiting factor for the hot carrier aging mechanisms under low temperatures for this technology. Consequently, the critical analog circuit paths of the

ASIC circuit blocks, including ADC, DAC and voltage regulator, needed to be analyzed to determine the transistor failure criteria. Typically, threshold mismatch has a mean standard deviation from 1 to 20mV. Therefore, to be conservative, we consider a 30mV mismatch of threshold voltages in a differential pair as circuit failure criterion, and this is equivalent to a 3% threshold change or, in this case, a 15% maximum transconductance (g_{max}) change during the hot carrier aging.

Figure 2 shows g_{max} degradation versus time for RT and -150°C hot carrier aging tests. These degradation results have a similar slope, which indicates the degradation mechanism is the same over this temperature range.

Using 15% g_{max} degradation as the failure criterion, Figure 3 shows the transistor hot-carrier lifetime versus I_{sub} plot for data taken at RT, -100°C , and -150°C , indicating that the lifetime can be expressed as a function of substrate current.

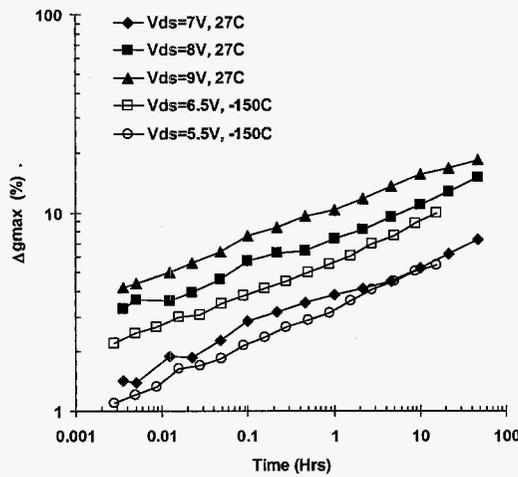


Figure 2. g_{max} shift during hot carrier aging at RT and 150°C .

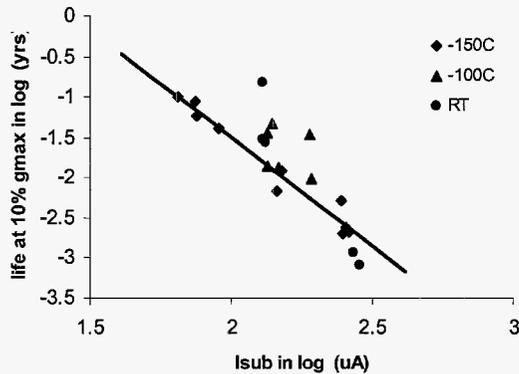


Figure 3. NMOS lifetime versus I_{sub} at RT, -100°C and -150°C .

Hot carrier aging tests were also performed at room temperature on the NMOS transistors with different channel lengths of 0.5, 0.6, 0.7 and 0.8 μm to obtain channel length dependence. Figure 4 shows the hot carrier aging lifetime versus $1/V_{ds}$ for the devices with four different channel lengths.

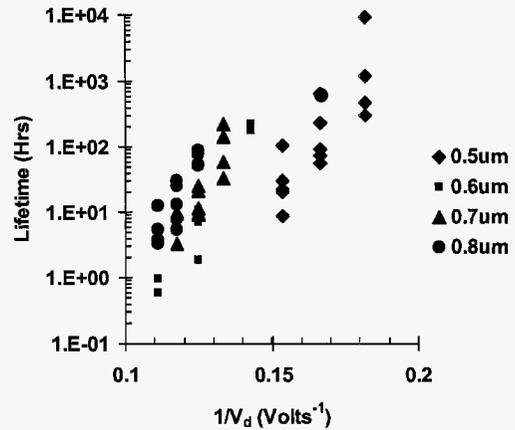


Figure 4. Hot carrier aging tests at RT for NMOS transistors with different channel lengths.

Based on the information in Figure 4, the hot carrier aging lifetime was extrapolated to 5 V and plotted against channel length, as shown in Figure 5. This channel length dependence will be used in simulation for channel-length determination.

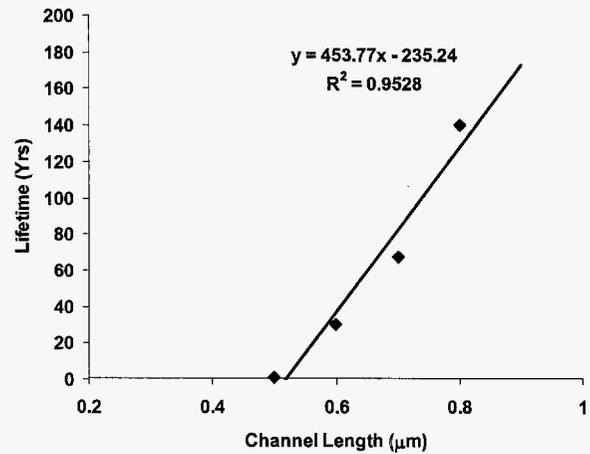


Figure 5. Channel-length dependence at RT.

Simulation

The temperature profile on Mars depends on landing location and spacecraft design. The temperature profile of the mission is determined to be -120°C to $+80^{\circ}\text{C}$, with a sinuous shape. The hot carrier aging lifetime of the NMOS transistors needs to be projected beyond 5 years under the Mars temperature profile to ensure mission success.

The substrate current (I_{sub}) profile during transistor switching and typical operating conditions was simulated. The Mars temperature profile was then divided into k intervals, where each interval was one I_{sub} profile cycle and each Mars temperature profile cycle was one Martian day.

Based on substrate current profile, temperature profile and channel length dependence, Figure 6 shows the projected hot carrier aging lifetime on the ASIC as a function of channel length under the Mars temperature profile. Using this methodology, the minimum

channel length to achieve the 5 year mission can be determined as 0.8 μm for the ADC, DAC and voltage regulators of the ASIC.

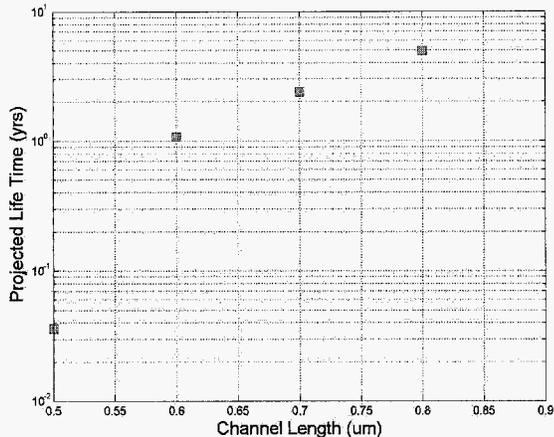


Figure 6. An example of the projected NMOS hot carrier aging lifetime under a Mars temperature profile.

SUMMARY

We have presented a methodology for designing reliability into electronics that will be operated under low-temperature applications. The hot-carrier lifetime extrapolation model takes account of the evaluation of the hot carrier aging impact on the technology, analysis and simulation of circuit critical path and the determination of minimum channel length for critical transistors. This methodology can be applied to other transistor-level failure and/or degradation mechanisms for applications with a varying temperature ranges.

ACKNOWLEDGEMENTS

The author would like to thank Jonathon Perret and Travis Johnson of JPL for invaluable technical discussions on the ASIC design and system applications and for the support from AMI Semiconductor.

This work was carried out at Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

REFERENCES

1. F. Balestra, G. Ghibaudo, "Device and circuit cryogenic operation for low temperature electronics," Kluwer Academic Publishers, 2001.
2. S. L. Von Bruns and R. L. Anderson, "Hot-electron-induced interface state generation in n-channel MOSFET's at 77K," *IEEE Transactions on Electron Devices*, vol. ED-34, p. 75, 1987.
3. S. B. Bibyk, H. Wang and P. Borton, "Analyzing hot-carrier effects on cold CMOS devices," *IEEE Transactions on Electron Devices*, vol. ED-34, p. 83, 1987.
4. A. Acovic, M. Dutoit, M. Ilegems, "A study of the increased effects of hot-carrier stress on NMOSFET's at low temperature," *IEEE Transactions on Electron Devices*, vol. ED-36, p. 2603, 1989.
5. M. Song, K. P. MacWilliams, J. C. S. Woo, "Comparison of NMOS and PMOS hot carrier effects from 300 to 77K," *IEEE Transactions on Electron Devices*, vol. ED-44, p. 268, 1997.
6. J. Wang-Ratkovic, et al., "New understanding of LDD CMOS hot carrier degradation and device lifetime at cryogenic temperatures," *IRPS*, 1997.
7. M. Chen, C. Leung, W.T. Cochran, W. Jungling, C. Dziuba, T. Yang, "Suppression of hot carrier effects in submicrometer CMOS technology," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, December, 1988.
8. I.C. Kizilyalli, G.C. Abeln, Z. Chen, J. Lee, G. Weber, B. Kotzias, S. Chetlur, J.W. Lyding, K. Hess, "Improvement of hot carrier reliability with deuterium anneals for manufacturing multilevel metal/dielectric MOS systems," *IEEE Electron Device Letters*, Vol. 19, No. 11, November, 1998.
9. W.R. Tonti, W.P. Noble, W.W. Abadeer, S.W. Mittl, "Doping profile design for substrate hot carrier reliability in deep submicron field effect transistors," *IRPS*, 1991.
10. C. Chang, K. Wang, M. Marek-Sadowska, "Layout driven hot carrier degradation minimization using logic reconstructing techniques," *Design Automation Conference*, 2001.
11. K.N. Quader, E.R. Minami, W. Huang, P.K. Ko, C. Hu, "Hot carrier reliability design guidelines for CMOS logic Circuits," *IEEE Journal of Solid State Circuits*, Vol. 29, No. 3, March 1994.
12. E. Xiao, "A design technique to reduce hot carrier effect", *IRW*, 2003.