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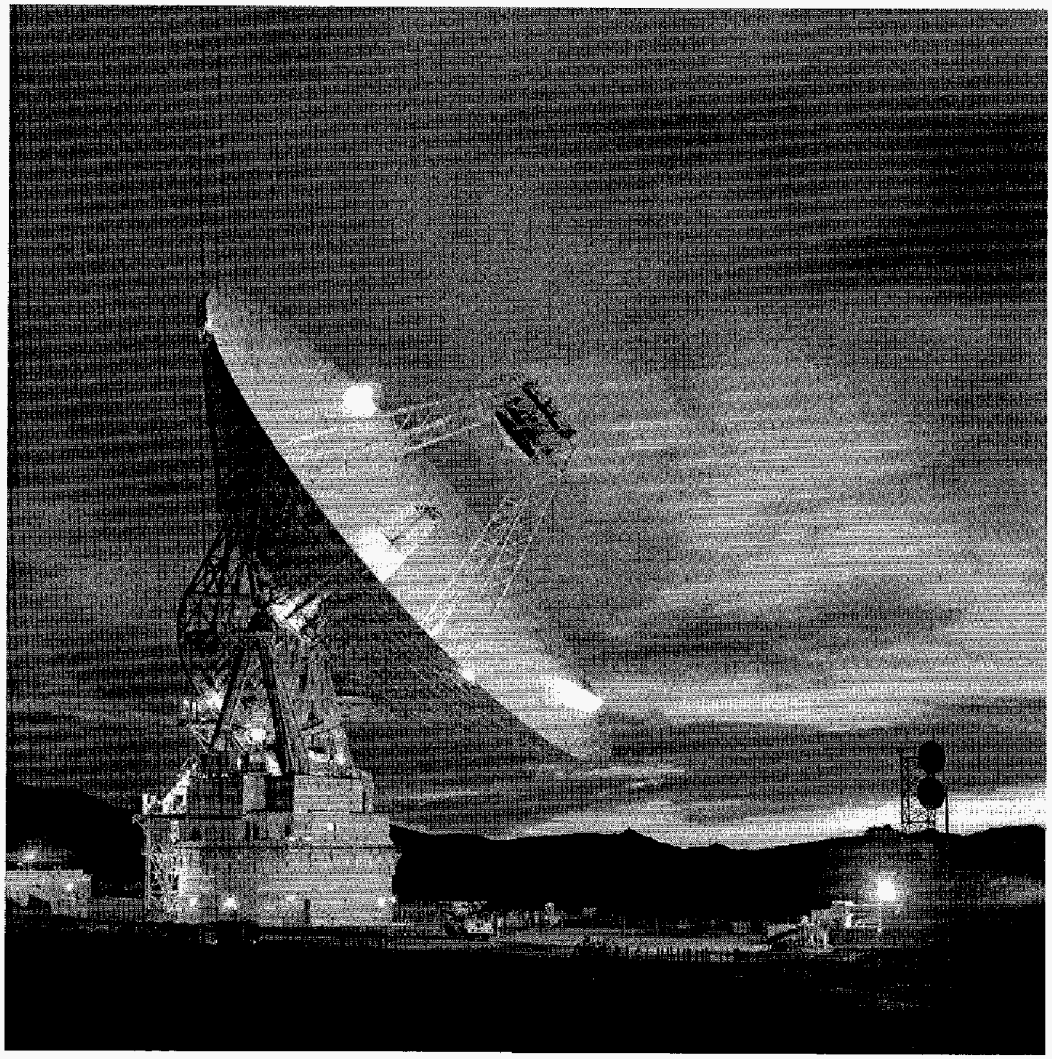

DEEP SPACE NETWORK TURBO DECODER IMPLEMENTATION

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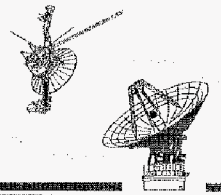
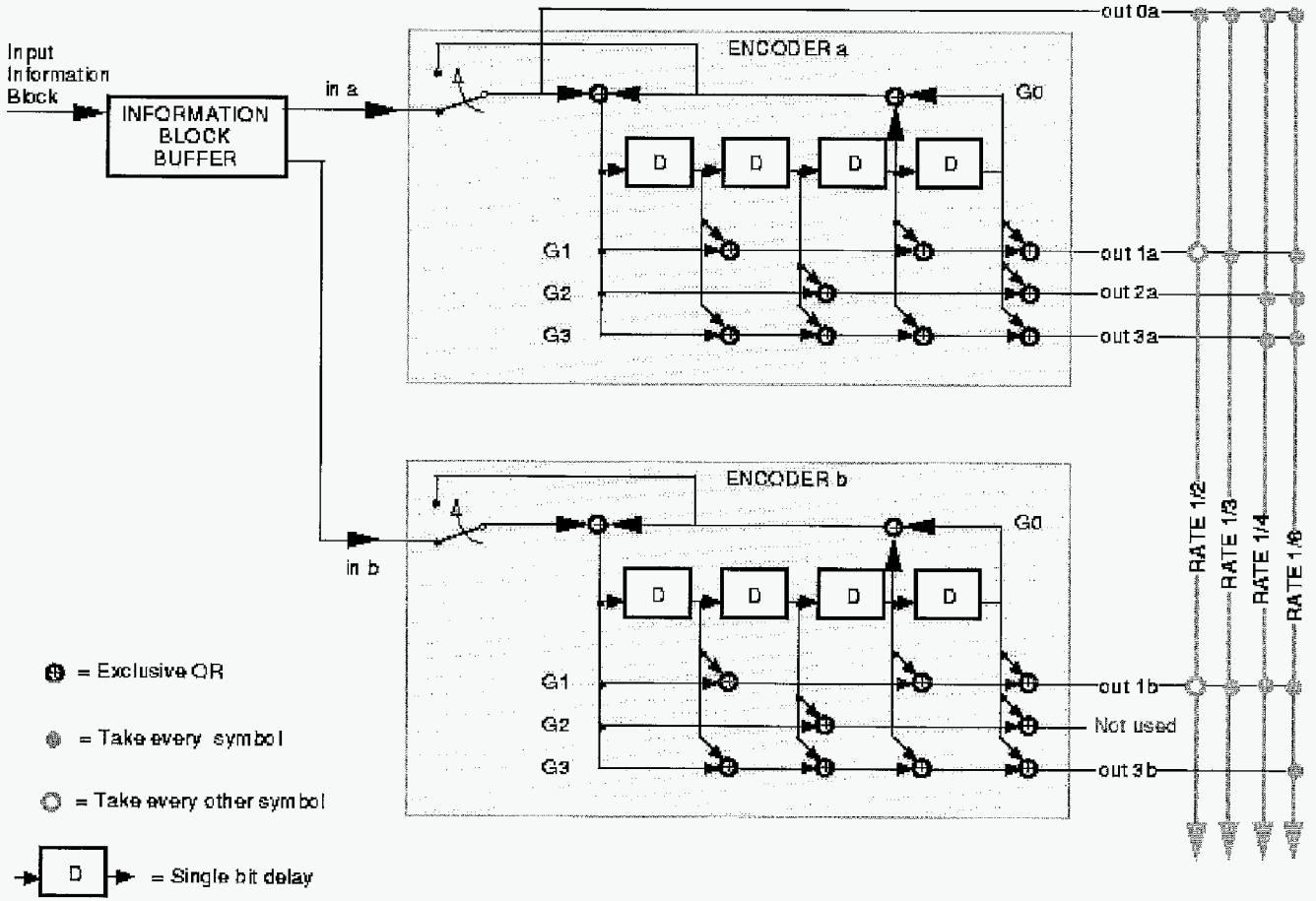
WHAT ARE TURBO CODES?

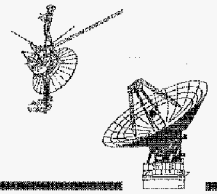


- TURBO CODES ARE A NEW CLASS OF ERROR CORRECTING CODES THAT HAVE BEEN APPROVED BY THE CCSDS
- THEY ARE BLOCK CODES THAT ARE GENERATED BY TWO CONSTRAINT LENGTH 4 CONVOLUTIONAL CODES
  - ONE OF THE CONVOLUTIONAL CODES OPERATES ON A PERMUTATED SET OF SOURCE BITS
- THERE ARE FOUR FRAME SIZES CURRENTLY DEFINED: 1784, 3568, 7136, AND 8920 BITS
- THERE ARE FOUR CODING RATES DEFINED: 1/2, 1/3, 1/4, AND 1/6
- THE CCSDS TURBO CODES ARE SYSTEMATIC (THE UNENCODED BITS ARE PRESENT IN THE CODEBLOCKS)
- TURBO CODES ARE NOT TRANSPARENT (POLARITY INVERTED BLOCKS ARE NOT CODEWORDS)

ENCODER BLOCK DIAGRAM

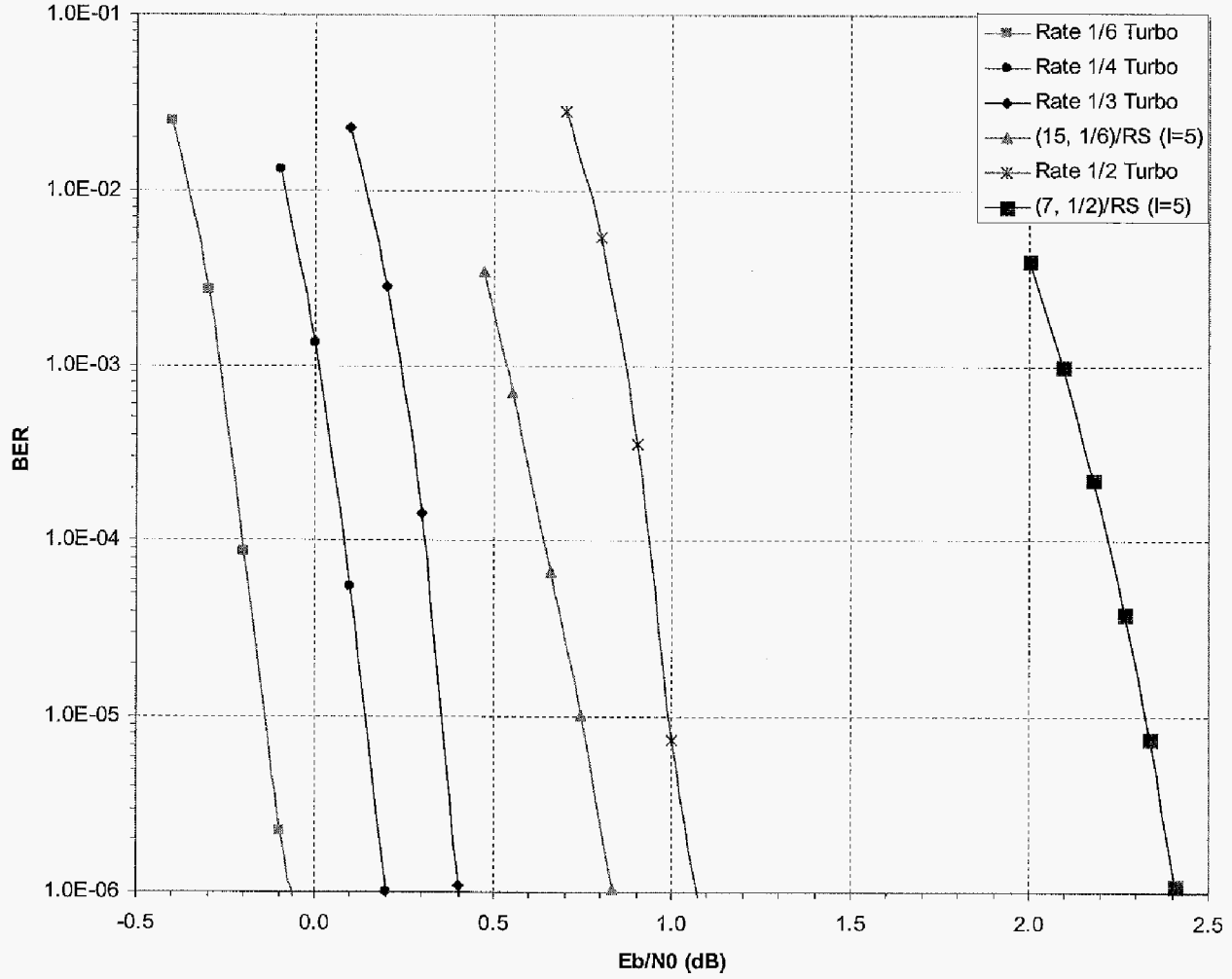


TURBO CODE ADVANTAGES

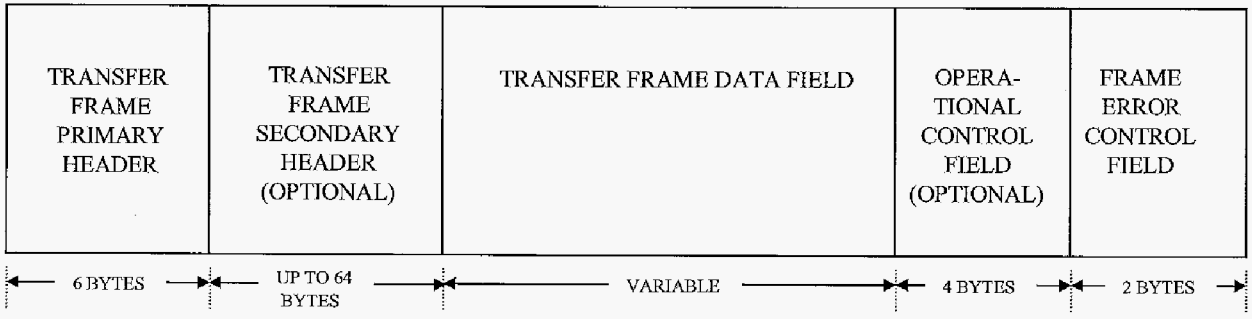


- PERFORMANCE GAIN
  - RATE 1/6 TURBO CODE IS 0.8 dB BETTER THAN (15, 1/6) CONVOLUTIONAL CODE CONCATENATED WITH REED-SOLOMON CODE
  - RATE 1/3 TURBO CODE IS 0.4 dB BETTER
- CCSDS COMPLIANCE
  - PROVIDES INTEROPERABILITY OPTIONS NOT AVAILABLE WITH (15, 1/6) CODE (WHICH IS NOT A STANDARDIZED CODE)
- DECODER COMPLEXITY
  - DECODING ALGORITHM FOR (15, 1/6) CODE IS APPROXIMATELY 10 TIMES MORE COMPLEX
  - CAN IMPLEMENT TURBO DECODING IN SOFTWARE RUNNING ON COMMERCIAL DSPs
    - (15, 1/6) DECODER REQUIRED CUSTOM ASIC IMPLEMENTATION

BIT ERROR RATE (8920 BIT FRAME)

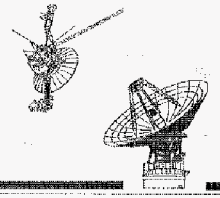


TURBO BLOCK



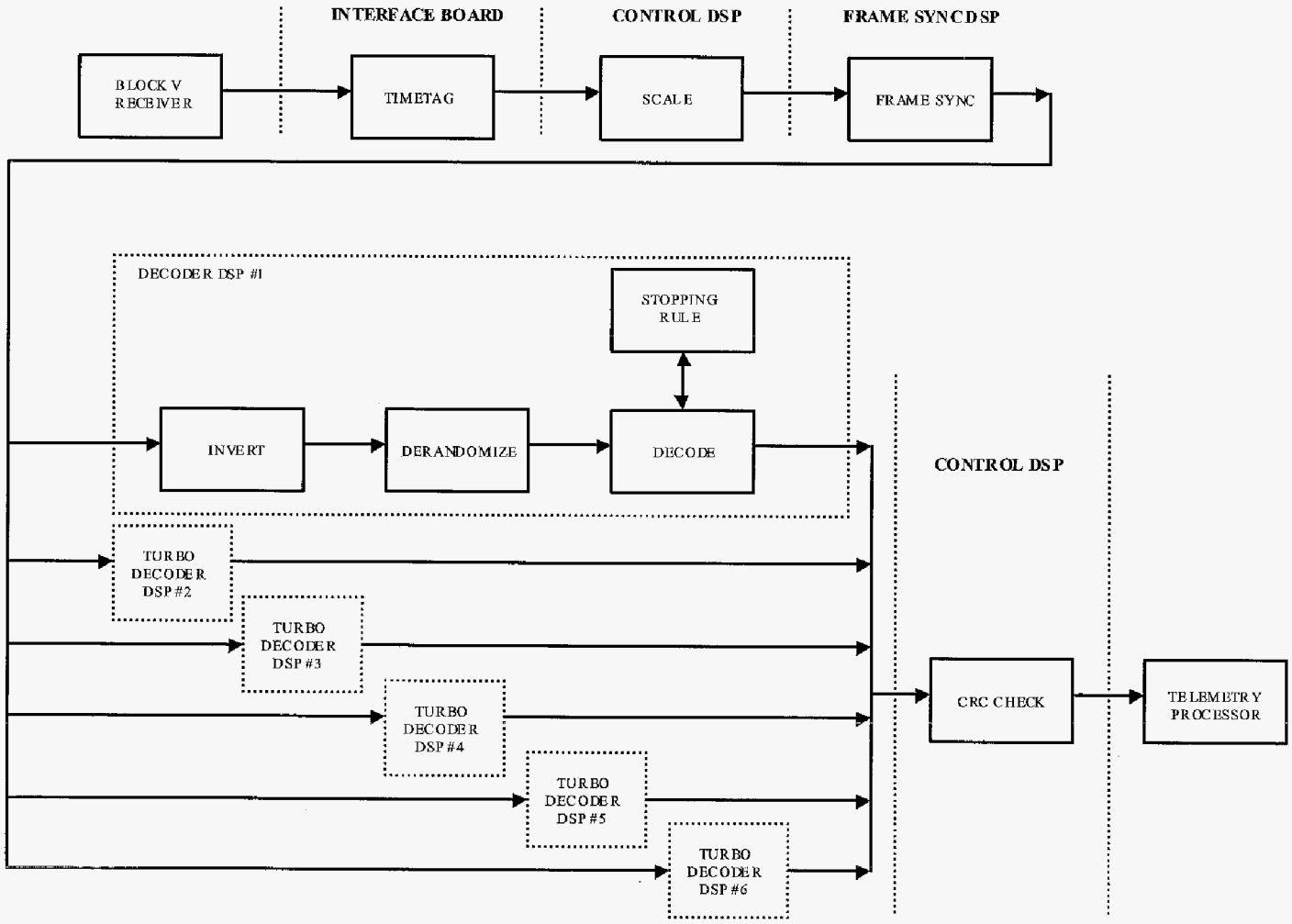
- TO DETECT DECODING FAILURES, TURBO ENCODED BLOCKS SHOULD USE CCSDS FRAME ERROR CONTROL FIELD (FECF)
  - FECF IS A 2 BYTE CRC
- PSEUDO-RANDOMIZATION IS ALSO RECOMMENDED TO AID IN RECEIVER TRACKING
  - AVOIDS LONG SEQUENCES OF NO TRANSITIONS

DECODER

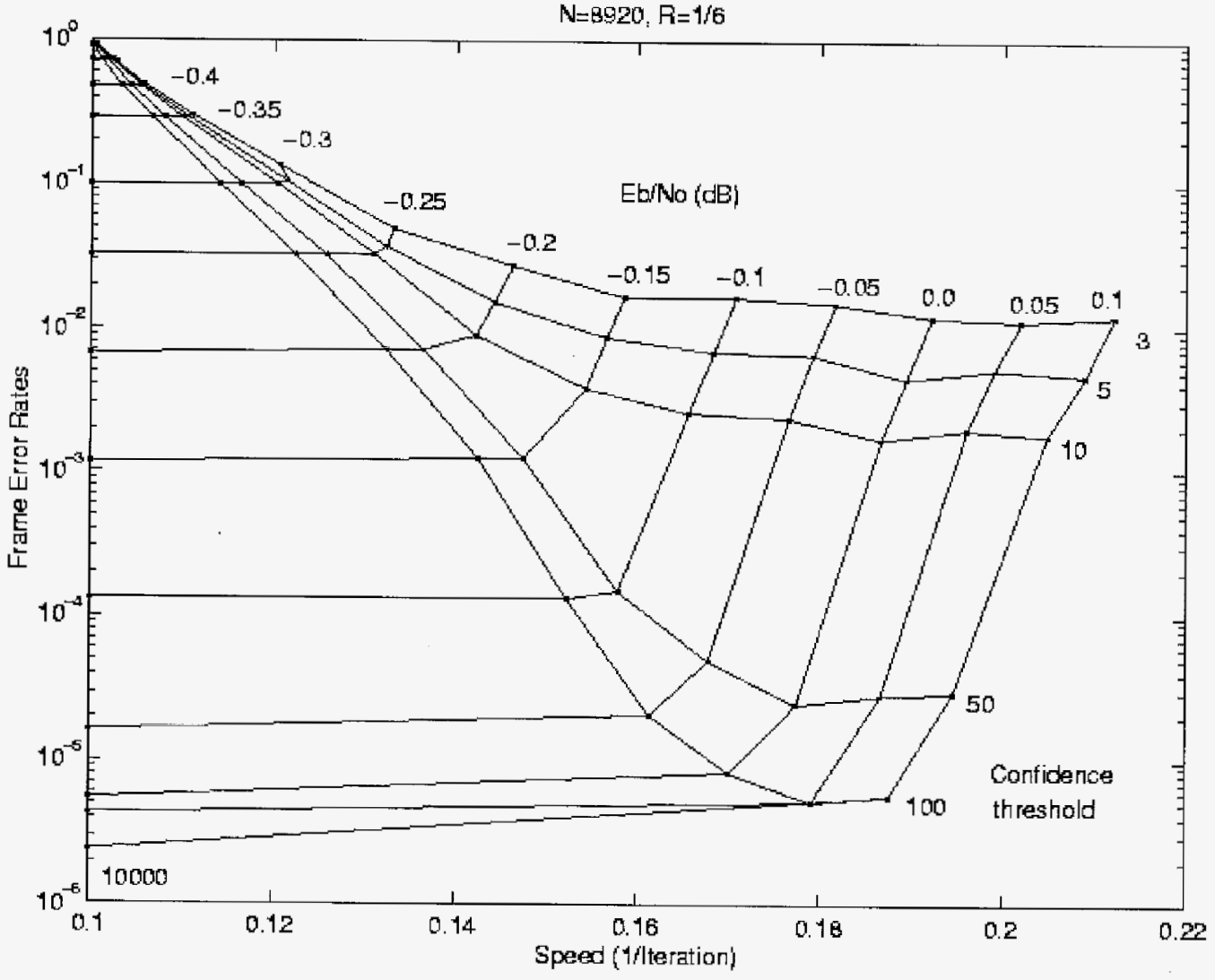


- DECODER PERFORMS SEVERAL FUNCTIONS
  - TIME TAGGING
    - 0.1 μSEC RESOLUTION
  - FRAME SYNCHRONIZATION
    - DONE IN SYMBOL DOMAIN
    - MULTIPLE FRAMES USED
  - PSEUDO-DERANDOMIZATION
  - TURBO DECODING
  - CRC CHECK
- DECODER IS AN ITERATIVE PROCESS
  - EITHER RUNS FOR A FIXED NUMBER OF ITERATIONS OR DETECTS CONVERGENCE AND STOPS (STOPPING RULES)
- SINCE TURBO CODES ARE BLOCK CODES, SPEED CAN BE OBTAINED BY DECODING MULTIPLE BLOCKS IN PARALLEL
  - IMPLEMENTATION USES 6 DECODER ELEMENTS
  - FRAME SYNC AND I/O MUST BE DONE AT SYMBOL RATE
  - DECODERS OPERATE AT FRAME RATE
    - SPEED A FUNCTION OF CLOCK RATE OF DSPs

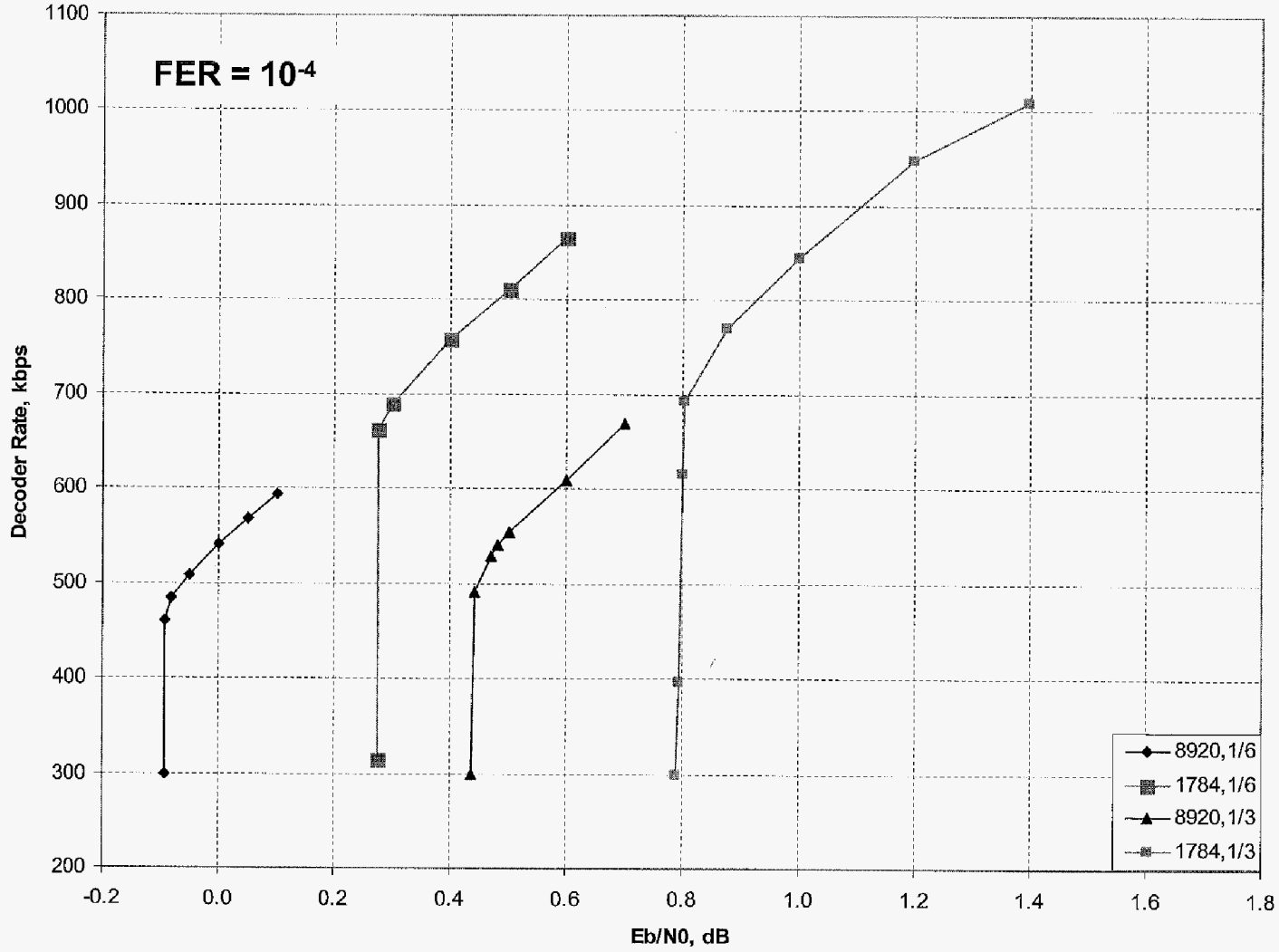
DECODER BLOCK DIAGRAM



STOPPING RULES



STOPPING RULES (CONT.)



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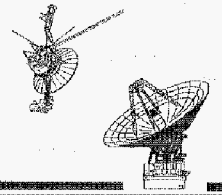
STOPPING RULES (CONT.)



- WITH 10 ITERATIONS, DECODING RATE ABOUT 300 kbps (USING 200 MHz PROCESSOR)
- WITH STOPPING RULES (STOPPING DECODING WHEN CONVERGENCE DETECTED), DECODING SPEED (WITH NEGLIGIBLE DECODING LOSS) INCREASES AS SHOWN IN CHART
  - RATE 1/6, 8920 BIT FRAME -> ~460 kbps
  - RATE 1/3, 8920 BIT FRAME -> ~490 kbps
  - RATE 1/6, 1784 BIT FRAME -> ~689 kbps
  - RATE 1/3, 1784 BIT FRAME -> ~692 kbps
- HIGHER SPEED CAN BE OBTAINED, WITH HIGHER DECODER LOSSES

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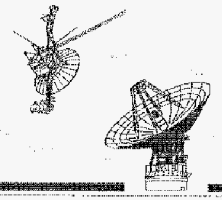
STATUS/CONCLUSIONS



- CURRENTLY DECODING AT RATES UP TO 690 kbps (1784 BIT FRAMES) WITH 200 MHz DSP
  - PROJECTS TO 1.035 Mbps (1784 BIT FRAMES) FOR 300 MHz DSPs
  - DEPENDS ON FRAME SIZE AND CODING RATE
- IMPLEMENTATION UNDERWAY
  - WILL BE INSTALLED IN ALL 34M/70M ANTENNAS BY 10/03
- MESSENGER AND STEREO PLANNING TO USE TURBO CODING