Evolvable Hardware System at Extreme Low Temperatures

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Abstract

This paper describes circuit evolutionary experiments at extreme low temperatures, including the test of all system components at this extreme environment (EE). In addition to hardening-by-process and hardening-by-design, "hardening-by-reconfiguration", when applicable, could be used to mitigate drifts, degradation, or damage on electronic devices (chips) in EE, by using re-configurable devices and an adaptive self-reconfiguration of their circuit topology. Conventional circuit design exploits device characteristics within a certain temperature/radiation range; when that is exceeded, the circuit function degrades. On a reconfigurable device, although component parameters change in EE, a new circuit design, suitable for new parameter values, may be mapped into the reconfigurable structure to recover the initial circuit function. This paper demonstrates this technique for circuit evolution and recovery at liquid nitrogen temperatures (-196.6°C). In addition, preliminary tests are performed to assess the survivability limitations of the evolutionary processor at extreme low temperatures.

1. Introduction

Future NASA missions to Moon, Mars and Beyond will face Extreme Environments (EE), including environments with large temperature swings, such as between -180°C and 120°C at the initial landing sites on the Moon, low temperatures of -220 °C to -233°C during the polar/crater Moon missions, and -180°C for Titan *in-situ* mission. High temperatures of 460°C and harsh sulfuric acid environment will be encountered for Venus Surface Exploration and Sample Return mission. High radiation levels will be faced for Jupiter's Icy Moons Orbiter (JIMO) missions: 5MRad Total Ionizing Dose (TID) for Europa Surface and Subsurface mission. These extreme environments of extreme low temperatures and high radiation induce drifts, degradation, or damage into electronic devices and reliability issues of package designs and associated materials.

The current approach for space electronics designs is to use commercial-of-the-shelf or military range electronics protected through passive (insulation) or active thermal control, and heavy metal (high weight)shielding for radiation reduction. This adds to increase in sizable weight and volume, compounded by power loss, and additional cost for the mission. More importantly, as missions will target operations with smaller instruments/rovers and operations in areas without solar exposure, these approaches sometimes become infeasible and it will be more expensive. In many cases the electronics must be collocated with the sensor or actuator in the extreme environment, without the option of being insulated or shielded properly, for example panoramic camera and its electronics in Mars Exploration Rover project. Therefore, developing EE-robust electronics would have several advantages including lower costs, less power, no thermal control, and offering in some cases, the only reasonable solution.

Conventional approaches to Extreme Environment Electronics include *hardening-by-process* (HBP), i.e. fabricating devices using materials and device designs with higher tolerance to EE, (e.g using special materials like Silicon Carbide for high temperatures, or Silicon-on Insulator for radiation, ceramic materials for packaging). Another promising approach is *hardening-by-design* (HBD), i.e. use of special design/compensation schemes. For example, circuit techniques, such as auto-zero correction, are used to alleviate the problem of the (temperature dependent) offset voltages in Operational Transconductance Amplifiers (OTA) operated at low temperatures [1]. Both these hardening approaches are limited, in particular for analog electronics, by the fact that current designs are fixed and, as components are affected by EE, these drifts alter functionality.

A recent approach pioneered by JPL is to mitigate drifts, degradation, or damage on electronic devices in EE by using re-configurable devices and an adaptive self-reconfiguration of circuit topology. This new approach, referred here as hardening-by-reconfiguration (HBR) mitigates drifts, degradation, or damage on electronic devices in EE by using reconfigurable devices and an adaptive self-reconfiguration of circuit topology. In HBR, although device parameters change in EE, while devices still operate (albeit on a different point of their characteristic) a new circuit design, suitable for new parameter values, is mapped into the reconfigurable system to recover the initial circuit functionality. Partly degraded resources are still used, while completely damaged resources are bypassed. The new designs, suitable for various environmental conditions, can be determined prior to operation or determined in-situ by reconfiguration algorithms running on a built-in digital controller.

The scope of this paper is on HBR for extreme low-temperatures, since other studies have been performed for high temperatures and radiation environments [2]. The application here described encompasses the separate testing of the whole Evolvable Hardware system (Evolutionary Processor + Re-configurable chip) at low temperatures, following the assumption that the entire system will be exposed to the space EE. In the experiments, we demonstrate the evolution and recovery of circuits at liquid nitrogen temperatures (-196.5°C) and verify the operational limitation of the evolutionary processor at low temperatures. This adds to our previous experiments where only the re-configurable chip was exposed to EE [2].

The Stand-Alone Board Level Evolvable (SABLE) system [3] designed by JPL is used in the experiments described in this paper. This system is constituted by a Digital Signal processor (DSP) working as an evolutionary processor and a reconfigurable mixed signal chip, the Field Programmable Transistor Array (FPTA). Section 2 of this paper overviews the SABLE system. Section 3 describes the experiments and section 4 concludes the research work performed.

2. Overview of SABLES

SABLES integrates an FPTA and a DSP implementing the Evolutionary Processor (EP) as shown in Figure 1. The system is stand-alone and is connected to the PC only for the purpose of receiving specifications and communicating back the results of evolution for analysis [3].

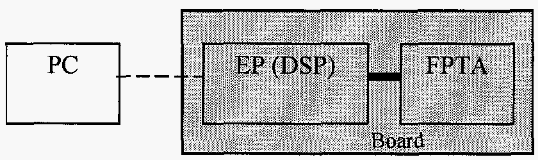

Figure 1. **Block diagram of a simple stand-alone evolvable system.**

The FPTA has transistor level reconfigurability, consisting of an 8x8 array of reconfigurable cells. Each cell has a transistor array as well as a set of other programmable resources, including programmable resistors and static capacitors. Figure 2 provides a detailed view of the reconfigurable transistor array cell. The reconfigurable circuitry consists of 14 transistors connected through 44 switches and is able to implement different building blocks for analog processing, such as two- and three-stage OpAmps and Gaussian computational circuits. Details of the FPTA-2 can be found elsewhere [2,3].

The evolutionary algorithm is implemented in a DSP that directly controls the FPTA-2, together forming a board-level evolvable system with fast internal communication ensured by a 32-bit bus operating at 7.5MHz. Details of the evolutionary platform (EP) were presented in [4]. Over four orders of magnitude speed-up of evolution was obtained on the FPTA-2 chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit).

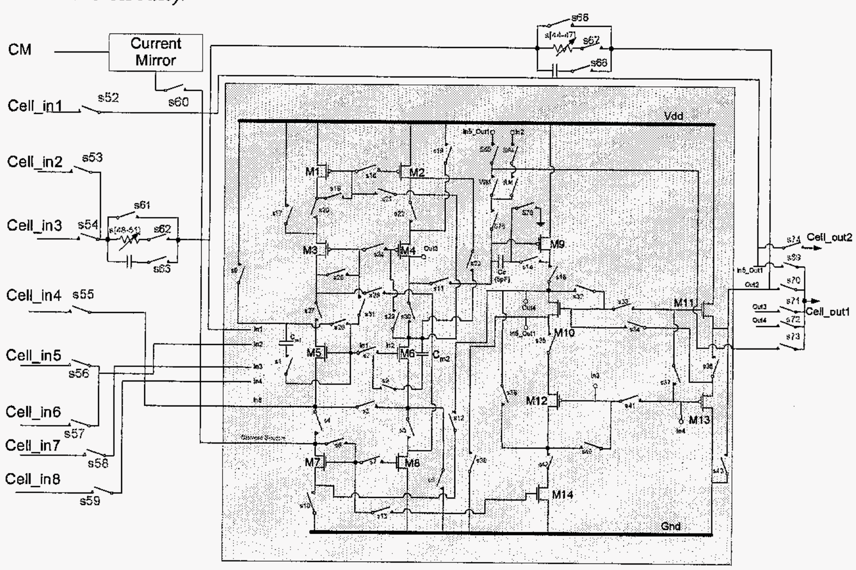

Figure 2: Schematic of the FPTA-2 Cell.

3. Low Temperature Experiments

This paper particularly focuses on analog/digital electronics at low-temperatures [5]. The experiments cover separate tests of the whole Evolvable Hardware system: the Evolutionary Processor (the DSP in the SABLE system) and the FPTA tested at low temperatures.

3.1 DSP Tests at low-temperatures

Previous experiments focused exclusively on the tests of the FPTA chips at extreme environments. However, no tests have been reported so far on the behavior of the Evolutionary Processors (EP) at extreme environments. This particular experiment focuses on low-temperature characterization of the DSP working as the EP.

A 320C6701 DSP was tested in a board fabricated by Innovative Integration (SBC62). The board communicates with a PC through a JTAG connection. During the test only the DSP board was placed on the low-temperature chamber: the PC and the JTAG were outside. The FPTA chip was not used in this arrangement.

The DSP was tested by running a simple Generic Algorithm (GA) whose target was a simple optimization problem (the maximization of the number of '1's in the chromosomes). This problem is solved in less than 1 minute, after 464 generations. The GA results are deterministic, i.e., the same for each run.

The temperature of the chamber/test article has been driven to 0°C with a scan rate of 5°C/min from room temperature. The dwell time at 0°C temperature was for 8 minutes and electrical measurements were made during this time. Later, the temperature of the chamber has been driven to –30°C, –60°C, –90°C, –120°C at a scan rate of 5°C/min and electrical measurements were made respectively during the dwell (Figure 3).

A Failure was observed during the testing at –120°C step. Electrical measurements were made at –90°C again and the DSP regained its characteristics. This procedure was repeated again: the temperature was driven to –90°C, –100°C, –110°C and –120°C to narrow the temperature range. The dwell time at each temperature was for 5 minutes and electrical measurements were made during this time. The DSP was functioning at –90°C, –100°C, and –110°C. The failure was again observed during the testing in a temperature range of –110°C to –120°C. During the failure the DSP did not communicate with the PC. The PC-DSP communication link was the only means to read out the DSP outputs in this experiment.

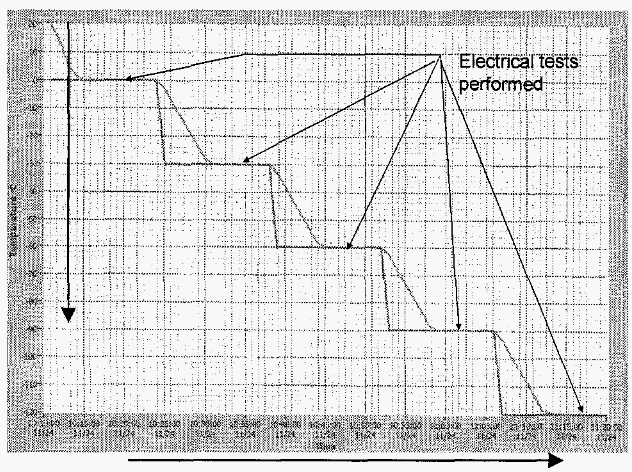

Figure 3: Temperature Profile in the DSP Test. Time in the horizontal axis and temperature in the vertical axis.

Other Evolutionary Processors implementations, including FPGAs and other DSP models, will be tested. The final goal of the experiments is to have an implementation operational at -180°C or below.

3.2 Half-Wave Rectifier

The low temperature test bed for these experiments used liquid nitrogen, establishing a temperature of -196.5°C. In order to study the effect of low temperatures on the FPTA device only (the DSP was at room temperature), the chip was placed on a separate board that was immersed into liquid nitrogen. This setup did not allow a control for intermediate temperatures between room ambient and liquid nitrogen as described in the previous experiment. A standard ceramic package was used for the chip. A half-wave rectifier was then evolved at -196.6°C with the following setup.

The fitness function given below does a simple sum of errors between the target function and the output from the FPTA. The input was a 2 kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for}\,(t_s < n/2) \\ R(t_s) - V_{\max}/2 & \text{otherwise} \end{cases}$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{max} is 2V (the supply voltage). The output must follow the input during half-cycle, staying constant at a level of half way between the rails (1V) in the other half.

After the evaluation of 100 individuals, these were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), either among themselves or with an individual from the elite, and then mutation (4% rate). The entire population was then reevaluated. The experiment used 2 cells and was run for 300 generations.

The oscilloscope caption is shown in Figure 4a. This was not a robust solution (and it was not even expected to be, since evolutionary algorithm was not asked, through the fitness function, to respond to an entire temperature range) and when taken out to room temperature the response deteriorated as shown in Figure 4b.

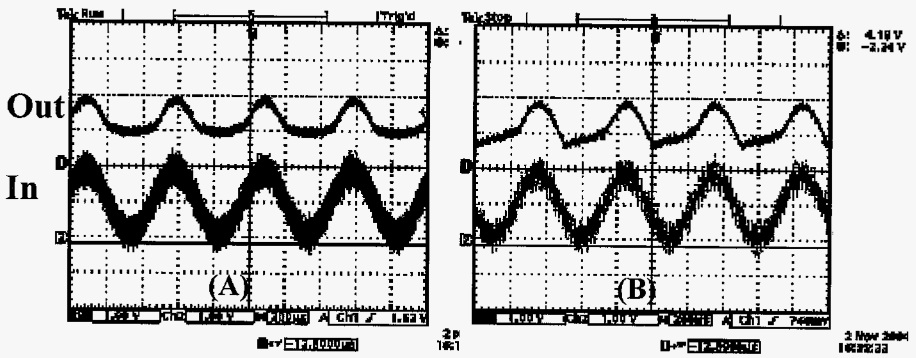

Figure 4: Half-wave rectifier evolved at -196C (A); solution is not robust and degrades when returned to room temperature (B). An environmental noise signal is also present at the circuit input.

3.3 NOR Gate

A NOR gate was evolved at -196.5°C using the same method described in section 3.2. Two FPTA cells were used and the experiment processed 100 individuals along 300 generations. Figure 5.a shows the oscilloscope picture of the evolved solution at -196.6°C. The same solution was tested at room temperature using another FPTA chip, producing an almost identical behavior (Figure 4b) opposing to the rectifier case study.

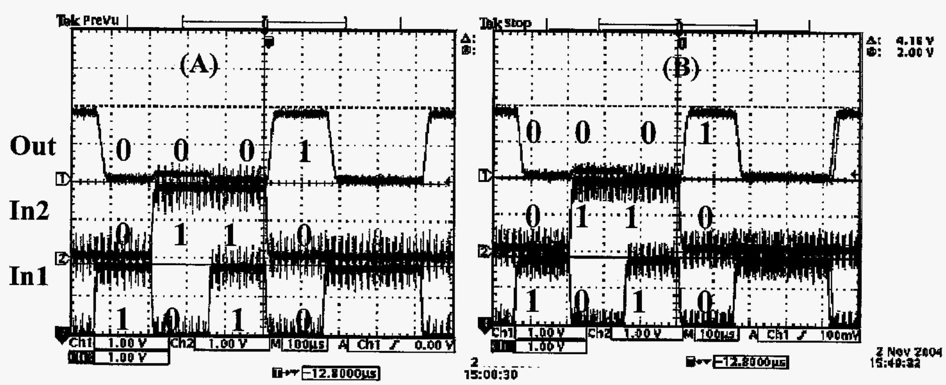

Figure 5. NOR circuit evolved and tested at -196.5°C (A); the same circuit was tested successfully at room temperature (B). An environmental noise signal is also present at the circuit input.

3.4 Recovery of Controllable Oscillator at Low Temperatures

Four cells of the FPTA were used to evolve a controllable oscillator. This circuit receives a digital input and it should oscillate when the input is at one digital level (either '0' and '1') and stay at ground for the other level. Initially, a controllable oscillator was evolved at room temperature, the circuit behavior being depicted in Figure 6a. The circuits output a 70kHz sine wave (with a small degree of harmonic components) when the input is '0'. When the same circuit is tested at -196.5°C, it can be observed a distortion (increase in harmonics) at the output (Figure 6b).

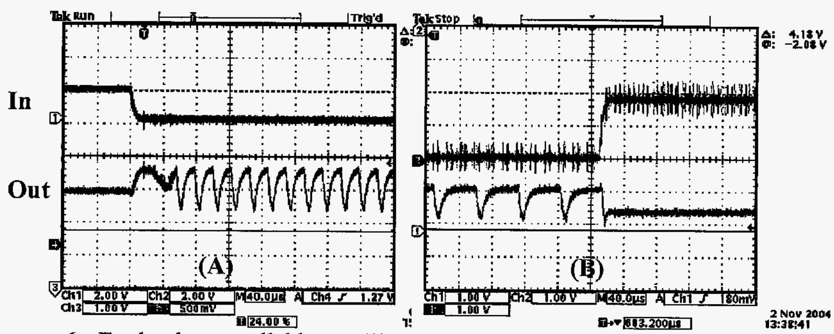

Figure 6: Evolved controllable oscillator at room temperature and deteriorated response at -196.6°C.

The controllable oscillator was evolved again at -196.5°C, the response being displayed in Figure 7. It can be observed that the output distortion largely removed. In addition, evolution found a circuit that oscillates for a high level input, opposing to the room temperature solution.

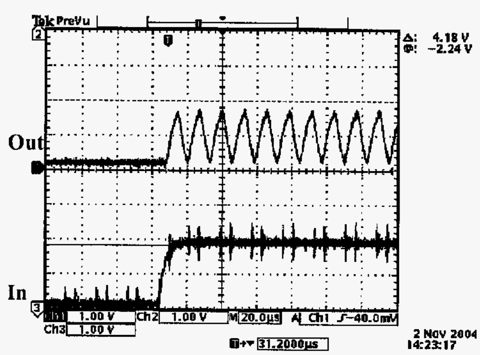

Figure 8. Evolved controllable oscillator at low temperature.

4. Conclusions and Future Work

The results summarized above prove the concept, yet have the following limitations: 1) the tests were of short duration, 2) did not implement temperature cycling, 3) did not use the combined EHW system (DSP and FPTA) at low temperature simultaneously, 4) were not demonstrated on complex analog or digital circuits performing in an application.

Particularly, the DSP Board worked down to -110°C, but failed for further lower temperatures. A short-term goal is to test other Evolutionary Processor implementations, such as FPGAs, for an extended operation at -180°C.

Longer term goals planned for this effort are: demonstrate the integrated reconfigurable array-reconfiguration logic in the same chip under temperatures cycles accurately replicating those in Moon and Mars and for longer duration and in combined radiation/temperature tests, performing a sensor processing function. More specifically, the overall objective of the new effort is to develop/demonstrate reconfigurable analog electronics performing characteristic analog functions (filtering, amplification, etc) for extended operations in extreme environment with temperatures cycling in the range of –180°C and 120°C and cumulative radiation of at least 300kRad total ionizing dose (TID). The objective is to develop and validate Self Reconfigurable Electronics for Extreme Environments (SRE-EE) technology by demonstrating a Self-Reconfigurable Analog Array (SRAA) IC in sustained (over 200 hours) operation at temperatures between -180°C and 120°C, and irradiated to 300kRad total ionizing dose (TID). The temperature range of -180°C and 120°C covers the temperature range for both Moon and Mars environments and 300kRad TID reflects accumulative dose during very long Mars missions (100kRad for near-term missions), or missions beyond the Moon and Mars, such as to Jupiter's Icy Moons. This would validate the technology for Moon and Mars temperature and Jupiter radiation environments and the even harsher radiation environments for missions beyond.

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