

## A BACK-ILLUMINATED MEGAPIXEL CMOS IMAGE SENSOR

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In this paper, we present the test and characterization results for a back-illuminated megapixel CMOS imager. The imager pixel consists of a standard junction photodiode coupled to a three transistor-per-pixel switched source-follower readout [1]. The imager also consists of integrated timing and control and bias generation circuits, and provides analog output. The analog column-scan circuits were implemented in such a way that the imager could be configured to run in off-chip correlated double-sampling (CDS) mode. The imager was originally designed for normal front-illuminated operation, and was fabricated in a commercially available 0.5  $\mu\text{m}$  triple-metal CMOS-imager compatible process. For backside illumination, the imager was thinned by etching away the substrate was etched away in a post-fabrication processing step.

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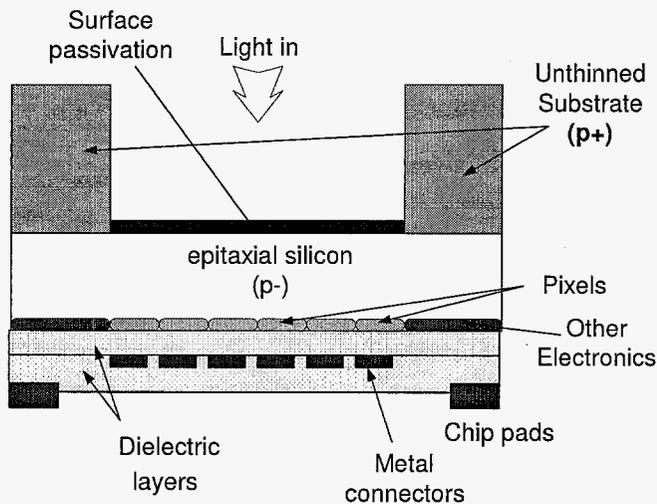


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The imager was thinned at an individual die level using a frame-thinning approach. Only the pixel area was thinned down to  $\sim 7\text{-}10 \mu\text{m}$  thickness (corresponding to epitaxial silicon thickness), leaving a thick peripheral region ( $\sim 1 \text{ mm}$  wide). A surface passivation step was then applied to the thinned silicon layer.

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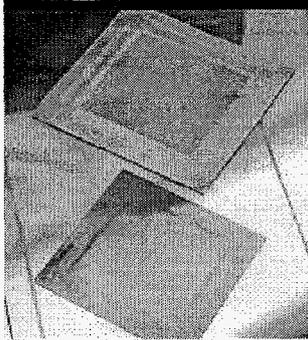


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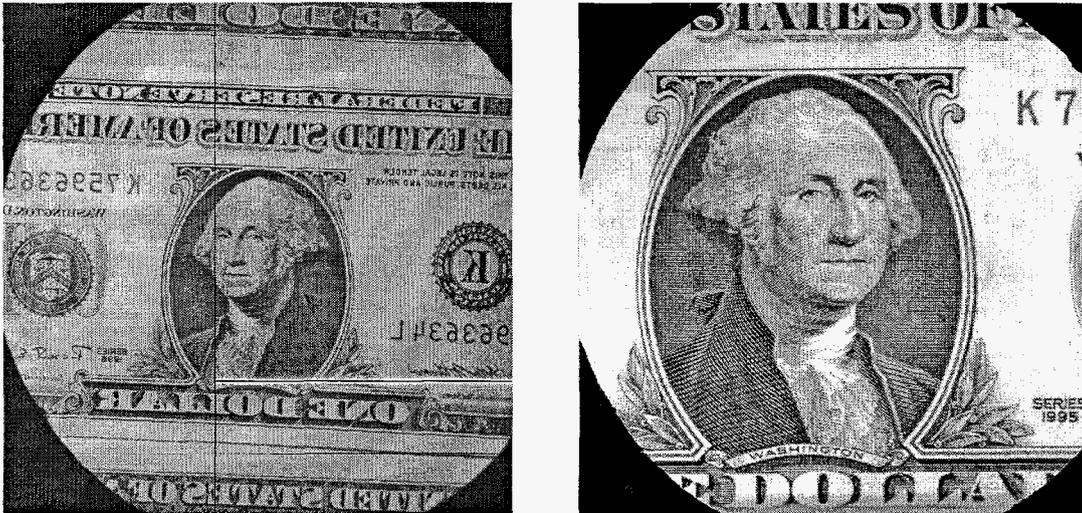


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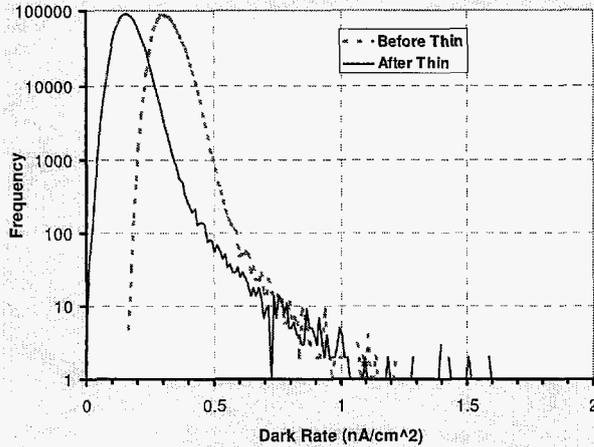


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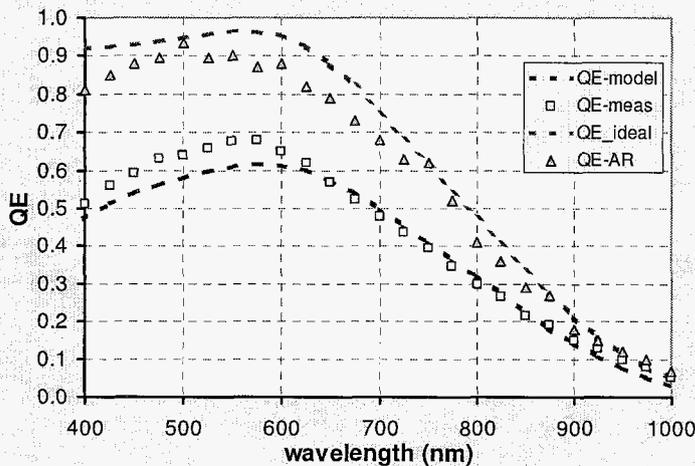


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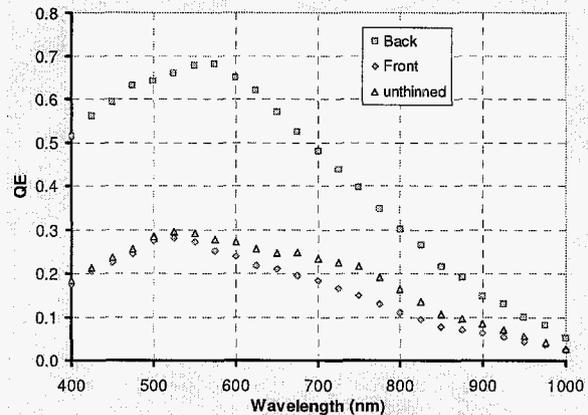


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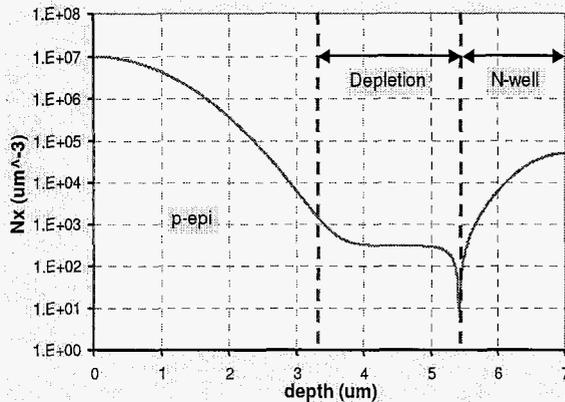


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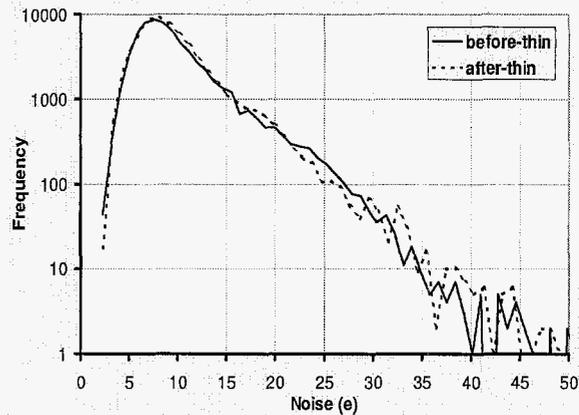


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#### References:

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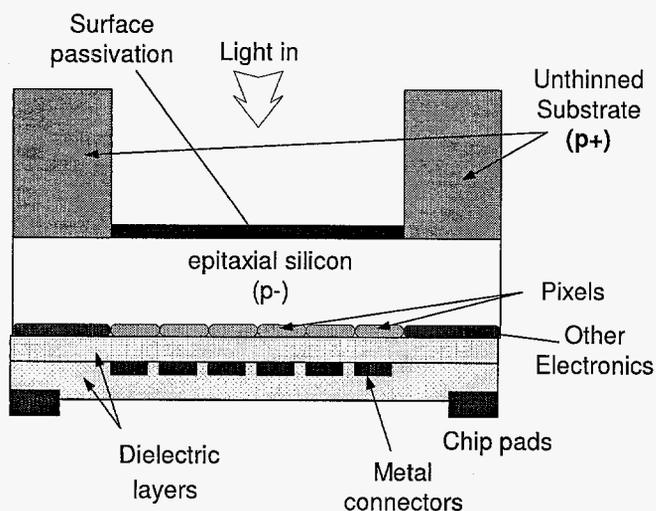
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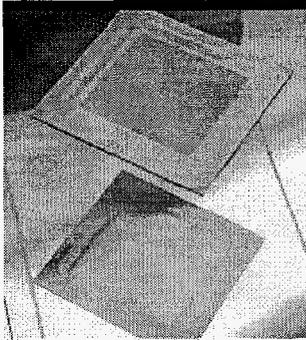


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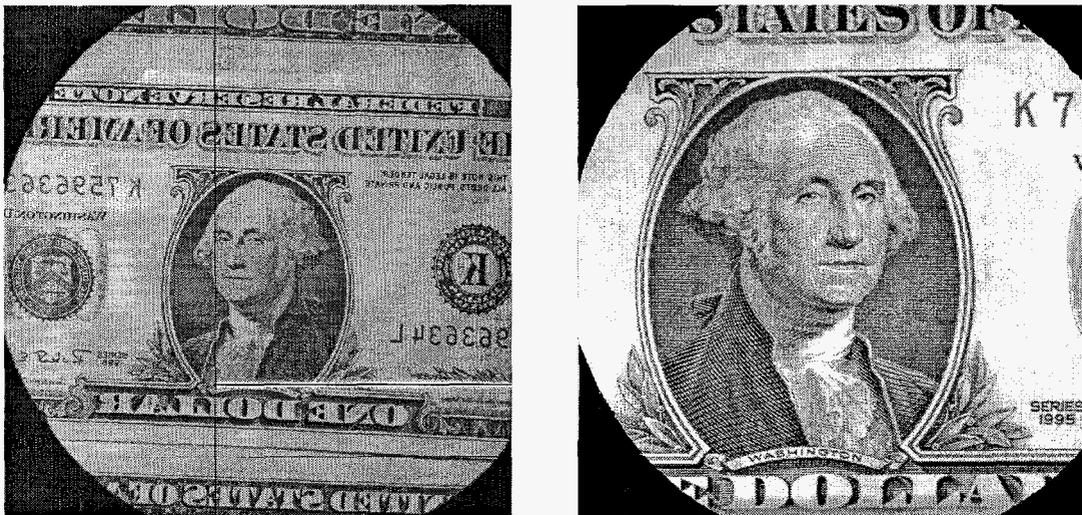


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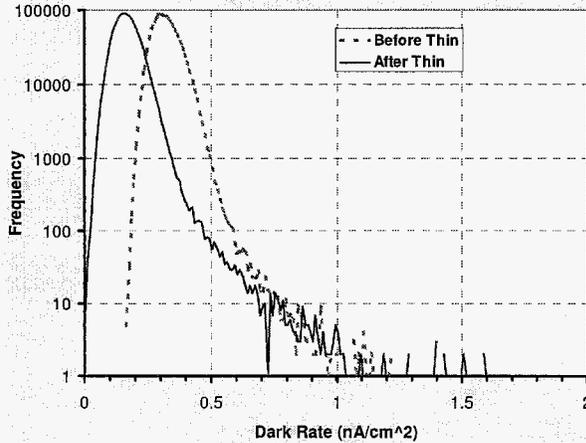


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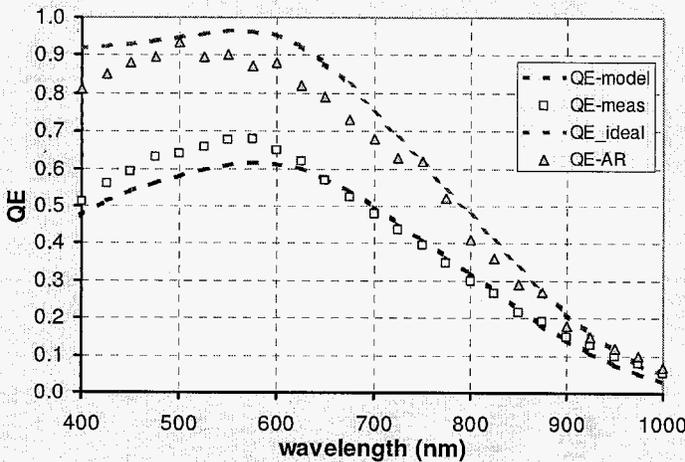


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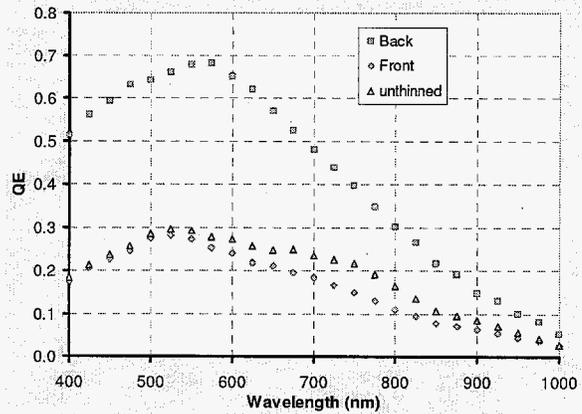


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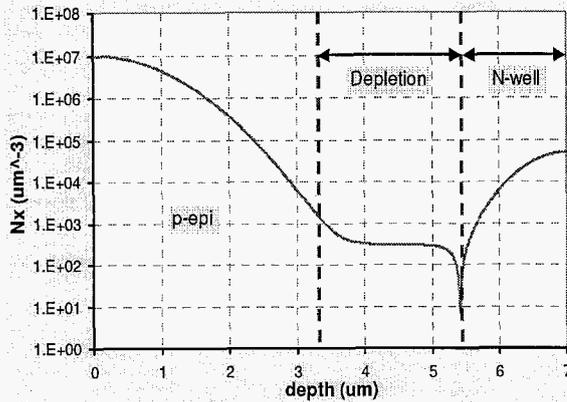


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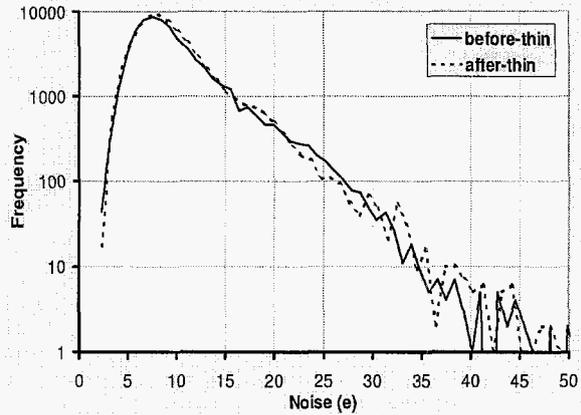


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