Beyond G-Band: A 235 GHz InP MMIC Amplifier

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***Abstract*—We present results on an InP monolithic millimeter-wave integrated circuit (MMIC) amplifier having 10-dB gain at 235 GHz. We designed this circuit and fabricated the chip in Northrop Grumman Space Technology's (NGST) 0.07-μm InP high electron mobility transistor (HEMT) process. Using a WR3 (220–325 GHz) waveguide vector network analyzer system interfaced to waveguide wafer probes, we measured this chip on-wafer for S-parameters. To our knowledge, this is the first time a WR3 waveguide on-wafer measurement system has been used to measure gain in a MMIC amplifier above 230 GHz.**

***Index Terms*—G-Band, high electron mobility transistors (HEMTs), indium phosphide, millimeter wave field-effect transistor (FET) amplifiers, monolithic millimeter-wave integrated circuits (MMICs), WR3 waveguide.**

I. Introduction

In THIS letter, we describe the device technology, amplifier design, and measurements for a monolithic millimeter-wave integrated circuit (MMIC) amplifier having gain in the 220–325 GHz WR3 waveguide band, with a peak gain of +10 dB at 235 GHz. Prior to this work, the highest reported frequency for a MMIC amplifier was 225 GHz, from an InP metamorphic high electron mobility transistor (HEMT) MMIC with four-stages in a coplanar waveguide cascode configuration, using 0.1 μm gate lengths and having over 10 dB gain [1]. Earlier results at 215 GHz, from an InP HEMT MMIC having six stages in a grounded coplanar waveguide topology with wet-etched through-substrate vias and 0.08 μm gate-lengths, had 15-dB gain [2]. Both of these results represented an enormous breakthrough for MMIC amplifiers. Even the measurement apparatus for on-wafer S-parameters up to 220 GHz was in the early stages of development only six years ago, when the first full two-port S-parameter on-wafer vector network analyzer capability was reported [3].

Today, many results of MMIC amplifiers have been reported in G-Band (140–220 GHz). These include high performance InP HEMT low noise amplifiers, modules and receivers at 183 GHz and beyond [4]–[6], InP heterojunction bipolar transistor (HBT) amplifiers [7], double heterostructure bipolar transistor amplifiers (DHBTs) for power amplifier applications [8], and InP HEMT medium power amplifiers [9]. InP MMIC amplifier technologies have evolved to produce consistent, high yield chip designs throughout G-Band. Advances in test equipment have made the measurements of these chips straightforward and reliable, enabling improvements in the various device technologies. Present day high-speed transistors used in high performance MMICs have cutoff frequencies f_T of 250 to 300 GHz.

Some of the applications for MMIC amplifiers at these high frequencies include advanced communications, millimeter-wave radar, active and passive millimeter-wave imaging, and radiometer instruments for atmospheric measurements [10].

For this letter, we report on the advances in state-of-the-art InP HEMT technology, as well as enhanced on-wafer measurement capability up to 325 GHz, which have enabled the development of a 235 GHz MMIC amplifier chip.

II. Device Technology

The 75% indium channel heterostructure and 0.07-μm gate-length T-gate InP HEMT process provide the high gain and cutoff frequency that are required for the WR3-band MMIC. The InP HEMT epitaxial layer structures were grown by molecular beam epitaxy (MBE) at Northrop Grumman Space Technology (NGST) on 3-in semi-insulating InP substrates. The InP HEMT material structure is single-side delta-doped, and includes a 75% indium channel. Room temperature Hall measurements typically yield mobilities of 12000 cm^2/Vs and channel electron carrier densities of 3.5×10^{12} cm^{-2}. The device process enhancements made for G-Band MMICs are detailed in [11] and [12].

The wafers were processed similarly to the baseline NGST 0.1 μm gate InP HEMT MMIC production process, with RF circuit yields of 80%. The frontside InP HEMT MMIC process provides 75-nm silicon nitride passivated 0.07-μm T-gate HEMT devices, 100 Ω/sq thin film resistors, 300-pF/mm^2 metal-insulator-metal capacitors, and two levels of metal interconnects. The only modification made in the frontside process for the 0.07-μm MMIC wafers was to reduce the gate length to 0.07 μm, and change the gate recess targeting to maintain aspect ratio as needed due to the shorter gate length and 75% indium channel heterostructure MBE material.

The backside InP HEMT MMIC process provides a 50-μm-thick wafer with dry-etched through-substrate vias which connect the backside metal ground plane to the frontside device and circuit elements. In order to minimize source inductance and maintain high device gain, compact 25-μm diameter dry-etched through-substrate vias are used with compact 40-μm frontside metal pads.

The 0.07-μm gate HEMTs typically average peak transconductance (G_{mp}) values above 1400 mS/mm and cutoff frequency f_T above 250 GHz. The simulated maximum available

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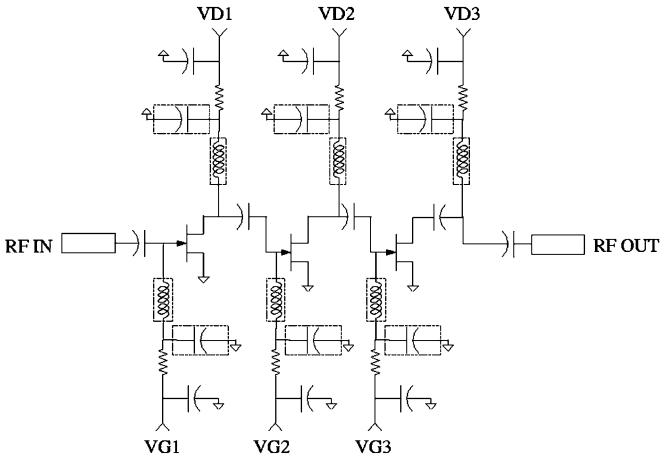

Fig. 1. Schematic of the 235-GHz MMIC. Capacitors and inductors which are boxed indicate open stubs and high impedance transmission lines, respectively.

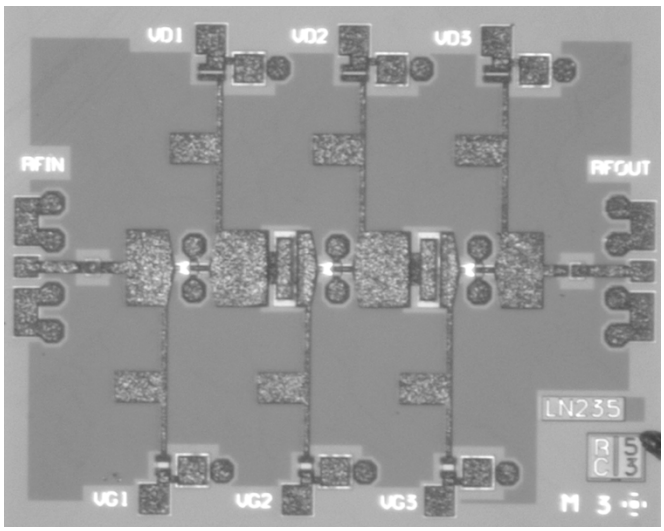

Fig. 2. Chip photograph of the MMIC amplifier.

gain (MAG) at 235 GHz is approx. 4.2 dB, with an estimated maximum frequency of oscillation, $f_{\max}$, of 400 GHz.

III. Circuit Design

The chip was designed using two-finger HEMT devices having gate widths of 15 μm each, for a total gate periphery of 30 μm. Three stages were employed with dual source vias on each HEMT device. RF matching was accomplished using microstrip transmission lines and metal-insulator-metal capacitors. We designed each stage to have a separate gate and drain bias pad, with quarter-wave shunt stubs employed as RF shorts to provide bias to the transistors. A schematic of the design is shown in Fig. 1. Each microstrip element was separately modeled using the ADS Momentum electromagnetic simulation tool. The chip dimensions are 0.6 mm $\times$ 0.9 mm. In Fig. 2, we show a chip photograph.

IV. On-Wafer Measurements From 220–325 GHz

In order to measure the on-wafer S-parameters in the 220–325 GHz band, we used Oleson Microwave Labs (OML) WR3 waveguide vector network analyzer extension modules interfaced to GGB Industries' WR3-waveguide 60-μm pitch

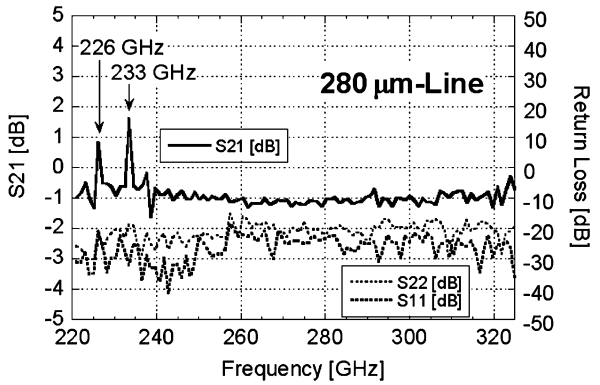

Fig. 3. S_{21}, S_{11}, and S_{22} of a 280 μm-Line calibration standard measured from 220–325 GHz. Spurs occur in the data at 226 and 233 GHz.

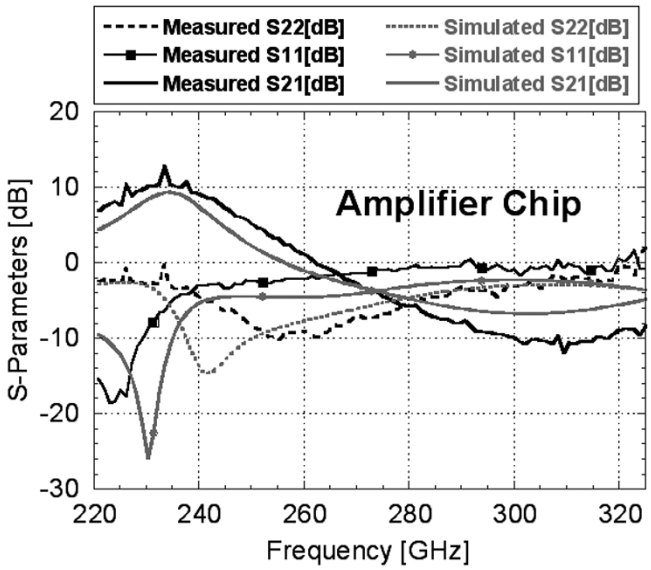

Fig. 4. On-wafer S-parameters of the amplifier chip measured with WR3 waveguide wafer probes and OML WR3 waveguide vector network analyzer frequency extension modules, and simulated chip design curves.

wafer probes. We used a line-reflect-line (LRL) calibration procedure with a standard GGB CS-15 alumina substrate, having specially laser-milled lines for the 220–325 GHz waveguide band. A standard thru-line with an impedance of 50 Ω and 175 μm in length was used for the first Line calibration standard, and for the Reflect standard, the probes were lifted off the calibration substrate. The second Line standard used was a 280-μm custom-cut line. The first and second Line length difference gives an effective electrical length corresponding to 90° at 325 GHz.

Fig. 3 shows the measured result of the 280 μm-Line calibration standard. This calibration standard is expected to show loss, as the LRL algorithm places the reference planes at the probe tips, and gives a measure of the system noise and any spurious signals. Systematic glitches appear in the data at 226 and 233 GHz, and are spurious signals generated in the harmonic mixers in the test equipment.

In Fig. 4, we show the measured S-parameter results of the amplifier chip. In order to suppress low-frequency ($<$1 GHz) gain and potential oscillations which are commonly observed with very high frequency transistors, we mounted the chip on a gold carrier and wire-bonded off-chip bypass capacitors with

values of 51 pF to each gate and drain bias pad. The second and third stage gate voltages were tied together. We biased the amplifier chip under the following conditions: $V_d = 1.3$ V, $I_d = 36$ mA, $V_{g1} = +0.31$ V, $I_{g1} = 70\ \mu$A, $V_{g2} = V_{g3} = +0.33$ V, and $I_{g23} = 140\ \mu$A. The chip exhibits at least 10-dB gain from 229 to 238 GHz, with input return loss of 3–15 dB and output return loss of about 3–5 dB over this frequency range. The measured gain is slightly higher than the simulated gain in Fig. 4. We can explain this by noting that the transconductance g_m varies with bias conditions, while the device model used a fixed g_m for the simulation. The variation of g_m with dc bias conditions was not taken account in the simulation, and the measurement was biased for maximum gain. The minimum in the S_{11} and S_{22} data agree to within 8% of the predicted frequency, which is reasonable agreement for our first narrow-band design attempt centered above 220 GHz. While we achieved first-pass design success of this 235-GHz amplifier, our work was based on that of [4], and refinement to the original hybrid-pi HEMT device model used for the designs in [4] was required for the success of the 235-GHz design.

The glitches observed at 226 and 233 GHz are systematic spurs, like the ones observed in the measurements of the 280-μm Line. Similar spurs have been observed in prior amplifier data, particularly near the band edges in waveguide vector analyzer measurements [13]. To confirm our results, we measured two different chips which exhibited similar S-parameter curves within 1 dB of each other. Both chips had significant gain up to 260 GHz. Apart from the narrow band frequency spurs at 226 and 233 GHz, we estimate the error in the measurement of S_{21} to be within 1 dB.

V. Conclusion

We have designed, fabricated and measured an amplifier chip on-wafer with 10-dB gain at 235 GHz. Applications of this work include low-noise receivers for atmospheric sounding, and millimeter-wave imaging. Future work will involve packaging this MMIC in a waveguide module and measuring its noise figure and 1-dB compression point.

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